SELECTIVE HETEROEPITAXIAL GROWTH OF GE FOR MONOLITHIC INTEGRATION OF MOSFETS AND OPTICAL DEVICES

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DOCTOR OF PHILOSOPHY

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Abstract

As Si bulk CMOS devices approach their fundamental scaling limit, diverse research is being done to introduce novel structures and materials. High carrier mobility and possible monolithic integration with Si based devices have prompted renewed interest in Ge based devices. For optical applications, it was challenging to make photodetectors operate in 1.3-1.55μm wavelength range with Si, due to its relatively large indirect (1.1eV) and direct (3.4eV) bandgaps. However, Ge's smaller direct band gap (0.8eV) corresponding to ~1.55μm in wavelength and possible monolithic integration with Si CMOS technology make Ge a strong candidate for photodetectors.

In this study, we demonstrate high performance Ge MOSFETs and optical devices which can be monolithically integrated to Si technology, by employing novel Ge heteroepitaxial growth and in-situ dopoing technique.

In the first part of the thesis, selective Ge heteroepitaxial growth on Si and in-situ doping technique for n+/p junction are discussed. Surface roughness of heteroepitaxially gorwn Ge on Si is considerably reduced by high temperature hydrogen annealing. Ge growth and hydrogen annealing steps are repeated until desired epi layer thickness is reached. High quality Ge film (minimal dislocation ($1x10^7 cm^{-2}$) and very smooth surface (0.65nm (RMS)) is achieved selectively on Si using SiO_2 window. For abrupt and box shaped n+/p junction in Ge, in-situ phosphorus doping using PH_3 is employed during the epitaxial growth. Temperature dependency of the dopant activation was investigated associated with the shallower and abrupt junction formation. Novel n+/p diodes show better characteristics (on/off ratio and on current density) compared with conventional ion-implanted junction. High performance Ge MOSFETs and optic devices fabricated using selective Ge heteroepitaxial growth on Si are discussed in the second part of the thesis. For n-MOSFETs, in-situ doping technique is used to form source and drain with very low

series resistance and shallow junctions. p-MOSFETs are fabricated with high-k/metal gate stack. Results show the highest electron mobility ever reported on (100) Ge n-MOSFETs and ~80% enhancement of hole mobility over Si universal mobility for p-MOSFETs. Normal incidence p-i-n photodiodes on selectively grown Ge are also demonstrated. Enhanced efficiency in the near infrared regime and the absorption edge shifting to longer wavelength is achieved due to residual tensile strain. Measured responsivities are promising towards monolithically integrated on-chip optical links and in telecommunications.

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I dedicate this work to them.

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CHAPTER 1:

Introduction

This dissertation describes our contributions on monolithic integration of Ge on Si for the CMOS technologies and optical detection technologies. This introductory chapter begins with a brief background and discussion of the motivation of this work. The limitations of scaling of conventional Si bulk MOSFETs and electrical wires are summarized. Finally, the organization of the dissertation is presented.

1.1 Motivation

The Silicon Metal-Oxide-Semiconductor Field Effect Transistor has been the workhorse of the semiconductor industry for the last three to four decade. Device scaling has improved both packing density and transistor performance, resulting in increase in cost per function, which propelled the success of semiconductor industry. Fig 1.1 depicts the exponential increase in microprocessor performance represented by millions of instructions per second, over technology generations. Even though the physical dimensions have been continually shrinking by a factor of 2-3 in accordance with Moore's Law [1], the fundamental architecture and materials of the device has remained the same. However, as we further shrink the device dimension, transistor with conventional structure and material is reaching its fundamental scaling limit. Without change in transistor geometry and introduction of novel materials, exponential decrease in device dimensions cannot continues further, as beyond the 22nm node fundamental as well as practical constraints will limit the maximum performance achievable by these scaled transistors.

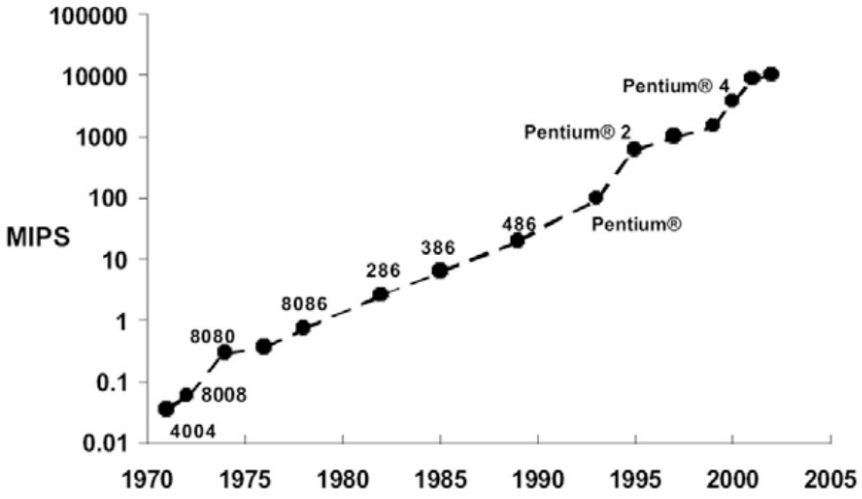

Fig. 1.1 Microprocessor performance increase due to scaling [2]

Increased performance has come at a cost of increased off state power in transistors. Fig 1.2 depicts the evolution of power density as the devices are scaled traditionally.

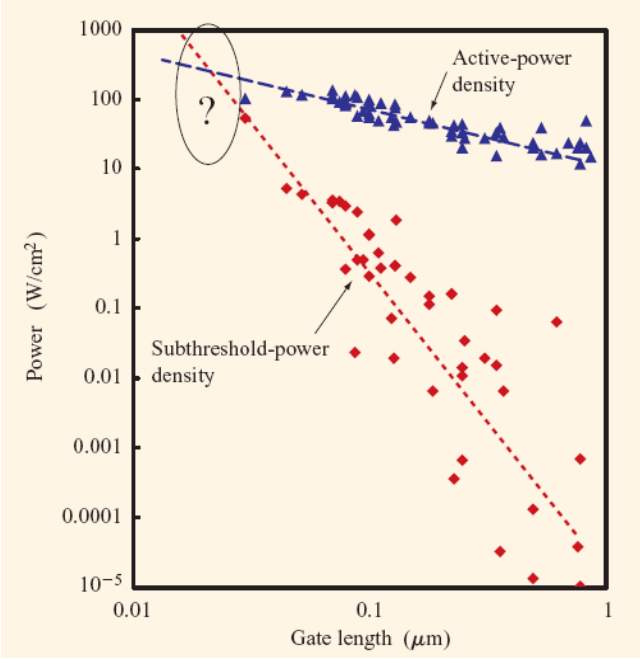

Fig. 1.2 Active and standby power density trends plotted from industry data. The extrapolations indicate a cross over below 20nm gate length [3].

The static power has increased more rapidly compared with the linear increase in the active power dissipation. Around the gate length of 20 nm, static power would approach the active power, and even surpass it, as we continue the scaling. Hence, beyond gate length of 20nm, it is questionable if the traditional scaling techniques would be effective. The major reason for this rapid increase in static power is the sub-threshold leakage. With decreasing channel length, gate bias cannot form effective potential barrier between the source and the drain when the transistor is turned off, which blocks the current flow. This results in the increased static leakage current, and increases the static power dissipation. Management and suppression of static power is one of the major challenges to continued gate length reduction for higher performance. Once the scaling of conventional bulk MOSFETs starts slowing down, the insertion of performance boosters, like novel materials and non classical device structures, will be necessary to continue to improve performance.

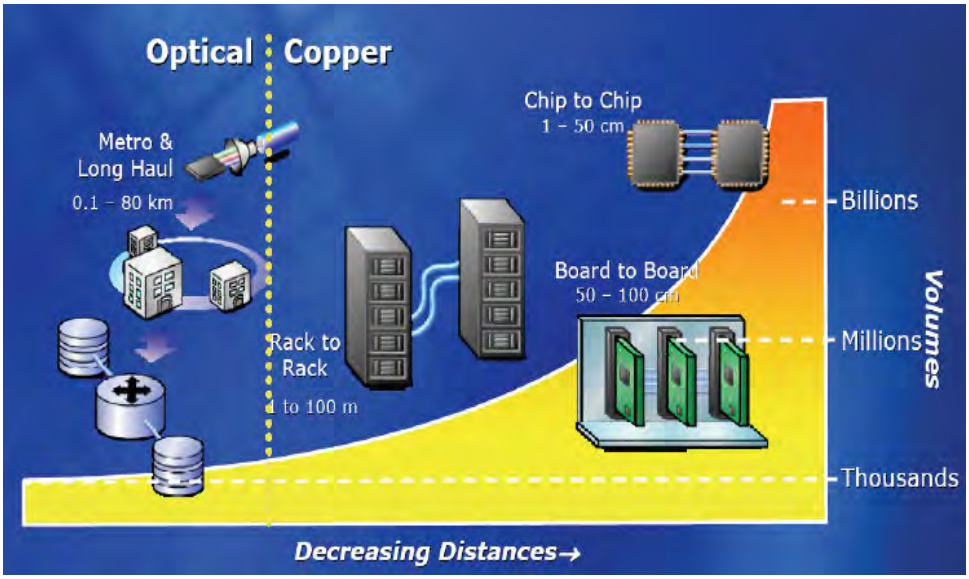

Fig. 1.3 The chain of communication systems versus the length of the interconnection and the business volume of the corresponding technology (Source: Intel)

On the other hand, while individual logic elements have become significantly smaller and faster, computational speed is limited by the communication between

different parts of digital systems. This bottle neck is identified as one of the grand challenges in the progress of integrated electronics.

Since the introduction of low-loss silica fibers for optical communications, optics has been dominating the long haul communications and it has consistently made its way down to short distance (Fig. 1.3). There are several benefits for replacing conventional electrical cables with optics. Signals in both optical and electrical links are carried by electromagnetic waves. Information in typical electrical wires such as coaxial cables propagates almost at the velocity of light similar to that in optical links as illustrated in Fig 1.4. However, with increased modulation frequencies, the traditional electrical wires are becoming increasingly resistive and the signals moves at a slower rate due to dissipative wave propagation.

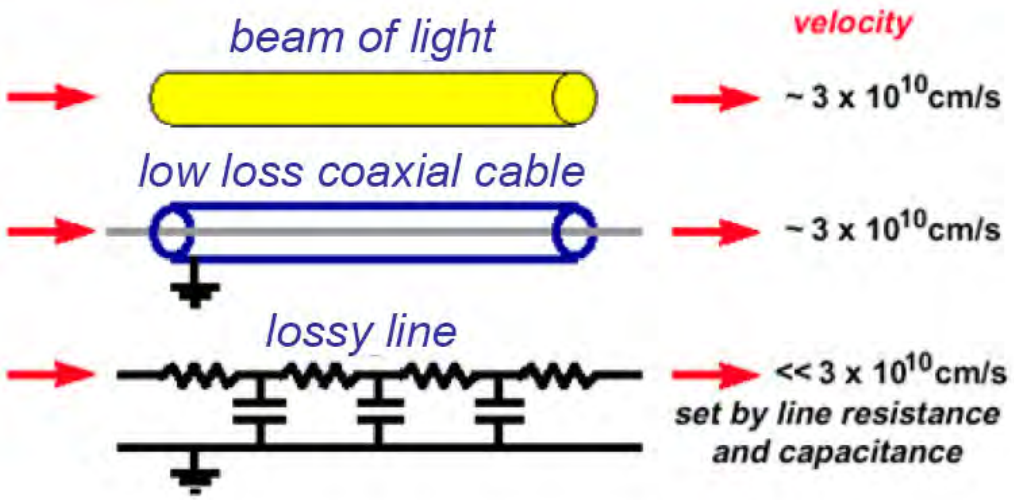

Fig. 1.4 Illustration of types of optical and electrical propagation and their velocities [4].

An excellent review of the potential benefits offered by optical interconnections is presented in [4] based on the fundamental physical differences of the higher frequency, shorter wavelength and larger photon energy of optics compared to electrical interconnections. Optics has negligible propagation loss from large bandwidth signals because the carrier frequency of light is very high compared to any practical modulation frequency. On the other hand, electrical interconnects suffer from significant signal distortion and frequency dependent cross-talk at high modulation

frequencies. Owing to the short optical pulses, optics provide increased time precision over electrical interconnects, and this leads to the ability to transmit multi-channels down a single optical link thanks to wavelength division multiplexing. Furthermore, for optics, it is relatively easy to guide optical wave. The transmitted signal can be confined into the material boundaries of the guiding medium owing to the small waveguide of the optical signals. Additionally, due to the quantum nature of the physical processes, optics does not suffer from the impedance mismatching problem, which is quite challenging for electronics. While electronic devices have high impedance and low capacitance, the communication between such devices rely on low impedance and high capacitance transmission lines. In electronics, line drivers are used to match the impedance, which increase power dissipation and chip area at high operation frequencies. On the other hand, for the optics, the classical field or voltage is irrelevant.

1.2 Thesis Organization

Chapter 2 is a brief introduction to advantages and challenges of Ge material as nanoscale CMOS and optoelectronics. The physical and technological challenges in continued CMOS scaling are outlined. It also introduces the growth mechanism of Ge on Si and two main consequences of the 4.2% lattice mismatch between Ge and Si.

Chapter 3 focuses mainly on the reduction of the surface roughness and threading dislocation density by using selective multiple hydrogen annealing for heteroepitaxy (MHAH). This chapter provides an overview of chemical vapor deposition (CVD) and the epitaxial growth process for the selective area growth. The overlateral growth technique by using MHAH is also introduced for Ge On Insulator (GOI) structure.

Chapter 4 describes abrupt and box shape n^+/p junctions in Ge with high level of activation of n-type dopant, phosphorus (P) using *in-situ* doping during epitaxial growth of Ge.

Chapter 5 reports Ge p-MOSFETs with high-k gate dielectric and metal gate fabricated on selectively growing Ge through patterned SiO_2 on Si. High performance Ge n-MOSFET processing techniques, in particular novel *in-situ* doping Ge growth for raised source/drain, are introduced.

Chapter 6 presents a normal incidence *p-i-n* Ge photodiode by selectively growing Ge on Si using the MHAH technique. Biaxial and uniaxial strain effects of Ge p-i-n photodiodes on Si are investigated through the photocurrent absorption spectrum shift.

Chapter 7 concludes with a brief summary of the key achievements of this dissertation, and briefly discusses future work.

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CHAPTER 2:

Ge: Ideal for Nanoscale CMOS & Optoelectronics

2.1 Introduction

More than three decades scaling down of the device dimension has guaranteed consistent improvement in both device packing density and performance, as shown in Table 2.1. With the scaling of the device dimension, there has been quadrupling of transistor density and a doubling of electrical performance every 2-3 years, drastically lowering cost per function. Together with the scalability, available CMOS technology in Si has played a pivotal role in the success of semiconductor industry.

Parameter	*Constant-field scaling*	*Generalized field scaling*
Physical dimensions, L, W, T_{ox}, wire pitch	$1/\alpha$	$1/\alpha$
Body doping concentration	α	E/α
Voltage	$1/\alpha$	E/α
Circuit density	$1/\alpha^2$	$1/\alpha^2$
Capacitance per circuit	$1/\alpha$	$1/\alpha$
Circuit speed	α	α (goal)
Circuit power	$1/\alpha^2$	E^2/α^2
Power density	1	E^2
Power–delay product (energy per operation)	$1/\alpha^2$	E^2/α^3

Tab le 2.1 Relationships for constant-field scaling and generalized field scaling [1].

Although scaling of the device has provided huge success, it seems to be approaching its limit. Due to the rapidly rising leakage power and short channel effects, improvement on device performance is not as much as before. It is believed that, for the conventional bulk Si device, continued scaling will take the industry down to the 32nm technology node, at the limit of the long-term range of the International Technology Roadmap for Semiconductors (ITRS). The difficulty in scaling the conventional MOSFET makes it prudent to search for alternative device architectures. This will require new structural, material and fabrication technology solutions that are generally compatible with current and forecasted installed Si manufacturing.

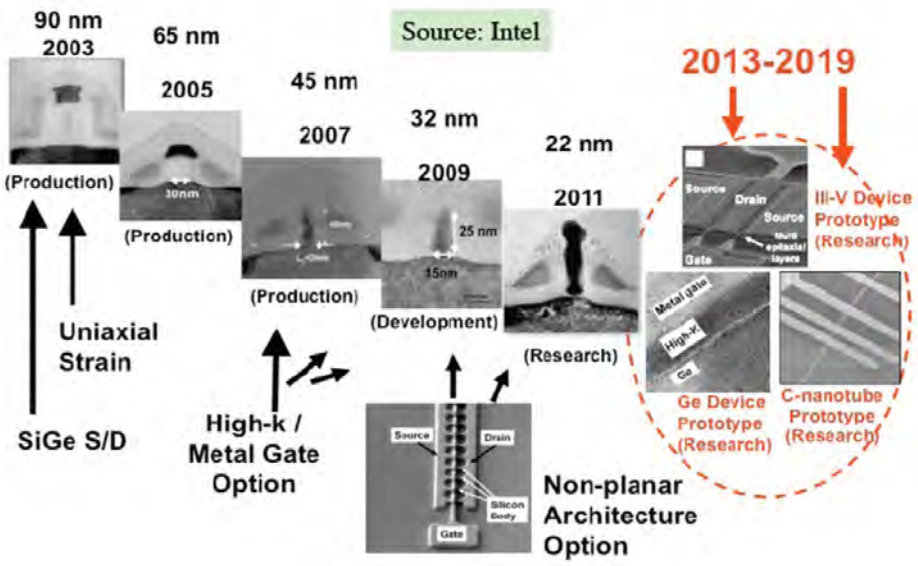

Fig. 2.1 MOSFET transistor scaling (Source: Intel)

2.1.1 Challenges to Scaling Conventional CMOS

In digital applications, MOSFET gate controls the potential barrier between source and drain, enabling the device to operate as a digital switch. The simplest scaling approach is to reduce the dimensions in the horizontal and vertical direction and the supply voltage proportionally so that the electric field at the surface is unchanged (constant electric field scaling) (Table 2.1). However, actual scaling implementations have been based on slightly modified approaches where both the

geometry and supply voltage have been reduced by different factors. Fig. 2.2 shows a schematic of the conventional bulk transistor, identifying the various problems faced in scaling the transistor.

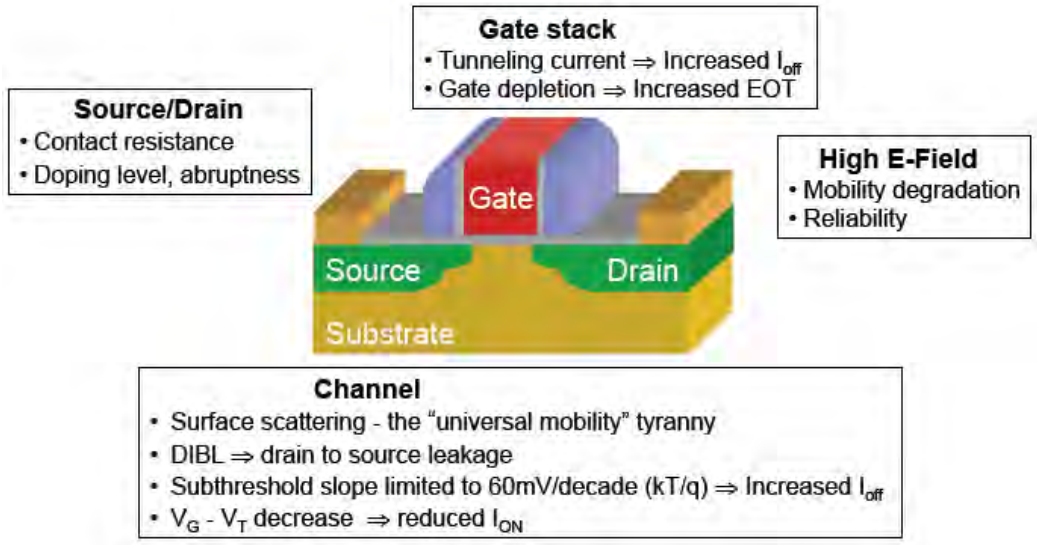

Fig. 2.2 Schematic of the bulk transistor identifying the various problems faced in scaling.

In the conventional bulk MOSFET, gate-controlled charge under the gate region forms conducting channel. Potential barrier between the source and the channel, which controls carrier injection from the source, depends only on the gate bias. In long channel bulk MOSFET, threshold voltage (V_T), at which the device turns ON, is dependent only on the gate voltage and is independent of the drain voltage. However, as the channel length is scaled down, distance between the gate region and the top of the potential barrier shrinks, and electric field lines originated from the drain can easily reach the source side of the channel. As a result, applied drain bias affects the channel potential and reduces the potential barrier between the source and the channel. These are called the short-channel effects (SCE) e. As a result, V_T decreases with the reduced gate length (V_T roll-off) and under high drain voltage. With the reduced V_T and source-side barrier, off-state leakage current increases, and so does the static leakage power.

To maintain gate control over the channel, which is required for acceptable on-off ratio (I_{on}/I_{off} ratio), as the device dimension is scaled down, gate oxide thickness should be reduced as well. As the gate oxide thickness is reduced below 2nm in today's device, quantum mechanical tunneling of carriers through the gate oxide increases exponentially. This leads to the increased leakage power.

Researchers have reported several techniques to arrest the degradation of the MOSFET performance as a switch with scaling:

(1) Source-drain junction depth lowering:

Reducing the source/drain junction depth reduces the drain coupling to the source barrier. However, as the source/drain junction depths get shallow, their doping must be increased so as to keep the sheet resistance constant. The solid solubility of dopants in Si poses an upper limit to the maximum doping that can be achieved. Hence, reducing the junction depths increases the extrinsic resistance leading to a reduced overdrive and hence reduced drive currents.

(2) Channel doping increase:

In modern bulk MOSFETs, the channel doping is tailored to have complicated vertical and lateral profiles so as to minimize the impact of gate length variation on the short channel effects. However, increasing the doping in the channel leads to a decrease in the mobility due to increased impurity scattering. Also, increased channel doping increases the sub-threshold slope leading to higher OFF state current.

(3) Gate oxide thickness reduction:

The gate control of the channel can be improved by increasing the capacitive coupling between the channel and the gate electrode. However, when these oxides become too thin, they begin to conduct current via quantum mechanical tunneling, increasing the leakage current.

2.1.2 Importance of Mobility in Scaled MOSFETs

The drain current in saturation normalized to channel width can be given as $I_{ds}/W=C'_{ox,inv}\cdot(V_{GS}-V_T)\cdot v$, where v is the effective carrier velocity at the virtual source. This virtual source point is located at the top of the potential barrier between the source and the channel, as shown in Fig. 2.3 [2]. Hence for extremely scaled MOSFETs the velocity of the carriers at the source determines the net drive current. By using new materials in the channel, which have lower carrier effective masses in the length direction, the injection velocity in the channel may be increased leading to higher drive currents. Carrier velocities have been increasing primarily because of the reduction of the characteristic length of the potential barrier near the source, as L_G is scaled, and therefore a reduction in the backscattering. Increasing the mobility reduces this backscattering rate, hence providing for higher carrier velocities and hence higher drive currents.

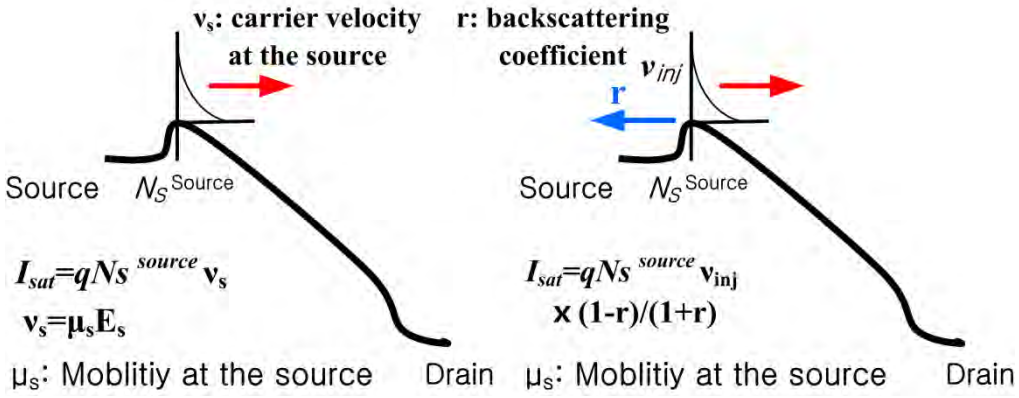

Fig. 2.3 Models used to describe the drive current in nanoscale MOSFETs. The current is proportional to the velocity of the carriers at the source and the backscattering rate, both of which are determined by the low-field mobility.

Hence current flow in ultra-short channel transistors may be described by a small number of scattering events referred to as a quai-ballistic transport model. Fig. 2.3 depicts the factors that dominate current drive in the classical drift model and the quasi-ballistic model respectively. In the drift model, the carrier velocity near the

source region is strongly affected under non-stationary transport by the low-field mobility near the source region, while the injection velocity and the back-scattering rate at the source determine the velocity near the source region in the quasi-ballistic model. Both factors are strongly related to the low-field mobility at the source. As a result, both models predict an increase in the current in nonoscale MOSFETs by increasing the low-field mobility near the source region.

2.1.3 Germanium for Scaled MOSFET

Property	Si	Ge	GaAs	InAs	InSb	GaSb
Electron mobility	1600	3900	9200	40000	77000	6000
Hole mobility	430	1900	400	500	850	1000
Bandgap (eV)	1.12	0.66	1.424	0.36	0.17	0.72
Dielectric constant	11.8	16	12.4	14.8	17.7	15.7

Table 2.2 Carrier mobilities, bandgap energies, and dielectric constants for bulk materials.

As scaling of conventional Si device approaches its limit, novel materials with better electrical properties are being aggressively researched. Possible candidates are Ge and several III-V materials. Among them, Ge shows much promise for novel channel material.

In Si based devices, relatively low hole mobility which limits the pMOS performance has been a problem. Ge shows the highest bulk hole mobility (Table 2.2), and this should ideally correspond to an increase in surface mobility and an ultimate increase in the transistor performance. Electron mobility also shows about 2.5 times increase, compared with Si. Although surface mobility of electron in Ge suffers much from the poor surface scattering, if provided with adequate passivation technique, in nMOS performance can be increased, as well. In addition to the increase in mobility, compared with Si, Ge's more balanced electron and hole mobility values will lead to

more symmetric design for nMOS and pMOS transistors in the CMOS inverter cell, allowing smaller area pMOS devices and easing deign constraints.

It is interesting to compare the two systems of Ge and Si in the ballistic limit. For ultra short channel devices in this limit, an electron travels from source to drain independent of scattering and thus I_{dsat} is no longer governed by V_{sat}. Thus, during scaling, the I_{dsat} limit is governed by the thermal injection velocity(v_{inj}). Fig. 2.4 is a plot of drift velocity versus electric field for various semiconductors.

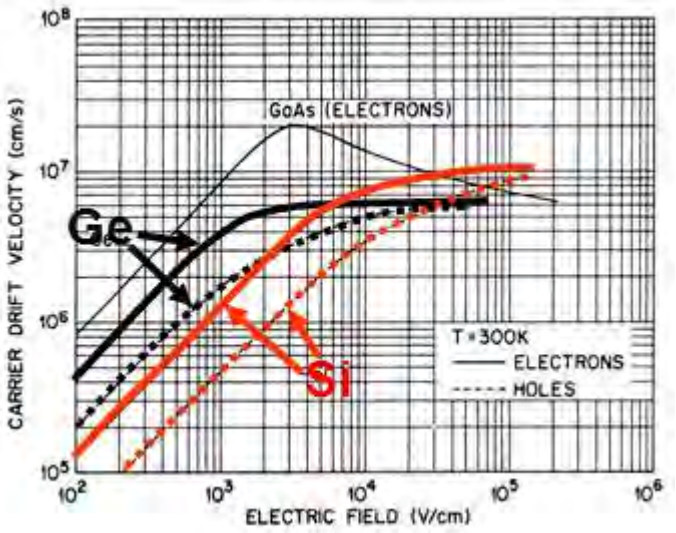

Fig. 2.4 Carrier drift velocity (cm/s) versus electric field (V/cm) [3].

Another advantage of using germanium is its smaller bandgap, being around 0.6eV compared to 1.2eV for Si. Smaller bandgap leads to smaller threshold voltage hence to better V_{DD} scaling, which is a major limitation in the scaling of Si devices. Also, the smaller band gap results in smaller Schottky barrier height, which will lead to smaller contact resistance helping the drive current of MOSFET.

2.1.4 Germanium as an Optical Detector Material

The absorption coefficients vs. photon wavelength for various semiconductors including Silicon are plotted in Fig. 2.5 [4]. Since the low-loss window for telecommunication silica fiber is formed around near infrared region (wavelength of

1300-1500 nm), most optical communication systems use optical signals within this range. As a result, detecting material should show high optical absorption in this region.

Silicon is relatively transparent in this region, due to its high indirect bandgap. Therefore, a suitable detection material that is efficient in the near infrared and simultaneously compatible with Si is vital for realizing low-cost optical interconnects. However, Ge is a strong absorber for the standard telecommunication region. Although Ge is also an indirect bandgap material like Si, relatively small direct bandgap of 0.8 eV (Fig. 2.6) enables efficient signal detection. Furthermore, high carrier mobility of Ge promises fast operation.

In addition to these desirable electrical properties, Ge's compatibility with Si and low temperature processing capability makes it very promising for optical applications.

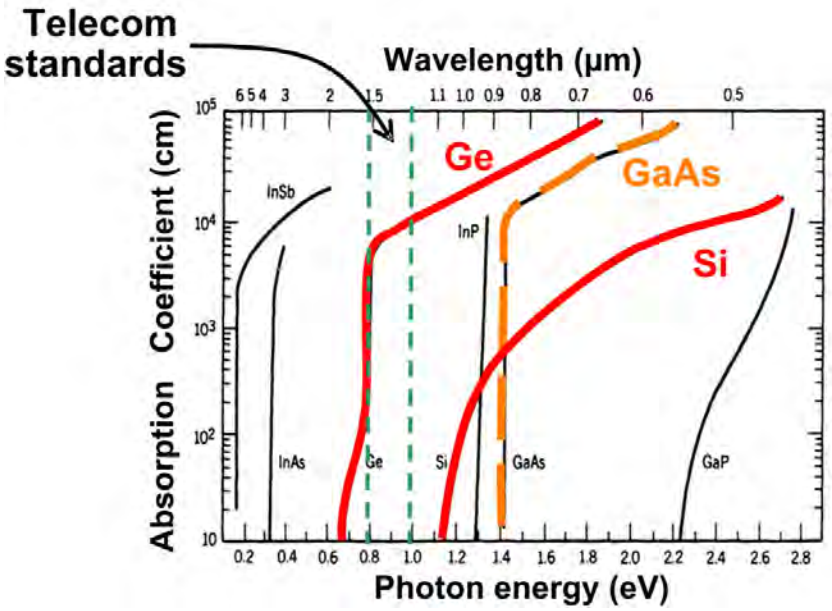

Fig. 2.5 Absorption coefficient for various semiconductors vs. photon energy.

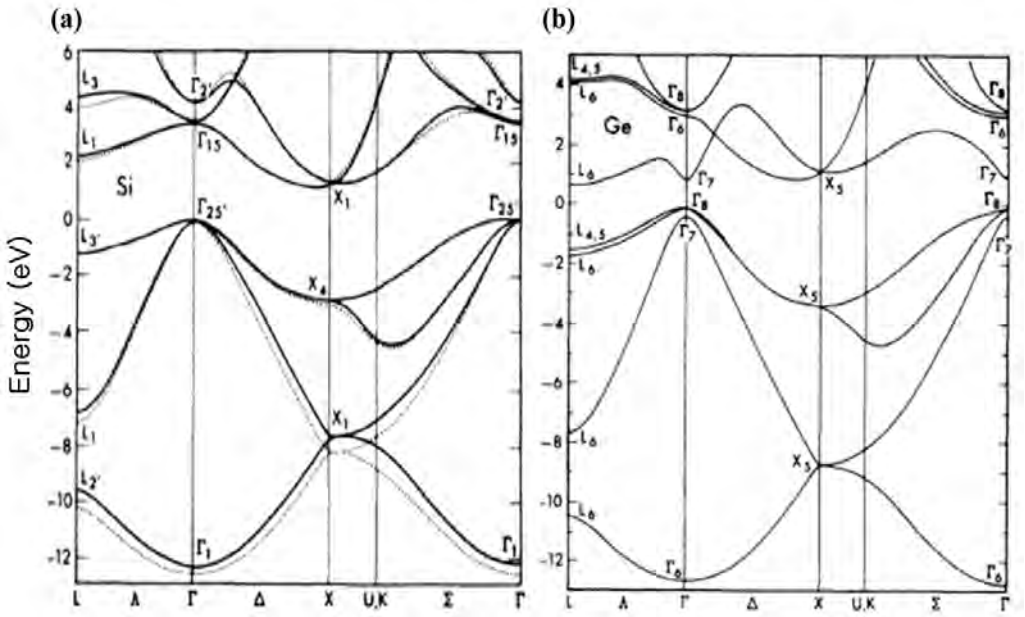

Fig. 2.6 Band structures of (a) Si and (b) Ge [5].

From structural point of view, several device structures have been suggested as photodetectors. Among them are p-i-n photodiodes (PIN), avalanche photodiodes (APD), and metal-semiconductor-metal detectors (MSM). APDs provide high selectivity, owing to impact ionization gain. But, APDs require high applied voltage to initiate the avalanche gaining process, and are relatively slow. Furthermore, APDs suffer from thermal noise, since the noise can also be amplified by the avalanche process. PIN and MSM diodes are relatively fast. But, the top metal electrode which covers some portion of the surface will block the incident light, degrading the detector's sensitivity.

In this work, to demonstrate the absorption efficiency of strained Ge, we fabricated and measured responsivity of PIN photodetectors, which have relatively simple fabrication steps.

2. 2 Challenges of Germanium Growth on Si

2.2.1 Introduction

Though Ge has its advantages over Si, it has some drawbacks, for example, high cost and mechanical weakness compared with Si. Furthermore, today's industry is much concentrated in Si technology. So, to exploit advantages of Ge on Si-based platform, monolithic integration of Ge on Si is needed, and Ge growth technology on Si would be a starting point to the monolithic integration. However, the lattice mismatch between Ge and Si causes much problem in growing Ge on Si.

2.2.2 Lattice Mismatch: Ge/Si

If a material, for example, Si is to be grown on the same material (homo-epitaxy), since lattice constants of the starting material and the epi material are same, high quality layers can be achieved, without incurring significant defects like threading dislocations. Even if the two materials are different (hetero-epitaxy), if they have the same lattice constant, equally high quality epi-layers can be achieved. Growth of GaAs on AlAs and Ge on GaAs are examples for hetero-epitaxial growth with same lattice constants.

Difficulties rise if the lattice constants for the substrate and the epi material are different. If the mismatch is only a few percent and the layer is thin, the epitaxial layer grows with a lattice constant in compliance along the surface plan as its lattice constant adapts to the seed crystal. Such a layer is called pseudomorphic because it is not lattice-matched to the substrate without incurring strain. However, if the epitaxial layer exceeds a critical thickness (t_c), which depends on the lattice mismatch, the strain energy leads to formation of defects called misfit dislocation. In our research, we want to grow high quality germanium layers on silicon. However, germanium's lattice constant is 5.6575 Å whereas silicon's is 5.4307 Å [3]. Thus the percent difference is 4.1763%.

If the mismatch is considerable and relatively thick epi-layer is needed, additional epitaxial growth techniques are needed. As one starts to grow Ge on Si, the new Ge layer will conform to the lattice spacing of the Si substrate. The Ge layer is now

compressively strained as the lattice is reduced. So below a certain thickness, one can grow defect-free compressively strained Ge on Si. This thickness has been shown to be around 4-10 nm. As one continues to grow thicker layers, it is energetically favorable to relieve the strain by forming dislocations at the Ge/Si interface. In addition, the islanding can occur as an additional means of reducing the elastic strain energy of the film [6]. This leads to rough surfaces unsuitable for device applications.

2.2.3 Growth Modes

The growth mechanics are governed by the physics of nucleation and growth processes. Theoretically, equilibrium growth mode is determined by the relative strength of the substrate free energy (σ_s), the interface free energy (σ_i), and the surface free energy of the heteroepitaxially grown layer (σ_f). Although in reality, kinetics and thermodynamics always influence film growth, so growth cannot take place under actual equilibrium conditions, it is useful to consider the ideal limits of the growth for the fundamental material analysis.

There are three known modes of heteroepitaxial growth. These are Frank-Van der Merwe, Volmer-Webe, and Stranski-Krastanov (SK) models [7]. These models loosely explain two dimensional (2-D) layer-by–layer growth, three dimensional (3-D) islanding growth, and layer-by-layer growth followed by islanding growth, respectively.

1. **Layer-by-layer growth:**

   Theoretically, 2-dimensional layer-by-layer growth (Fig. 2.7) is dominant when the inequality $\sigma_s > \sigma_i + \sigma_f$ holds, where the substrate free energy is large enough to suppress the interface free energy and the surface free energy altogether. This growth is observed when the growth rate is low or the substrate temperature is sufficiently high to accommodate atoms diffusion. In this growth mode, adatoms have sufficient mobility to find one another. Nucleated 2-D islands can grow and ultimately fill in the initial starting surface. This growth mode usually shows an increase of surface roughness with increasing layer thickness because

the previously deposited layer is never completely filled before the next layer nucleates.

Fig. 2.7 Schematic illustration of Frankvan de Merwe (layer-by-layer).

2. **Island growth:**

If the substrate free energy is relatively small compared with the interface free energy and the surface free energy ($\sigma_s<\sigma_i+\sigma_f$), then the growth material tends to coalesce by itself on the surface rather than wetting the surface, and opposite to the 2-D layer-by-layer growth, 3-D islanding growth becomes dominant. This type of growth occurs for relatively high deposition rates and slow lateral adatom diffusion. In this growth mode, atoms migrate only on the order of a few lattice sites before they are incorporated into the growing film. Growth under these conditions leads to a rough surface (Fig. 2.8) for which the roughness amplitude increases with increasing film thickness.

Fig. 2.8 Schematic illustration of Volmer-Weber (islanding).

3. **Strnski-Krastanov (SK):**

Somewhat in between the two previously mentioned modes, SK model takes place. For this case, epi-material initially wets the substrate, but because of lattice mismatch, as the layer thickness increases, strain energy contributes to σ_i, to the point at which the film no longer wets the substrate. Subsequently, islands and misfit dislocations are formed to relieve strain. The thickness beyond which the onset of misfit dislocation is favorable is the critical thickness. A smooth surface during deposition will be achieved when deposited atoms have sufficient

time to migrate and incorporate into a step before other atoms are deposited on the surface. The balance of forces will change during the growth if the materials have large lattice mismatch and associated strain. The first few layers will comprise a continuous, smooth film that usually has properties that differ from the bulk. Islanding happens to relieve the misfit strain. The clusters grow in size and density until the islands begin to merge in what is known as a coalescence phenomenon which decreases the island density allowing further nucleation to occur. This continues until a connected network with unfilled channels and voids develops. Finally, the voids are filled and a continuous film results (Fig. 2.9). It has been shown that the condition for SK growth is that the lattice mismatch is between 3% and 7% [8].

Fig. 2.9 . Schematic illustration of Stranski-Krastanov (layer-islanding).

For the epitaxial growth of Ge on Si, since the Ge-Ge bond is weaker than the Si-Si bond, leading to a smaller surface energy, 2-D model is dominant at first. However, high strain is imposed on the grown layer due to the large lattice mismatch between Si and Ge, so after the critical thickness, valleys and hills are formed to relieve the stress. Consequently, the system of Ge/Si is usually discussed as a classical model for the Strainski-Krastanov growth mode. The critical thickness is generally considered to be 4~10 nm. After the formation of one or more monolayers, subsequent layer growth becomes unfavorable and island growth begins to relieve the misfit strain. It has been reported that for pure Ge deposited on Si (001), by the third monolayer, strain energy can no longer be released by 2-D growth, and the growth mode changes from 2-D to 3-D, accompanied with the increased surface roughness. At a later stage, these 3-D structures relax to the Ge lattice constant and produce a high density of misfit dislocations between the substrate/epilayer interface and islands in the epilayers.

2.2.4 Threading Dislocations

For first several nanometers of Ge grown on Si, Ge is forced to have same lattice constant as that of Si, and the resulting layer is defect-free strained Ge layer (Fig. 2.10). As the thickness increases, Ge atoms continually suffer from the stress, and the total strain energy increases linearly with the grown layer thickness. When the layer thickness, thus the strain energy, reaches the critical condition, formation of defects to relieve strain becomes more favorable (Fig. 2.11). These defects are called misfit dislocations and are usually formed at the Ge/Si interface. Critical thickness varies with growth condition, but typically measures between 4~10 nm.

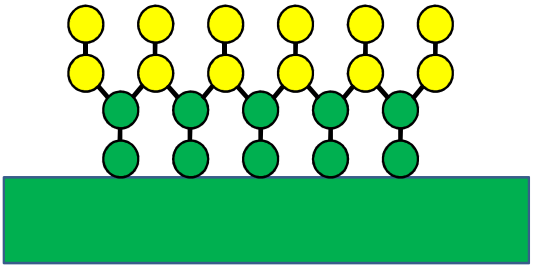

Fig. 2.10 Cross section of germanium on silicon growth; Ge is compressively strained by 4.2% below the critical thickness.

Generally, misfit dislocations are confined at the Si/Ge surface. But, some of the dislocations generated at the interface travel to the surface. These are called threading dislocations. Dislocations have to either form a loop or terminate at a free surface. Since threading dislocations cannot end in crystal, they are left in the layers, and are terminated at the layer surface, the closest free surface to the substrate. They typically thread from the layer substrate interface to the layer surface. Since the devices are built near the surface, threading dislocations near the surface affect device parameters, like carrier mobility and lifetime, and degrade device performance and reliability.

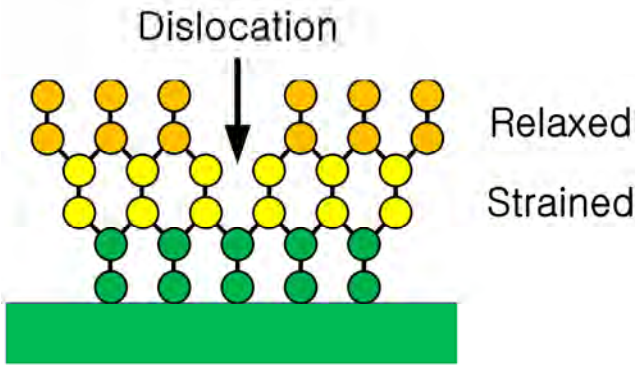

Fig. 2.11 Cross section and atomic view of germanium layer after critical thickness and dislocations have formed.

2.2.5 Literature Review

Historically, many novel ideas and techniques have been introduced to grow high quality Ge layers heteroepitaxially on Si which will lead to the fabrication of efficient optical detectors as well as MOSFET transistors. These previous studies achieved the threading dislocation densities in the range of 10^7-10^9 cm^{-2}. The following summarizes important research publications in this area over the past three decades in an attempt to grow dislocation-free high quality Ge on Si.

1. **Graded buffer layer:** In 1983, Bean and co-workers demonstrated that Ge_xSi_{1-x} layers can be grown on Si substrates over a full range of alloy compositions at temperatures from 400-750^oC by molecular beam epitaxy (MBE) [9]. At a given temperature, films can be grown in a smooth, two-dimensional manner up to a critical germanium fraction, x_c. The growth becomes rough beyond x_c, which, for instance, increases form 0.1 at 750^oC to 1.0 at 550^oC. RBS (Rutherford ion back scattering) and TEM measurements indicate good crystallinity over a wide range of growth conditions and that the lattice mismatch between Ge_xSi_{1-x} and Si layers can be accommodated by elastic lattice distortion rather than misfit dislocation formation. Fitzgerald and co-workers later showed that by growing SiGe relaxed graded buffer layers on Si

at a high temperature, high quality relaxed epilayers with 0-100% Ge can be grown on Si [10-12]. Their idea is to prevent massive dislocation nucleation, interaction and multiplication events that increase threading dislocations. This is done by staying within the low mismatch region with the introduction of each grading layer, which introduces a small number of new dislocations while providing the strain to glide dislocations out of the edge of the substrate.

2. **Superlattice buffer layers:** Luryi and co-workers used superlattice buffer layers to avoid the large lattice mismatch, and demonstrated p-i-n Ge detectors on Si with a quantum efficiency of 40% at 1330 nm [13]. Strained layer superlattices are essentially several low-misfit layers on top of each other. The idea is that strain can act as a barrier to the vertical movement of threading dislocations [14].
3. **Low temperature Si buffer layer:** Several groups have reported that the insertion of a low-temperature MBE grown Si buffer can dramatically reduce the threading dislocation density in the SiGe layer [15-19]. It has been suggested that point defects in a low-temperature Si buffer layer can trap the dislocations [20].
4. **Very high temperature MBE:** Malta and co-workers showed heteroepitaxial growth of Ge on Si by MBE at 900^{o}C. A highly faceted interface results, indicating localized Ge melting and subsequent local alloying with Si [21]. This phenomenon is associated with extensive threading dislocation confinement near the Ge/Si interface. Etch pit density measurements obtained on Ge films that had undergone interfacial melting were as low as 10^5 cm^{-2}.
5. **Cyclic thermal annealing:** A number of groups have reported that in-situ thermal treatment can reduce threading dislocation density in GaAs grown on Si [22-24]. Kimerling and co-workers later showed that heteroepitaxial growth followed by cyclic thermal annealing can also reduce dislocation density in Ge/Si systems [25]. They grew a thin Ge buffer layer followed by thick layer at elevated temperature and subject the film to cyclic thermal treatment. With such technologies, p-i-n detectors have been built on 4μm Ge layers grown on

Si using a low temperature buffer layer, yielding responsivity of 0.89A/W at 1300 nm. Moreover, with this technology, 52% quantum efficiency at 1300 nm was demonstrated on 1 μm Ge films grown on Si [26].

6. **Selective Growth:** Epitaxial growth on patterned substrates has been shown to reduce the overall threading dislocation density. In small misfit systems, growth on small patterns reduces the misfit dislocation density and dislocation interactions and therefore the threading dislocation densities [27, 28]. Growth in small areas also reduces the distance the threading dislocations need to travel before they reach the sides of the epilayer [29, 30]. If the threading dislocations thread to the epilayer surface at a certain direction, it is possible to reduce the dislocation density by blocking threading dislocations using amorphous materials such as SiO_2 and Si_3N_4. Epitaxial necking [31, 32], conformal growth [33], epitaxial lateral overgrowth [34, 35], and pendeo-epitaxy [36] are methods based on this idea.
7. **Strain-relaxed buffered layers:** Using dual strain-relaxed buffer layers, very high 3dB bandwidth up to 38.9 GHz was demonstrated on vertical p-i-n detectors with 300nm intrinsic regions [37]. Thin SiGe buffer layers with different Ge compositions were also used to relieve some of the strain during growth [38].
8. **Nanoscale Ge seeds:** Li and co-workers demonstrated that high quality Ge can be grown on Si covered with a thin layer of chemical SiO_2 [39]. When the oxidized Si substrate is exposed to a Ge molecular beam, 7-nm-wide seed pads form in the oxide layer and touchdown on the underlying Si. Upon continued exposure, Ge selectively grows on the seed pads rather than on SiO_2 and the seeds coalesce to form an epitaxial later overgrowth layer. The Ge epitaxial lateral overgrowth is free of dislocations network, but stacking faults exist near the Ge-SiO_2 interface. A fraction of these stacking faults propagate to the surface, resulting in etch pit density less than $2x10^6$ cm^{-2}. The high quality of Ge epitaxial lateral overgrowth is attributed to a high density of nanoscale Ge seed pads interspaced by 2-12 nm wide SiO_2 patches.

9. **Compliant substrate:** If threading dislocations can thread into the substrate rather than into the epilayer, dislocation-free layers can be obtained. This has been reported by the application of the compliant substrate technology [40, 41]. Several groups have reported epilayers with very low threading dislocation densities by introducing a thin compliant substrate by wafer bonding or by thinning of SOI wafer [41-44].

Recently, a method utilizing multiple steps of growth and annealing in a hydrogen ambient was introduced by Nayfeh et al. [45, 46] to grow high quality Ge on Si with low threading dislocation density. In this technique, a thin Ge film is grown heteroepitaxially on Si and in-situ annealed at higher temperature in an H_2 ambient which reduces the surface roughness by 90% and facilitates stress relief in the first few hundred angstroms. Subsequent Ge growth is homoepitaxy on a virtual Ge lattice with no additional defects forming. From our experiments, we find this method more controllable in addition to shorter annealing times required.

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CHAPTER 3:

Selective Multiple Hydrogen Annealing for Heteroepitaxy (MHAH)

3.1 Introduction

Many of the true breakthroughs in our technology are related to materials and the understanding of their properties. Emergence of new semiconductor materials systems, especially in crystalline form, strongly shapes future photonics and electronics. Today, among such new promising material systems is crystalline silicon-germanium (SiGe) heterostructures. Si is the most abundant element in the earth's crust after oxygen and dominates the microelectronics industry, enjoying decades of capital investment and offers advanced fabrication ability. However, Si is losing thrust in the scaling race as the operational frequencies increase and as electronics is reaching the fundamental physical limits [1]. The idea of bringing high speed optical signals directly to CMOS (Complementary Metal-Oxide-Semiconductor) chips offers opportunities for using light to aid electrical functions in novel ways. This seems increasingly imminent as SiGe based integrated photonics is showing promises to alleviate problems faced by copper wires [2]. Recently, there has been a surge in interest in SiGe based optoelectronics such as SOI waveguides [3, 4], near IR detectors [5-8], and optical modulators [9, 10] integrated on Si. The marriage of microelectronics to high performance photonics requires precise control and process compatibility. It is hence crucial to be able to grow high quality SiGe layers selectively on Si.

In this chapter, we demonstrate the selective Multiple Hydrogen Annealing for Heteroepitaxy (MHAH), a promising approach for the integration of SiGe based

optoelectronics on Si VLSI platform. The selective growth mechanism combined with hydrogen annealing steps yields high quality Ge on Si. This technique yields Ge layers with very low dislocation density and surface roughness as confirmed by TEM (Transmission Electron Miscroscope) analysis, and AFM (Atomic Force Microscope) surface morphology studies. In addition, the combined study of the geometry of the grown layers and the growth rates and conditions, shed light on the mechanisms of the selective Ge growth.

3.2 Selective Ge growth on Si

3.2.1 Ge Selectivity for Monolithic Integration

To employ the advantages of both Ge and Si, we need to apply Ge devices locally on Si platform, which is dominant in current industry. To do so, monolithic integration technique for Ge on Si is needed. Since Ge tends not to grow on SiO_2 under low temperature and low pressure, we used SiO_2 as the window for selective growth.

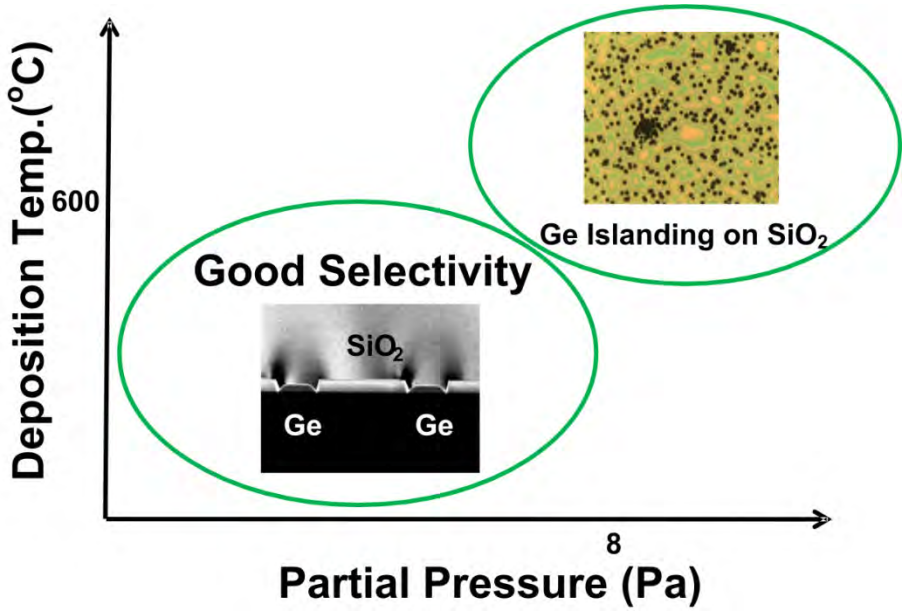

Fig. 3.1 Ge selectivity as a function of growth parameters.

Fig. 3.1 shows Ge selectivity as a function of growth parameters. Using oxide formed by thermal oxidation of Si as the field material, Ge films were epitaxially

deposited using GeH_4 in a H_2 carrier gas. Under growth conditions with low temperature (600°C) and partial pressure (8Pa), good selectivity is obtained, with Ge deposited only on the exposed Si surface and not on the oxide window. However, when either the temperature or pressure is increased, Ge can nucleate more easily on SiO_2 surface, and selectivity tends to be degraded. The reduction in the Ge nucleation density comes at the expense of lower Ge growth rate, and thus a compromise may be needed when choosing the growth condition for Selective Ge growth.

3.2.2 Experiment

A cold wall AMAT Centura epi reduced pressure chemical vapor deposition (RPCVD) reactor is used for Ge heteroepitaxy on Si. Dual load locks feed an exchange chamber through which a robot arm moves wafers between the load lock and the process chamber, avoiding excess oxygen contamination in the reactor chamber. The load lock and the exchange chamber are purged with facility nitrogen. The heating is via two circle lamp arrays, one above and one below a graphite susceptor. Typical depositions are carried out with a rotation rate of 50 revolutions per minute. The base pressure of the RPCVD chamber is 0.5 Torr. The reaction gases used were SiH_4 for Si and GeH_4 for Ge deposition. H_2 was flown into the reactor for controlling the reaction pressure, typically around 30 Torr.

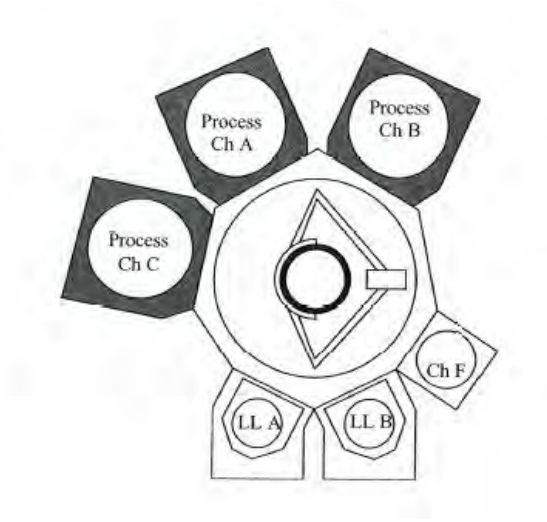

Fig. 3.2 Three Chamber Epi Centura System[AMAT Centura manual]

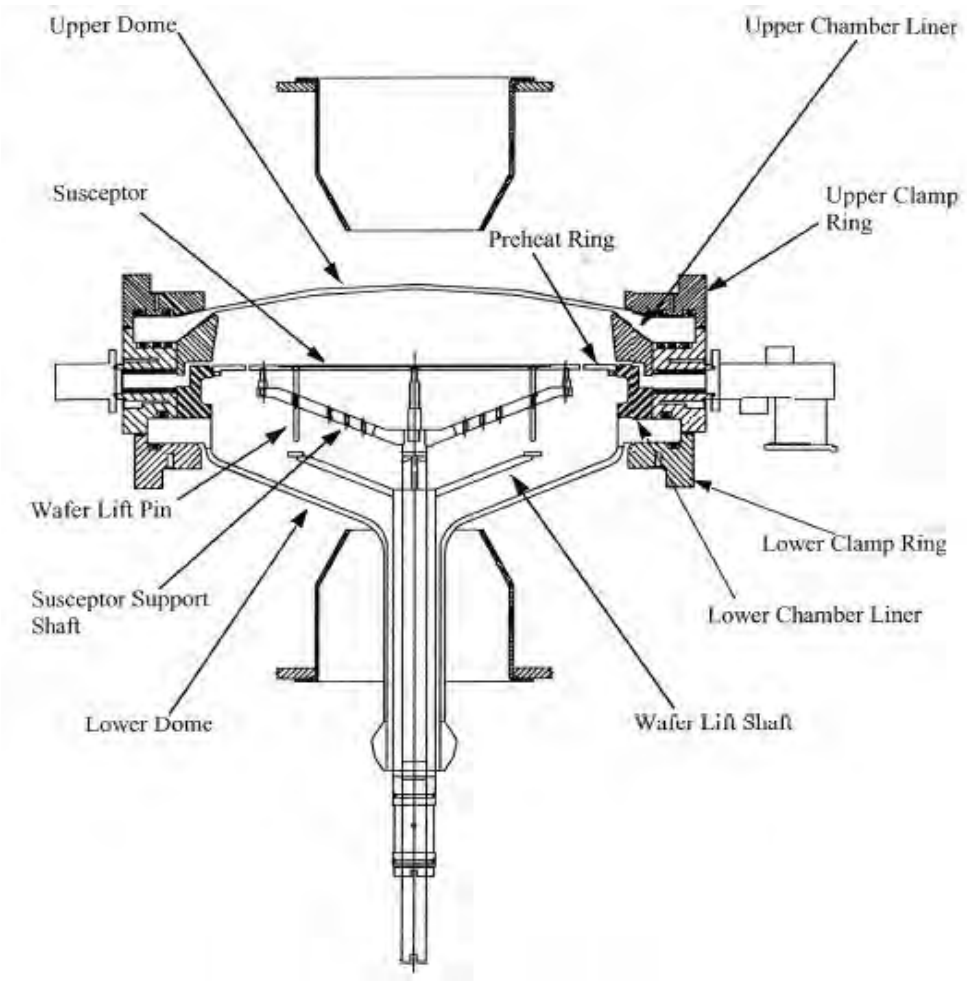

Fig. 3.3 Reduced Pressure Chamber Cross Section[AMAT Centura manual]

In a CVD process, there are seven main steps, as highlighted with numbers in Fig 3.4. The reactants are transported to the deposition region (1) followed by diffusion of reactants from the gas stream through the boundary layer to the wafer surface (2). The reactants are adsorbed on the wafer surface (3). Chemical decomposition and reaction take place on the surface accompanied with surface migration to attachment sites (4). Byproducts are desorbed from the surface (5), and flow to the main gas stream by diffusion (6). Finally, a thermal process is used to force away the byproducts from the deposition region (7).

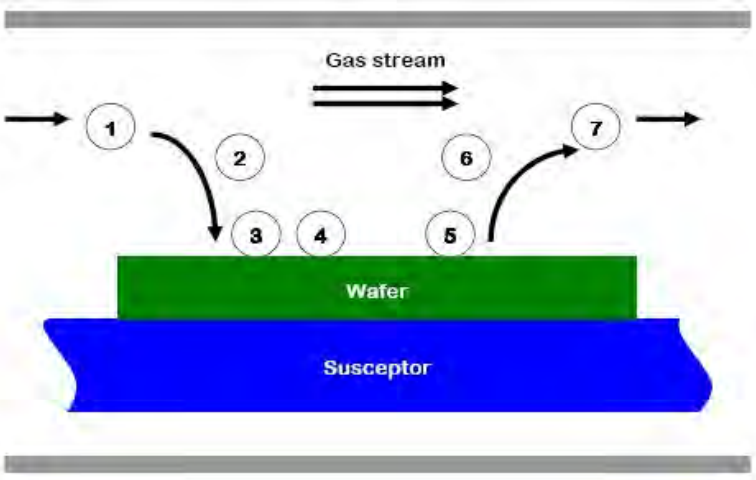

Fig. 3.4 Seven Parts of CVD Process.

Epitaxial growth is a special form of CVD process when the grown film takes the crystal lattice of the underlying substrate. Ideally, the grown substrate will be single crystal provided that the underlying substrate is single crystal. Previous research showed that the Ge grown on Si process is surface reaction limited at temperatures below 450^{o}C and is mass transport limited above 450^{o}C. This has been observed both in rapid thermal chemical deposition systems and in ultra vacuum chemical vapor deposition (UHV/CVD) systems [11, 12]. It has also been reported that at 330^{o}C [13], Ge growth occurs in an SK-related 2-D layer-by-layer mode. The major part of the relaxation process occurs during the deposition of the first two mono layers and the relaxation occurs primarily by the generation of misfit dislocations at the Ge/Si interface. Above 375^{o}C, growth occurs by the 3-D kinetically rough mode, in which islands form and the Ge surface roughness dramatically increase [14]. This is usually accompanied by a high dislocation density, increased leakage current, and degraded device performance. When the temperature increases above 600^{o}C, the step flow growth mode with reduced threading dislocation density and continuous 2-D growth is observed [15, 16].

A 300-nm-thick SiO_2 film was thermally grown on p-type (100) Si substrate at 1000^{o}C. The SiO_2 film was then patterned by a combination of dry-etching followed by wet-etching to define desired locations for Ge growth. The wafer was dipped in

50:1 H_2O:HF for 30 sec and immediately loaded into an Applied Materials Centura epitaxial reactor. A hydrogen bake at 900°C was carried out to ensure no native oxide remained on the Si surface in the patterned SiO_2 windows. In order to increase the film quality, a very thin Si epi-layer was first grown for 90 sec at 700°C with dichlorosilane (DCS) as the reaction species. DCS has good selectivity to SiO_2, which only allows the thin Si layer to be selectively grown on the patterned Si surface. The initial Ge film was grown at 400°C and 8 Pa, yielding a 400-nm-thick film. This was followed by annealing in H_2 ambient for 30 min at 825°C. The growth temperature was increased to 600°C for the last Ge layer. Finally, a 15 min H_2 bake at 750°C completes the process.

3.2.3 Selective Ge Growth Process

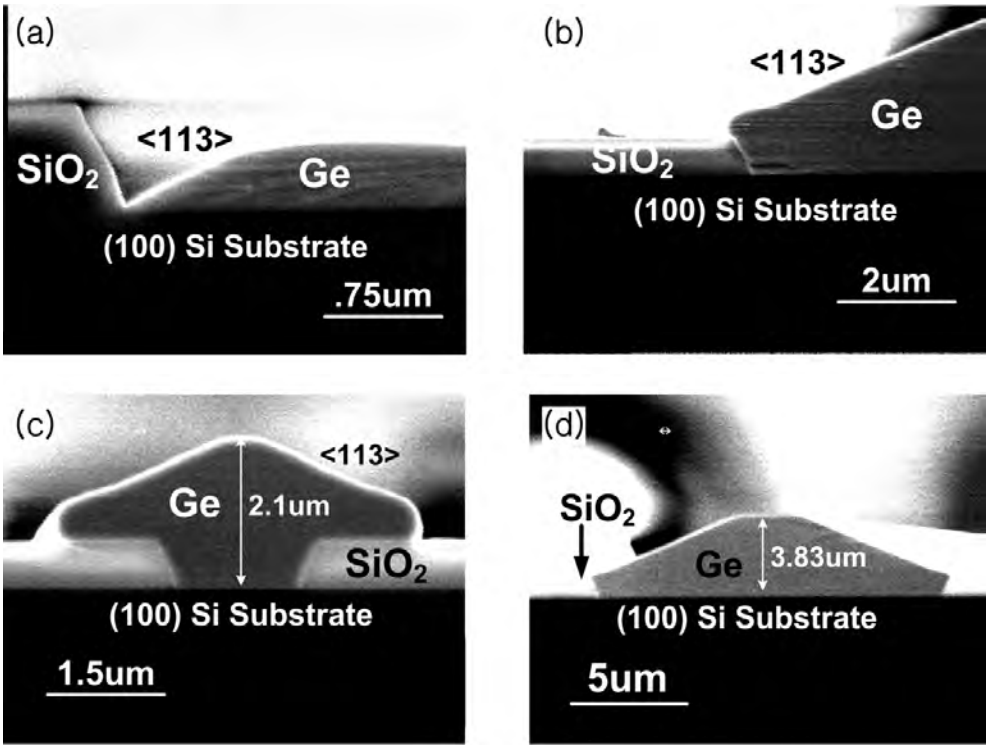

Fig. 3.5 Cross-sectional SEM images in growth temperatures of (a) 400°C and (b) 600°C with SiO_2 windows of 15 µm. SEM images of selectively grown Ge layers in (c) 2 µm and (d) 15 µm SiO_2 windows sizes showing 2.1 µm and 3.83 µm thicknesses of the grown films

The selective growth process is observed by the cross sectional SEM images in Fig 3.5. A cross-sectional SEM image of the sample grown at 400°C in a 15-μm-wide SiO_2 window is shown in Fig 3.5(a). At this temperature, the growth in <100> direction (perpendicular to the wafer surface) (30nm/min) is far more dominant compared to that of <113> direction (3nm/min). The resulting layer has a trapezoidal shape indicating the formation of facets with {113} surfaces. When the growth temperature is raised to 600°C however, significant deposition of {113} facets along with <100> deposition is observed. The calculated growth rates for the 600°C condition are 12 nm/min and 60 nm/min along <113> and <100>, respectively in Fig 3.5(b).

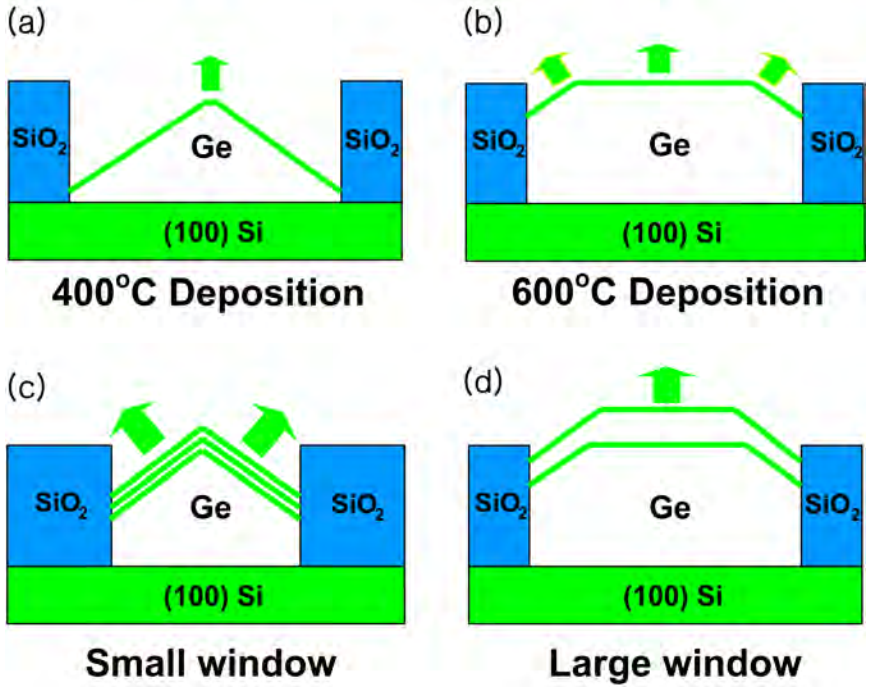

Fig. 3.6 Schematic of selective Ge growth at different deposition condition.

SEM images in Fig 3.5(c) and (d) show that the film thickness at the center of the growth opening is dependent on the size of the opening in the SiO_2 masking layer, keeping other conditions such as temperature and time unchanged. Fig 3.5(c), having a 2μm window size resulted in a thinner layer compared to Fig 3.5(d) which has a

window size of 15μm. We also observe that Fig 3.5(c) shows a pyramid structure while Fig 3.5(d) forms a truncated-pyramid structure.

Fig 3.6 explains this difference. At first, for both cases, <100> directional growth is dominant. For small window case, grown Ge forms pyramid shape soon after, and <100> directional growth cannot take place henceforth. So, <113> directional growth, which is comparatively slow, becomes the dominant growth (Fig 3.6(c)). On the other hand, in large window case, it takes longer time for Ge to form pyramid shape. Until then, <100> directional growth, which is relatively fast, is dominant (Fig 3.6(d)). So, under the same condition, larger window case will produce higher layer thickness.

Table 3.1 Ge growth rate at different orientation.

Deposition Temp	<100>	<311>
400°C	30nm/min	3nm/min
600°C	60nm/min	12nm/min

3.2.4 Selective Multiple Hydrogen annealing for Heteroepitaxy

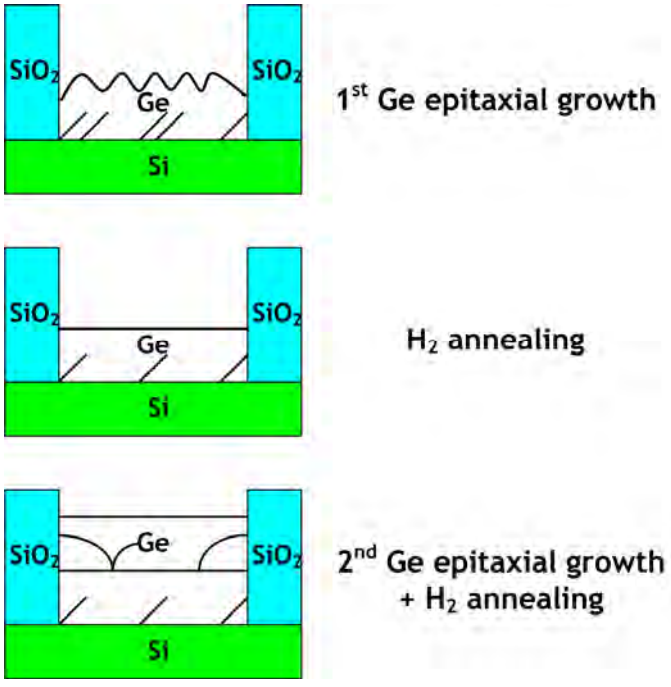

Fig. 3.7 Schematic process flow of the selective MHAH method.

To obtain high quality Ge layer on Si for monolithic integration, MHAH method is applied for selective Ge growth (Fig. 3.7). The initially deposited rough Ge surface due to the lattice mismatch with Si, characterized by islanding, is considerably smoothened by a high temperature hydrogen annealing. On this smooth layer, second epitaxial growth is performed, followed by another hydrogen annealing until desired epi layer thickness is reached. This MHAH procedure is performed on selectively grown Ge on Si through the SiO_2 window for monolithic integration.

3.2.4.1 Surface roughness

Although SiO_2 window provides good selectivity for selective epitaxial growth of Ge on Si, rough surface of resulting Ge layer, characterized by islanding, makes it difficult to fabricate optical and electrical devices on the surface. To get smooth Ge surface, we applied hydrogen annealing. Hydrogen annealing is known to reduce surface roughness of epi-grown layer [17]. Initially rough surface of epi-grown Ge on Si with islanding is smoothened after hydrogen annealing step. Another layer of Ge is grown epitaxially after the first annealing step, and the second annealing step is followed. This cycle is repeated until the desired epi layer thickness is reached.

Table 3.2 Optimum Ge growth condition.

	1st	2nd	3rd	4th
Temp. (°C)	400	400	600	600
Partial Pressure (Pa)	8	8	8	8

We found the optimized growth and annealing condition which minimizes resulting Ge surface roughness. At the same time, to maintain good selectivity for SiO_2 window, process temperature and partial pressure should remain below 600 ^oC and 8 Pa, respectively. Table 3.2 shows the optimum condition for each cycle.

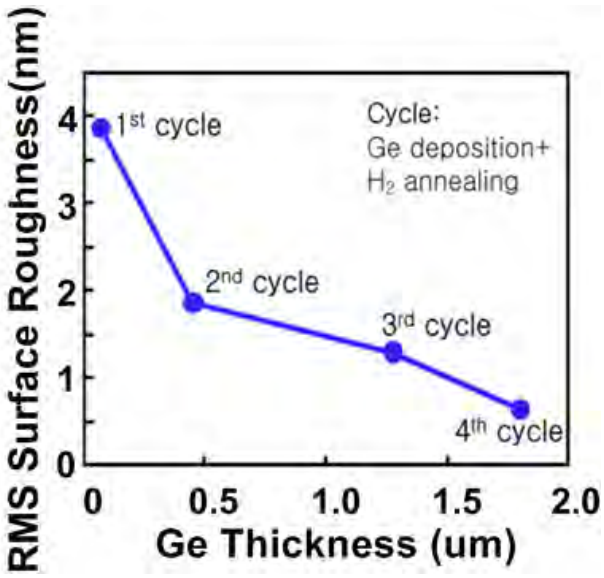

Fig. 3.8 RMS surface roughness as a function of Ge Growth thickness.

Atomic force microscopy (AFM) is used to extract the surface roughness of the films. Fig 3.8 shows the resulting surface roughness after each cycle. In each cycle, epitaxial growth of Ge is followed by hydrogen annealing. As-grown films without hydrogen annealing exhibit ~9.5nm rms surface roughness. After annealing, surface roughness is reduced 3.9nm. These results are in good agreement with the suggested surface roughness reduction model explained by Nayfeh et al [17], which attribute the roughness reduction to hydrogen-mediated Ge diffusion and the reconstruction of the surface. After each cycle, surface roughness is reduced. The hydrogen annealing is especially critical for the first layer of Ge as this will provide a smooth template for subsequent growth. After 4^{th} cycle, surface roughness reaches 0.61 nm, which is the lowest value ever reported for selective heteroepitaxial growth of Ge on Si

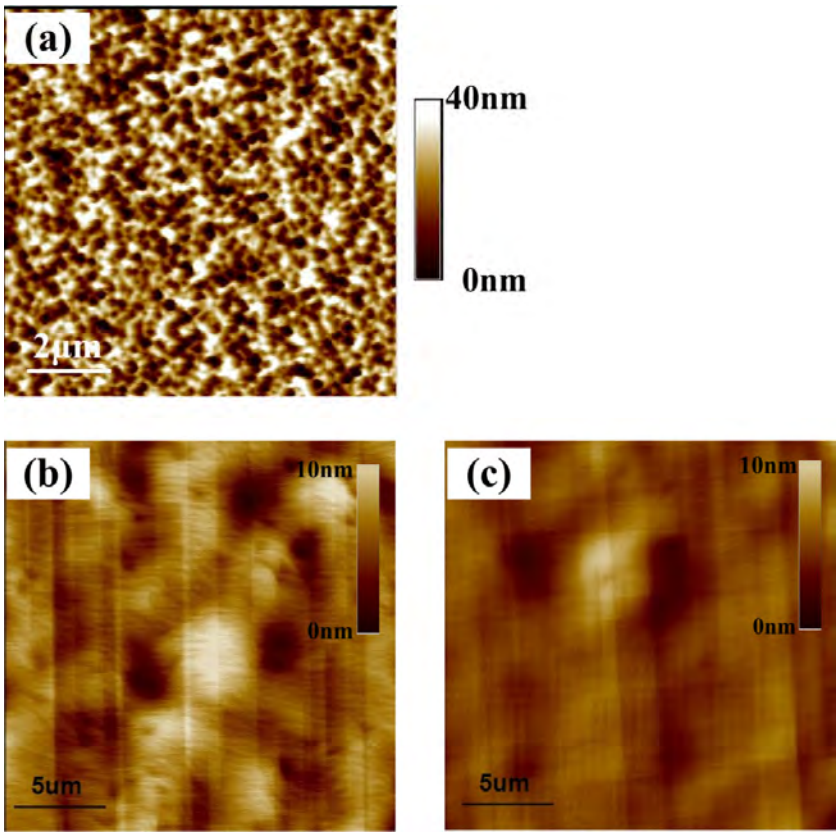

Fig. 3.9 Tapping mode AFM images of (a) as-grown Ge layer, (b) bulk Ge growth, and (c) selective Ge growth after MHAH.

The surface morphology of the grown Ge layers was studied by AFM as shown in Fig 3.9. AFM scan of the as-grown layer is shown in Fig 3.9(a) and after MHAH (Fig 3.9(b) and (c)), respectively. Large surface roughness (9.5 nm rms) and dislocation density is observed on as-grown samples, due to 4.2% lattice mismatch between Si and Ge crystal systems. The surface roughness was reduced significantly after annealing in hydrogen ambient at 825^{o}C. This is attributed to increased surface mobility of Ge species with temperature and the hydrogen ambient protecting the surface from oxidation which would otherwise hinder the mobility of Ge atoms [17]. The surface roughness reduction can be explained in terms of the Ge diffusion barrier as compared to the Ge–H cluster. The effect of attaching H to Ge reduces the diffusion barrier and increases the surface mobility by increasing the local density of states (LDOS) at the Fermi level. However, there appears to be an upper limit to the amount of diffusion barrier reduction. We can estimate diffusion barrier height which is

proportional to *kT* from basic diffusion kinetics. In the case of Ge it occurs around 800 °C which corresponds to 92 meV reduction of barrier height

Fig 3.9(b) and (c) show the AFM images of Ge layers grown on blank Si substrate and selectively in a 50 μm wide SiO_2 window, respectively. In both cases, the first and the second layers are grown at 400°C with an intermediate hydrogen annealing step and the third layer is grown at 600°C. Due to this hydrogen annealing step the surface roughness decreases significantly, 0.45nm (rms) for bulk growth and 0.6nm (rms) for selective growth. AFM images can be used to estimate threading dislocation densities owing to their influence on the surface morphology [18, 19]. The pit density count of bulk grown Ge film is 1×10^7 cm^{-2} while selectively grown layer is 2×10^6 cm^{-2}. The lower pit density indicates a significantly reduced threading dislocation density in selectively grown layers compared to the bulk grown layers [19].

3.2.4.2 Threading Dislocation

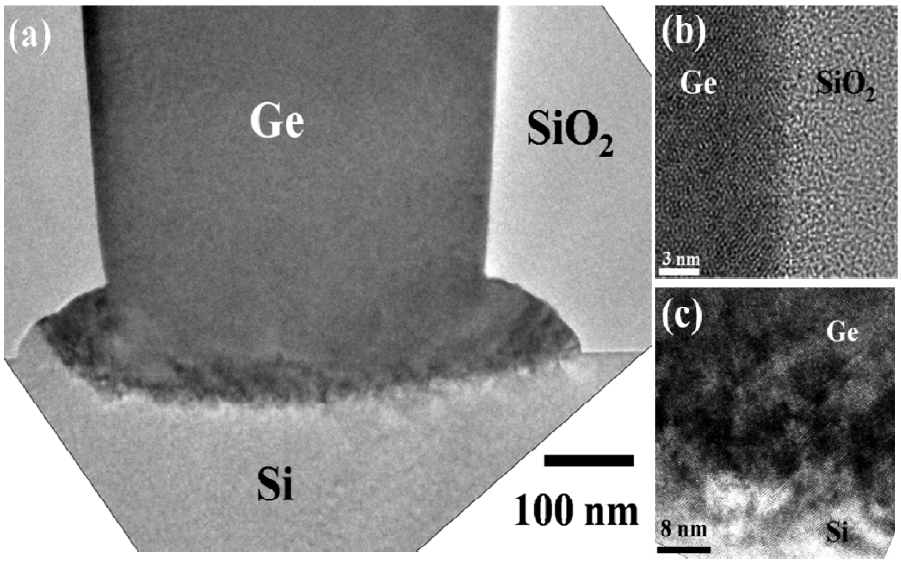

Fig. 3.10 (a) Cross-sectional TEM image of epi-Ge layer by using selective MHAH technique. (b) High resolution image at the interface between Ge layer and SiO_2 side wall. (c) High resolution image at the interface between Ge layer and Si substrate.

To better understand Ge crystal defects originating from 4.2% lattice mismatch between Si and Ge in selectively SiO_2 windows, cross-sectional TEM analysis is carried out. High resolution TEM images in Fig 3.10 show high quality Ge films grown selectively on patterned SiO_2/Si. The width of SiO_2 window is 500nm. Defects can be found only in the first 60-nm-thick region from the Ge and Si interface. Previous efforts to obtain high quality (relaxed) epi-Ge layers on Si required a 500nm or thicker buffer layers to confine the defects and dislocations [20, 21]. In our case, since the initial Ge layer with defects can be as thin as 60nm, growing a high quality epi-Ge layer with much smaller overall thickness will be possible. Most importantly, no threading dislocations inside the Ge are observed above the 60 nm defect layer. Threading dislocations are difficult to be completely eliminated for depositing Ge layer on Si even with selective area growth [20, 21]. Therefore, our high quality epi-Ge layer grown selectively by MHAH method is an important achievement on Ge and Si heteroepitaxy. The mechanism of defect reduction is believed to be similar to the Kimerling's thermal-cycling method [21]. The SiO_2 side walls are used as dislocation sinks. The high temperature hydrogen annealing process is effective on moving Ge atoms, which is also powerful on improving surface roughness of Ge. This rearrangement of Ge atoms will lead dislocations to glide to the Ge and SiO_2 interface and be annihilated. High resolution cross-section TEM picture at the Ge and SiO_2 interface is shown in Fig 3.10(b). The Ge layer near the interface is perfect without any defects.

3.2.4.3 Biaxial Strain

Micro-Raman spectroscopy has been employed to evaluate the in-plane strain in the Ge film. Fig 3.11 shows the Raman spectra of the selectively grown and bulk grown Ge layers. It can be clearly seen that the peak intensity due to Ge-Ge optical phonon mode appears at 301.54 for bulk grown and 301.28 cm^{-1} for selectively grown Ge. For comparison, we have included the Raman spectra from a bulk Ge substrate, where the optical peak appears at 302.12 cm^{-1}. The in-plane tensile strain component in the Ge film is calculated from the strain versus phonon peak shift relationship [22,

23]. The residual strain in the selectively grown Ge is 0.141% while that of the bulk grown Ge is 0.204%. The extracted tensile strains in both cases arise from difference in thermal expansion coefficient between Ge and Si. During the cooling stage after Ge deposition, the decrease in lattice constant of Ge is suppressed by that of Si generating residual tensile strain in Ge layer [24, 25]. The lower tensile strain value in the selectively grown Ge compared to bulk grown Ge can be explained by the Ge confinement by SiO_2 which has compressive strain.

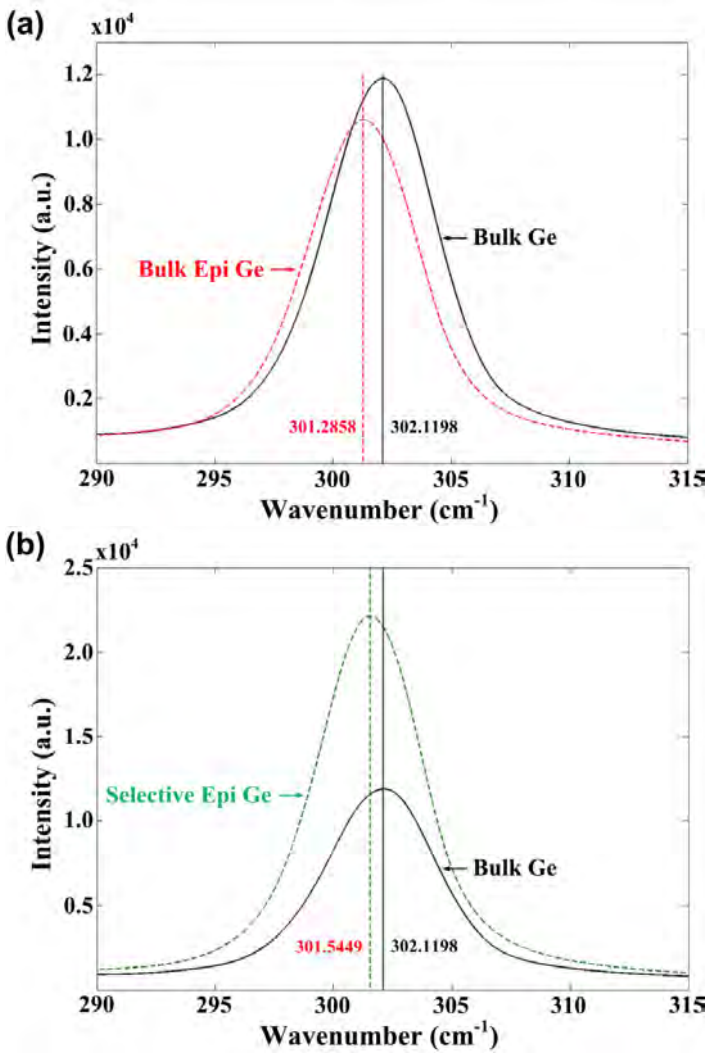

Fig. 3.11 Raman spectra of (a) bulk Ge growth and (b) selective Ge growth on (100) Si substrate. The tensile strain of (a) is 0.204% while that of (b) is 0.141%.

3.3 Over-lateral Growth for GOI

3.3.1. Over-lateral Growth Process

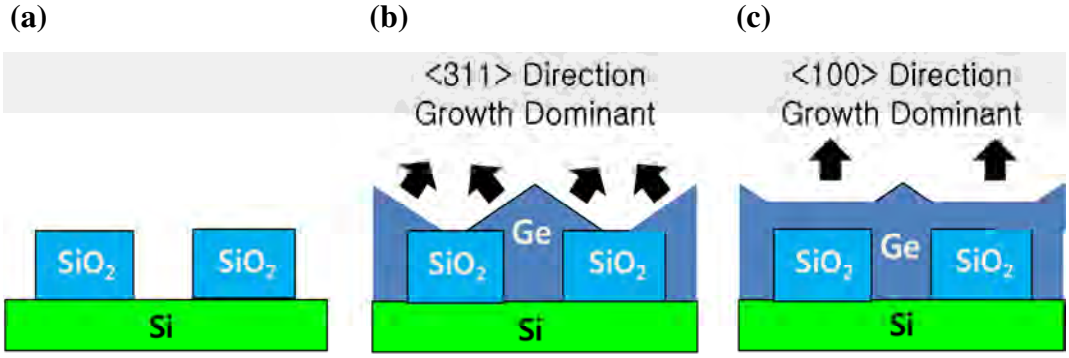

Fig. 3.12 Schematic of the over-lateral growth process; (a) SiO_2 window, Ge over-lateral growth (b) before, and (c) after coalescence.

Fig. 3.12 shows the schematic of the over-lateral Ge growth process. As shown in Fig. 3.12(a), Ge layer is grown only on Si, using the selectivity between the Si and SiO_2. Once Ge layer becomes pyramid-like shape in the SiO_2 trench, <311> direction growth becomes dominant before coalescence (Fig. 3.12(b)). After the coalescence happens, <100> direction growth starts at the valley where two Ge growth fronts meet. Due to a higher growth rate of <100> direction compared to that of <311> direction, the valley is quickly filled up and <100> growth is dominant (Fig.3.12(c)). Therefore, Ge on insulator structure is achieved by using over-lateral growth.

Fig. 3.13 shows cross-sectional SEM images at different growth temperature conditions. At 400^{o}C growth temperature condition, <100> direction growth doesn't start at the valley where two Ge growth fronts meet as shown in Fig. 3.13 (a). However, after the two Ge growth fronts meet, growth temperature is raised to 600^{o}C, where the valley is filled up due to fast <100> directional growth. Fig. 3.13 (b) shows the Ge over-lateral growth with the combined 400^{o}C and 600^{o}C growth temperature conditions. Before the coalescence, Ge layer is grown through the SiO_2 trench at 400^{o}C growth temperature. Once the two Ge growth fronts meet at the middle of the SiO_2 wall, the valley is quickly filled up at 600^{o}C growth temperature. Therefore, GOI structure is achieved.

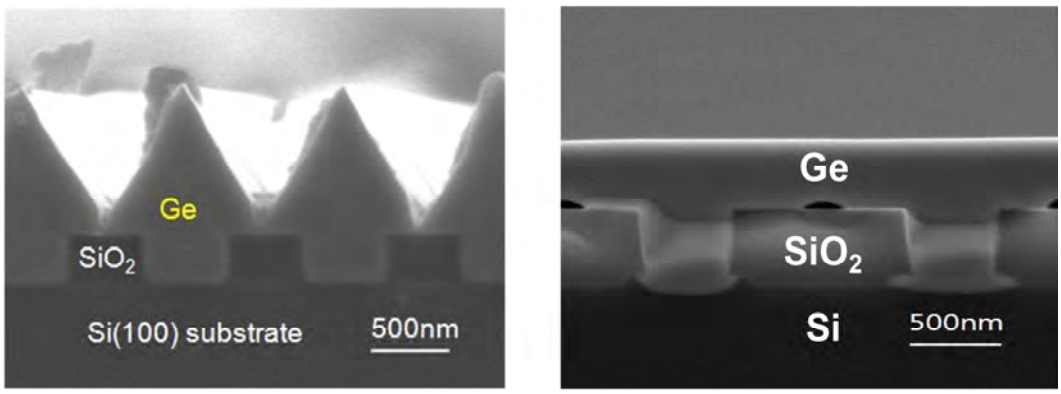

Fig. 3.13 Cross-sectional SEM images in growth temperatures of (a) 400°C and (b) 400°C and 600°C.

With the reduction of the oxide sidewall width, coalescence and subsequent initiation of <100> growth occur more quickly. Thus the total thickness of the Ge growth over the oxide sidewall depends upon the sidewall width; with wider oxide sidewall, it takes longer for the Ge layers to coalesce before <100> growth dominates, which makes the overgrown Ge layer to be thinner.

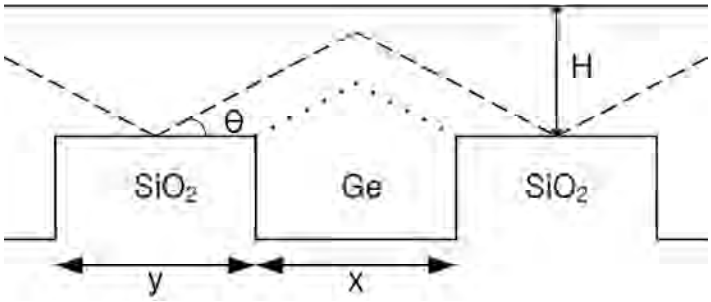

Fig. 3.14 Schematic of Ge over-lateral growth model showing time evolution.

Figure 3.14 shows the schematic diagram for the Ge growth on Si through SiO_2 window. At first, regardless of the height of the window, Ge fills the SiO_2 window, forming triangular shape at the top (dotted line). After the window is filled, Ge continues to grow on <311> direction with growth rate v_1, until the SiO_2 surface is fully covered by the two Ge areas from both sides of the SiO_2 wall (dashed line). When the SiO_2 is fully covered with Ge, then it also grows on <100> direction with

growth rate v_2, which is typically four times the v_1. Ignoring the void formed at the middle of the SiO_2 wall, achievable minimum flat Ge layer thickness can be calculated.

If time Δt is required to achieve flat Ge layer after the SiO_2 wall is fully covered, then

$$\frac{1}{2}(x+y)\cdot\tan\theta + \frac{v_1}{\cos\Theta}\cdot\Delta t = v_2\cdot\Delta t$$

$$\Delta t = \frac{\frac{1}{2}(x+y)\cdot\tan\theta}{v_2 - \frac{v_1}{\cos\theta}}$$

and, minimum achievable thickness H can be expressed as:

$$\mathbf{H} = \Delta t\cdot v_2 = \frac{\frac{1}{2}(x+y)\cdot\tan\theta}{v_2 - \frac{v_1}{\cos\theta}}\cdot v_2$$

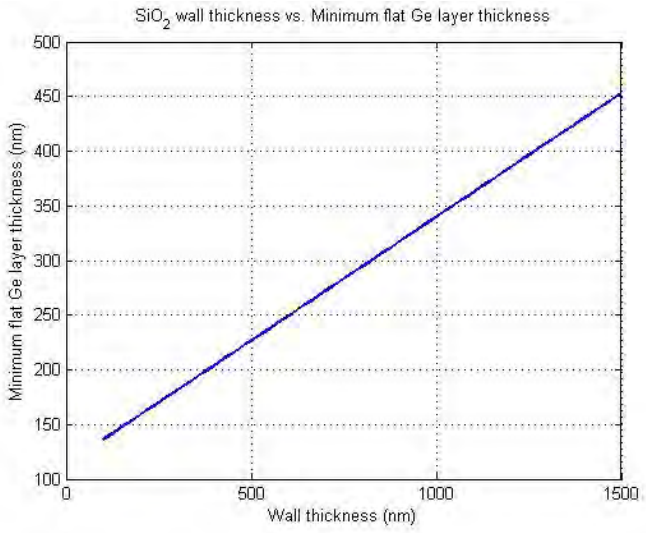

Fig. 3.15 The minimum flat Ge layer thickness on SiO_2 sidewall vs. SiO_2 sidewall width (Si window width (x): 500 nm).

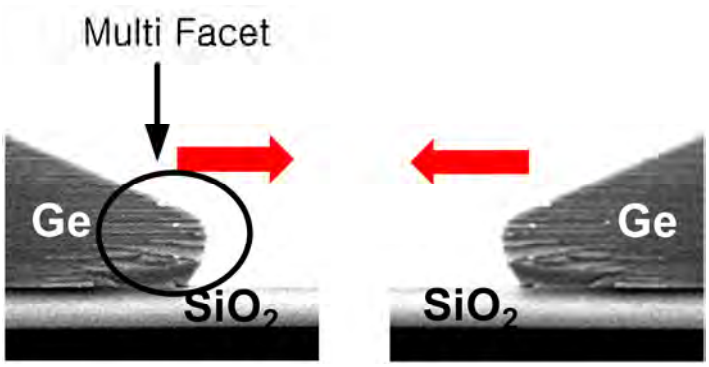

Fig. 3.16 Cross-sectional SEM image of Ge layer on SiO_2 window.

We note here the void at the middle of the oxide sidewall. The importance of the role of high-energy interface between Ge and SiO_2 is observed in the formation of a void upon the coalescence of Ge over the oxide sidewall [26, 27]. The overgrown Ge layer is multifaceted near the oxide sidewall, as indicated in Fig. 3.16. This minimizes the contact area with SiO_2. As a result, as the Ge layers coalesce, a void is formed at the middle of the oxide sidewall.

3.3.2 Threading Dislocation

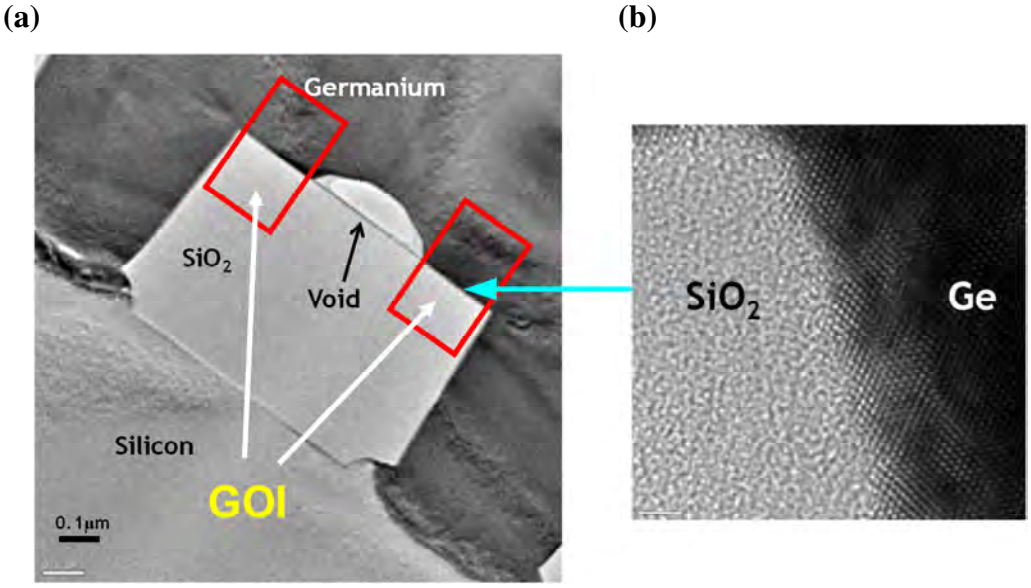

Fig. 3.17 (a) Cross-sectional TEM image of over-lateral Ge layer by using MHAH technique. (b) High resolution image of Ge layer on SiO_2 side wall.

To obtain high quality Ge layer on SiO_2 sidewall, MHAH technique is applied on Ge over-lateral growth. To better understand Ge crystal defects over SiO_2 windows, cross-sectional TEM analysis is carried out. High resolution TEM image (Fig 3.17 (b)) shows the high quality of Ge films grown on the oxide window. The width of SiO_2 window is 1 μm. As explained in section 3.2, the threading dislocation density due to the 4.2% lattice mismatch between Si and Ge can be reduced by using both dislocation trapping in SiO_2 trench and MHAH mechanism. Therefore, very high quality Ge layer can be obtained on the SiO_2 window as shown in Fig. 3.17(b). The Ge layer on SiO_2 window has threading dislocation density count of ~4×10^6 cm^{-2} based on the plan view TEM.

3.3.3 Surface Roughness

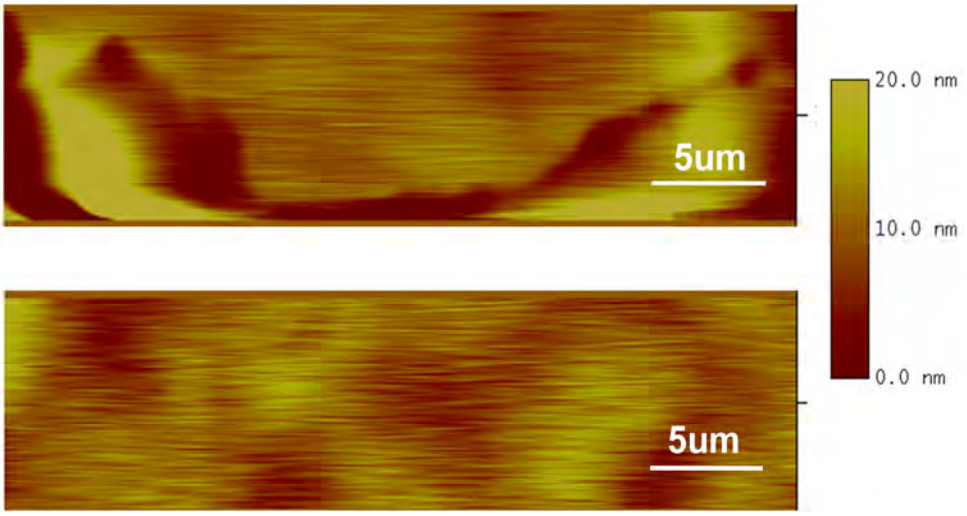

Fig. 3.18 Tapping mode AFM images of over-lateral grown Ge layer (a) without MHAH, and (b) with MHAH technique.

The surface morphology of the over-lateral grown Ge layers was studied by AFM as shown in Fig 3.18. AFM scan of the over-lateral grown sample without MHAH is shown in Fig 3.18(a) and after MHAH (Fig 3.18(b)), respectively. Large surface roughness (rms: 3.5 nm) is observed on as-over-lateral-grown samples. The surface roughness was reduced significantly after MHAH technique with annealing in

hydrogen ambient at 825°C. As explained in Section 3.2, the surface roughness reduction can be explained in terms of the Ge diffusion barrier as compared to the Ge-H cluster. The effect of attaching H to Ge reduced the diffusion barrier and increases the surface mobility in the overlateral Ge growth [17].

3.4 Conclusion

High quality Ge can be selectively grown on Si by MHAH through a SiO_2 masking pattern. Two different growth kinetics were observed at 400°C and 600°C, resulting from relative growth rate difference in <113> and <100> directions. The hydrogen annealing and the selective growth can be used to reduce the dislocation density and the surface roughness. The defect free Ge growth on the small window of SiO_2 was also demonstrated. In addition, tensile strain is observed due to the difference in thermal expansion coefficient.

Over-lateral Ge growth on SiO_2 window was suggested for GOI structure. By applying MHAH technique, high quality Ge layer on SiO2 window was observed. The hydrogen annealing and over-lateral growth can attribute the reduction of threading dislocation density and surface roughness.

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CHAPTER 4:

Germanium in-situ doped epitaxial growth on Si for high performance n+/p junction diode

4.1 Introduction

As scaling silicon MOSFET for higher performance is approaching fundamental limits, germanium (Ge) has appeared to be an attractive material because of its higher carrier mobility compared to Si. Since p-type dopants in Ge could be activated below 400^{o}C with minimum redistribution, mobility enhanced p-channel Ge MOSFET has not been an issue [1,2,3]. On the contrary, relatively low n-type dopant solubility [4,5] and fast n-type dopant diffusion [6] during activation in Ge make it difficult to fabricate source and drain (S/D) in n-channel Ge MOSFETS.

Normally ion implantation with post annealing has been used to form shallow junctions for MOSFET applications. However, in fabricating shallow junctions, the challenge is to minimize the redistribution of dopants during the post annealing since the ion implantation damage results in fast diffusion especially for n-type dopants in Ge [7,8]. Recently, the laser annealing method has been investigated for Ge *n*+/*p* junction due to its short annealing time to prevent diffusion [9]. In order to avoid Transient Enhanced Diffusion (TED), channeling effects, and extended defect formation, solid- or gas-phase diffusion techniques are also very attractive alternatives to form shallow junctions without any damage. However, because solid-source diffusion (SSD) technique requires high temperature annealing (>800^{o}C) for n-type dopant diffusion, the shallow *n*+/*p* junction formation in Ge would be more challenging [10]. In addition to these techniques, in-situ doping of Ge has recently gained interest due to the potential to form an ultra shallow junctions with high level

of dopant activation without any ion implantation damage and subsequent dopant deactivation [11-15].

In this chapter, we demonstrate an abrupt and box shape n^+/p junction in Ge with a high level of activation of n-type dopant, phosphorus (P) using *in-situ* doping during epitaxial growth of Ge.

4.2 Experiment

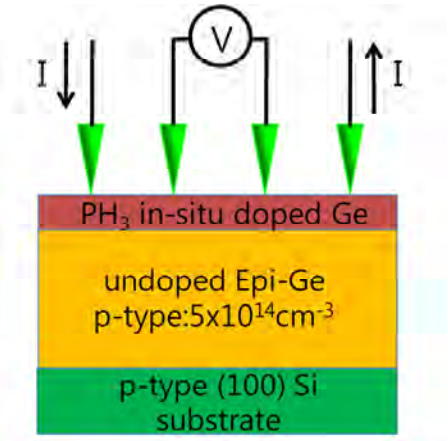

Fig. 4.1 Schematic cross section of n+/p junction for resistivity measurement.

P-type (100) Si wafer was cleaned according to the standard Si wafer cleaning process and immediately loaded into an Applied Materials Centura RP-CVD epitaxial reactor. A hydrogen bake at 900°C was carried out to ensure no native oxide remains on the Si surface. An initial Ge film was grown at 400°C and 8 Pa, yielding a 400-nm-thick film. This was followed by annealing in H_2 ambient for 30 min at 825°C. The growth temperature was increased to 600°C at 8 Pa for the second Ge layer. Subsequently, a 15 min H_2 bake at 750°C completed the intrinsic Ge epitaxial growth process. This intrinsic Ge epitaxial layer showed p-type $4x10^{15}cm^{-3}$ of electrically activated doping concentration. Before in-situ doped layer growth, the dopant gas base line was purged with diluted 1% phosphine to avoid the dopant cross- contamination during the stabilization step. Finally, an *in-situ* doped n-type Ge layer with diluted 1% phosphine doping was grown at 400°C~600°C and 8Pa on the intrinsic Ge layer for 1min to form n^+/p junction.

A four-point probe method was used to measure the sheet resistance R_S (Ω/square) of n-type in-situ doped Ge layers. Fig 4.1 shows the schematic cross section of n+/p junction for four-point probe measurement. Knowing the film thickness W, it was then easy to determine their resisitivity ($\rho=R_s \cdot W$) and, at least in the case of Ge, their ionized dopant concentration.

Mesa diode structures with 200μm in diameter were patterned by HBr/Cl_2 reactive ion etching (RIE) of 1μm of Ge layer in depth followed by a 20 nm thick SiO_2 layer deposition for surface passivation. Windows for the contacts were then patterned on the oxide and etched in HF, followed by metal deposition using electron-beam metal evaporation and photoresist lift-off. About 25nm of Ti was used as contact material, topped with ~45 nm of Au. Therefore, n+/p junction diode was achieved.

4.3 Result and Discussion

4.3.1 Resistivity vs. Flow Ratio

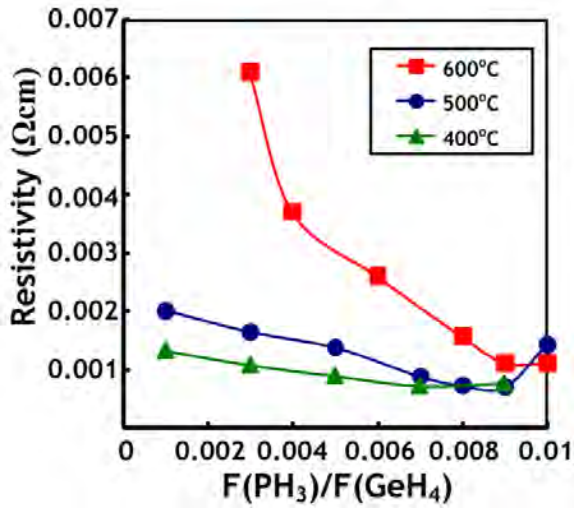

Fig. 4.2 Resistivity for phosphorus-doped Ge layer as a function of the $F(PH_3)/F(GeH_4)$ mass-flow ratio after 10min *in-situ* doped P layer growth

Fig. 4.2 shows the resistivity of P-doped Ge layers grown at different temperatures on the intrinsic Ge epitaxial layer for 10min, measured by four-point probe technique. This sheet resistance is a measure of electrical activation. The resistivity of grown P-doped Ge layer decreases monotonously until reaching a minimum value and finally increases due to the formation of poly-crystalline Ge as the $F(PH_3)/F(GeH_4)$ mass-flow ratio increases. We also measured the P doped Ge layer growth rate at different growth temperatures as a function of $F(PH_3)/F(GeH_4)$ mass-flow ratio. The growth rate is relatively independent of the mass-flow ratio, and mainly depends on the growth temperature. Measured growth rates are 65, 53.5, and 43nm/min at the growth temperature of 600, 500, and 400 ^{o}C, respectively.

4.3.2 SIMS and SRP Analysis

Figure 4.3 shows the depth profiles of P-doped Ge layers grown at temperatures of 400 ~ 600^{o}C for 1min to form *n+/p* junctions. Both secondary ion mass spectrometry (SIMS) and spreading resistance profiling (SRP) data are presented. Fig 4.3 (d) shows both SIMS and SRP data of the conventional ion implantation sample P (P^{31}, 18keV, and $4x10^{15}$ cm^{-2}) in intrinsic Ge layer with post RTA annealing at 600^{o}C for 1 min for comparison. As the deposition temperature increases, deeper phosphorus diffusion was observed. Phosphorus diffused into the intrinsic Ge grown layer up to 35nm due to 600^{o}C *in-situ* deposition for 1 min (Fig. 4.3 (a)) from the initial interface. However, at lower temperatures ($\leq$500^{o}C), diffusion was within 15nm and 10nm for 500^{o}C and 400^{o}C, respectively (Fig. 4.3(b) and (c)).

The electrical concentration profiles are also shown in Fig. 4.3 at different deposition temperatures. At 600^{o}C growth temperature, the resultant n^{+}/p junction has a junction depth of 97nm and a peak electrically activated concentration of $2x10^{19}$ cm^{-3} (Fig. 4.3 (a)). Shallower junction depth of 97nm is obtained, compared to the ion implanted sample (122nm) annealed at 600^{o}C for 1min. This *in-situ* doped profile also exhibits an abrupt edge near the n^{+}/p junction from SRP data yielding a slope for the decay of the phosphorus concentration of 13 nm/decade. Steeper profile is observed at 600 ^{o}C *in-situ* doping than the ion implanted sample (24 nm/decade) as shown in Fig.

4.3 (a) and (d). SIMS and SRP data confirm ~100% dopant activation without any post annealing step after 600°C 1min *in-situ* doped Ge layer growth (Fig. 4.3 (a)). The peak electrically active concentration decreases as the growth temperature decreases because lower temperature condition does not have enough thermal energy to activate the high level of dopants during 1min deposition.

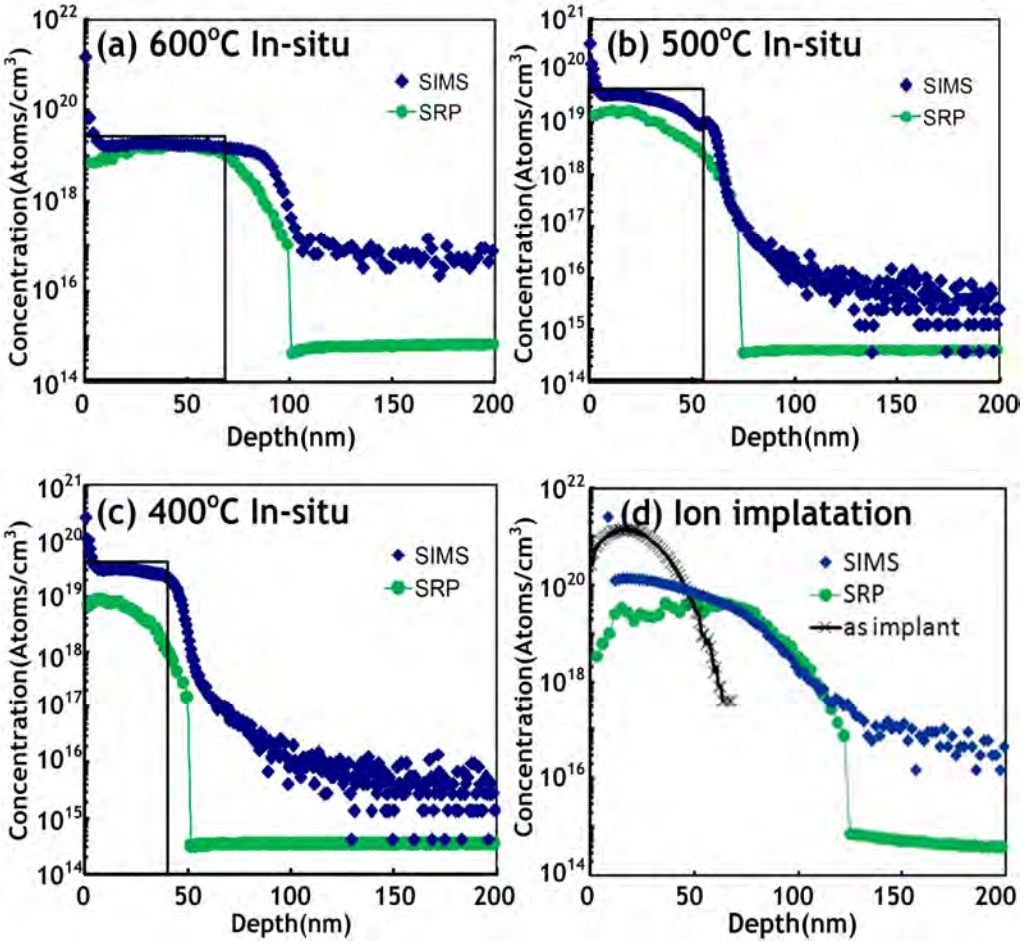

Fig. 4.3 SIMS and SRP depth profiles of P in (a) 600 °C, (b) 500 °C, and (c) 400 °C *in-situ* doped Ge layer growth for 1min (the box indicates the *in-situ* layer thickness), and (d) ion implanted Ge (P^{31}, 18keV, and $4x10^{15}$ cm^{-2}) after 600 °C/1min RTA.

4.3.3 In-Situ Doped Growth Model

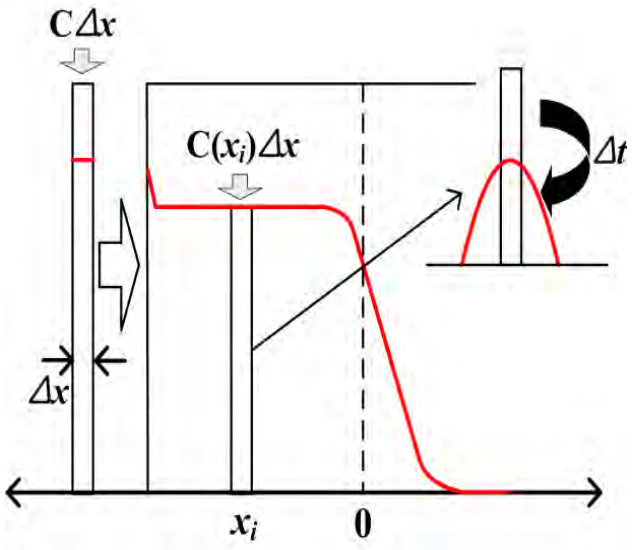

Fig. 4.4 Schematic of in-situ growth model.

To explain the shape of the resulting in-situ doping concentration, we developed a phenomenological model for in-situ doping process. During the in-situ doping process, dopants are provided at the growing surface, and at the same time, diffuse into the substrate. Since the epi-layer, at the top of which the dopants are provided, itself also grows with time, simple error-function like profile cannot be applied here. To model this properly, the process is divided into discrete cycles. Each cycle is composed of growth phase and diffusion phase. During the growth phase, highly doped thin Ge layer of thickness Δx is deposited on the top of the surface. Dopants are diffused during the diffusion phase, to get the new doping profile after short time interval Δt. This one cycle models in-situ doping growth and dopant diffusion during the short time interval Δt, so growth thickness Δx should be $v \cdot \Delta t$, where v is the growth rate of Ge (nm/sec).

To model the dopant diffusion during the time interval Δt, first, we divide the Ge substrate into very thin layers. If the thickness of the layer is thin enough, then the doping profile in each layer can be considered as a delta function. Since delta function

like profile diffuses over time to form a Gaussian diffused profile, each layer will form a Gaussian profile after Δt. So, adding all the Gaussian profiles gives the doping profile after Δt.

Figure 4.4 shows the schematic of in-situ doped growth model. (n-1) layers of Ge with thickness Δx have already been deposited. Doping profile at this point is defined as $C_{n-1}(k \cdot \Delta x)$, where subscript (n-1) denotes the number of deposited layers. To get the doping profile after short time interval Δt, first, n_{th} layer of Ge doped with C_0 is deposited on top. Then, diffusion step takes place.

$$C_n(k \cdot \Delta x) = \sum_{l=-\infty}^{n} \frac{C_{n-1}(1 \cdot \Delta x)}{\sqrt{4\pi \cdot D \cdot \Delta t}} \exp\left(-\frac{((k-1) \cdot \Delta x)^2}{4 \cdot D \cdot \Delta t}\right)$$

This cycle is iterated until the desired in-situ doped Ge layer thickness X is reached, which means, n reaches $X/\Delta x$.

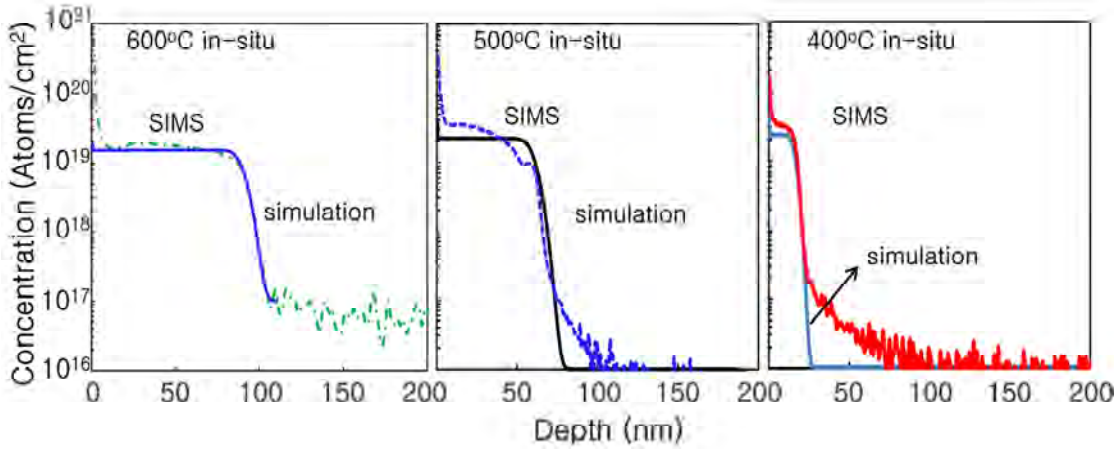

Fig. 4.5 SIMS and simulation depth profiles of P in (a) 600 °C, (b) 500 °C, and (c) 400 °C *in-situ* doped Ge layer growth.

Figure 4.5 shows the depth profiles of P-doped Ge layers grown at temperatures of 400 ~ 600°C. Both SIMS and simulation data are presented. We could extract Phosphorus diffusivity for different temperatures (400°C, 500°C, and 600°C) by fitting simulation results to the measured data. Under 600°C in-situ doping condition,

resulting diffusivity of 2×10^{-15} cm^2/sec reasonably matches with diffusivity for 650°C from previous study [16]. As expected, as we lower the temperature, diffusivity decreases. For 500 °C, extracted diffusivity is 1×10^{-15} cm^2/sec, and for 400°C, 6×10^{-16} cm^2/sec. There is no previous work available as a reference for diffusivity of phosphorus in Ge for temperature below 650°C.

4.3.4 n+/p Junction Diode

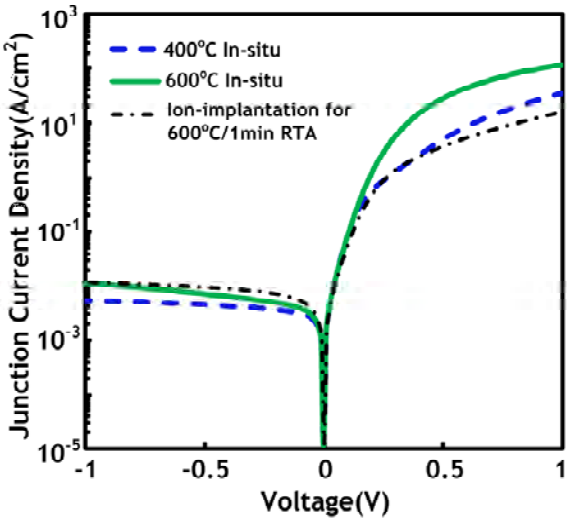

Fig. 4.6 Junction current density of n^+/p junction diodes using 1min *in-situ* doping and ion implantation with 600 °C/1min RTA.

In Fig. 4.6, the n^+/p junction diode formed by *in situ* doping process at 600°C shows a better diode characteristic, with $1.1\text{x}10^4$ on/off ratio and high forward current density (120A/cm^2 at 1V) than the conventional junction diode fabricated by using ion-implantation and 1min post RTA annealing ($1.37\text{x}10^3$ on/off ratio and 15A/cm^2 forward current density at 1V). The ideality factors of three n+/p junction diodes were extracted. At low forward bias, the ideality factors are found to be around 1. This means that the diffusion current component is dominant at the low forward bias due to the small band gap of Ge. Also the ideality factor increases as the forward bias increases. The shallower and more abrupt junction in 600°C in-situ sample with

~100% dopant activation provide higher forward current than the ion-implanted sample even though it has lower peak electrically active dopant ($2x10^{19}$ cm^{-3}) than ion implanted sample ($5x10^{19}$ cm^{-3}). This result confirms 600°C *in-situ* doped diode sample has high performance without damage such as TED, defect formation, etc. To the best of our knowledge, this is one of highest forward current density and on/off ratio [17-19]. Even at the lower growth temperature (400°C), the in-situ doped samples shows higher forward current (33.8 A/cm^2) and higher on/off current ratio ($6.47x10^3$). Table 4.1 summarizes various characteristics of the *in-situ* and ion-implanted n+/p junction diodes.

	Abruptness (nm/decade)	Junction depth(nm)	Activation (%)	Diffusivity (cm^2/sec)
600°C *in-situ*	13	100	100	$2x10^{-15}$
500°C *in-situ*	8	75	65	$1x10^{-15}$
400°C *in-situ*	7	35	30	$6x10^{-16}$
Ion Implantation	24	122	50	-

Table 4.1 Result of n-type in-situ doped Ge growth.

4.4 Conclusion

We have examined temperature dependence associated with abrupt *n+/p* junction formation and the activation of n-type dopant (P) in Ge. The abrupt and box shape junctions (less than 100nm) with high level activation of P are accomplished using *in-situ* doping technique at 400^{o}C-600^{o}C growth temperatures. This process will be feasible for making ultra shallow junctions. In addition, we have fabricated high performance Ge n^{+}/p junction diodes with excellent characteristics having $1.1x10^{4}$ on/off current ratio and high forward current density (120 A/cm^{2} at 1V).

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CHAPTER 5:

High Performance Germanium CMOS Technology

5.1 Introduction

Over several decades, device scaling has brought increase in performance and reduction in cost per function, and this propelled the success of semiconductor industry, though, basic design (bulk MOS transistor) and material (Si) have not been changed much. Recently, as Si bulk CMOS devices approach their scaling limits, new device structures and novel materials are being aggressively studied. Higher carrier mobilitiy, especially hole mobility, of Ge makes it a decent candidate for the channel material. Moreover, monolithic integration of Ge with Si devices is expected to provide an alternative solution for system-on-chip applications. Though relatively poor surface passivation so far tends to limit the performance of the Ge devices, very promising results for Ge p-MOSFETs with both high-k dielectric and GeO_xN_y dielectric have been demonstrated, with 2x hole mobility enhancement over Si for bulk devices and 4X for strained Ge FETs [1-4].

In order to integrate Ge devices on Si platform for high performance applications, it is critical to develop new methods for heteroepitaxial Ge growth technology. This is a challenging task, since the lattice constant mismatch between Si and Ge makes it difficult to get high-quality single Ge layer growth on Si. Since the quality of the Ge layer is critical to the performance of the Ge device built on it, numerous researches have been done on the heteroepitaxial growth technique. For example, employing super lattice buffer layers to grow Ge layers effectively reduces the large lattice mismatch between Si and Ge [9]. Cyclic thermal annealing and Hydrogen annealing are other methods of heteroexpitaxial growth [10, 11]. Also, molecular beam epitaxy

(MBE) method is yet another instance of Ge growth on Si, which creates thin strain-relaxed buffers on silicon substrate [13]. Also, Heteroepitaxy necking method by selective growth of Ge in SiO_2 trenches on Si has been thoroughly studied [14, 15]. These high-quality Ge layers on Si can be used to fabricate germanium-on-insulator (GOI) substrate. Very good transport properties for GOI p-MOSFETs have been already reported [4, 5, 6].

On the other hand, poor performance of Ge n-channel device poses much difficulty for the Ge CMOS technology. In addition to the poor surface passivation which limits the carrier mobility, relatively low solid solubility [5, 6], and fast diffusion during dopant activation [7] of n-type dopants make it difficult to fabricate source and drain regions in n-channel MOSFETs. Therefore, there is a relatively small process window to achieve both a stable gate stack and a well-activated n+ S/D.

In this chapter, we demonstrate Ge p-MOSFETs with high-k and metal gate and by selectively growing Ge through patterned SiO_2 on Si. We also demonstrate a promising approach for high performance Ge n-MOSFET processing techniques, in particular novel *in-situ* doping Ge growth for raised source/drain.

5.2 Gate stack Development

Compared to Si, Ge surface has much higher density of interface states, typically around 10^{14} $cm^{-2}eV^{-1}$, which causes faster recombination velocity and short carrier lifetime. When fabricated, this limits the performance of the resulting devices. Hence, gate stack for the Ge devices should provide decent passivation, which is critical to increase the performance of the device, in addition to desirable high permittivity (k). Traditionally, high-k materials experimented on Si have been investigated on Ge surfaces

5.2.1 Characterization of the MOS interface

The quality of the surface is often characterized by fixed charge density and interface trap density , D_{it}, determination. The fixed charge, which causes the flat band voltage (V_{FB}) shift in C-V measurements across the gate stack, is the sheet charge at

the interface. Since the change in V_{FB} is directly related to the fixed charge density, it can be determined by measuring the amount of shift. Interface trap density, which denotes the density of traps within the bandgap of the semiconductor is characterized by two important techniques, the quasi-static method and the conductance method. In this work, the conductance method was used to measure the interface trap density.

5.2.1.1 Low Frequency (quasi-static) Method

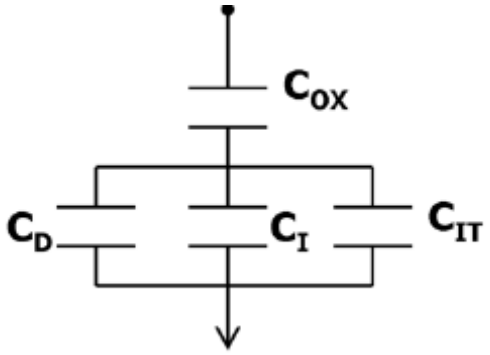

Fig. 5.1 Equivalent circuit for MOS C-V at low frequency. C_D: the depletion capacitance, C_I: the inversion capacitance, and C_{IT}: the capacitance associated with interface states .

The low frequency quasi-static measurement is the most common method to estimate the interface state density. This employs the C-V characteristics across the gate stack. High and low frequency measurements are performed to extract the capacitance due to the interface states, and from that, interface state density is calculated. For low frequency (LF) measurement, performed typically at a few Hz, interface states have enough time to capture and release electrons. So, interface states can contribute to the measured C-V characteristics. For high frequency (HF) measurement, frequency is high to an extent that interface states cannot follow the applied ac signal, so these states cannot contribute to the resulting C-V characteristics. For Si/SiO_2 interfaces, a high frequency ac modulation at 1MHz is used. The difference in the C-V characteristics between the LF and the HF measurements is used to determine the C_{IT} (Fig. 5.1) and hence determine the trap density distribution within the band gap of the semiconductor.

(C_{lf}: low frequency capacitance, Chf: high frequency capacitance, C_{ox}: oxide capacitance, C_s: semiconductor capacitance, C_{IT}: interface trap capacitance)

$$\frac{1}{C_{lf}} = (\frac{1}{C_{ox}} + \frac{1}{C_s + C_{IT}})^{-1}$$

$$\frac{1}{C_{lf}} = (\frac{1}{C_{hf}} + \frac{1}{C_{ox}})^{-1}$$

$$C_{IT} = (\frac{1}{C_{lf}} - \frac{1}{C_{ox}})^{-1} - (\frac{1}{C_{hf}} - \frac{1}{C_{ox}})^{-1}$$

Letting $\Delta C = C_{lf} - C_{hf}$, the interface state density is calculated as:

$$D_{it} = \frac{\Delta C}{q}(1 - \frac{C_{hf} + \Delta C}{C_{ox}})^{-1}(1 - \frac{C_{hf}}{C_{ox}})^{-1}$$

Using the above equation, interface state density can be extracted from measured quantities. To determine the location of the Fermi level at the interface, surface band banding should be calculated. Charge neutrality condition gives:

$$C_{ox} dV_G = [C_{ox} + C_{IT}(\psi_s) + C_s(\psi_s)] d\psi_s$$

Solving the equation gives:

$$\psi_s = \psi_{so} + \int_{V_{Go}}^{V_o} dV_G \frac{C_{ox}}{C_{ox} + C_{IT} + C_s} \text{ where } \psi_s = \psi_{so} \text{ when } V_G = V_{GO}$$

$$\psi_s = \psi_{so} + \int_{V_{Go}}^{V_o} dV_G [1 - \frac{C_{IT} + C_s}{C_{ox} + C_{IT} + C_s}]$$

5.2.1.2 Conductance Method [12]

Under applied ac signal on the gate, with changing gate bias, Fermi level changes. As a result, electrons fill and empty the surface states with varying ac gate bias. This causes an energy loss, and can be observed at all frequencies except for the very low and high frequency.

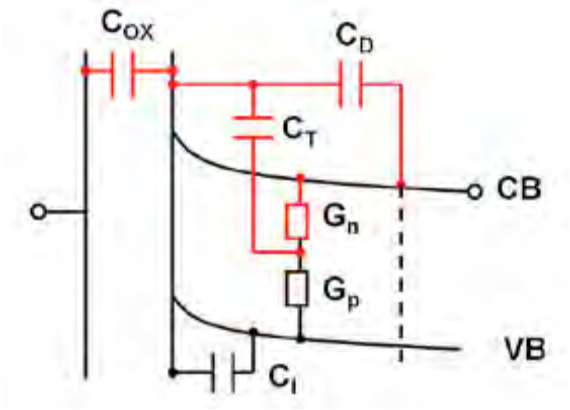

Fig. 5.2 Equivalent circuit of the MOS for conductance measurements. The components in red are the equivalent circuit fot rhe capacitor in inversion.

This energy loss can be measured as an equivalent parallel conductance (Figure 5.2). As the captured electrons spend a finite amount of time within the level, additional capacitance can be measured (C_{it}). At any given ac frequency on the gate, this loss depends both on the speed of response of the interface traps, determined by their capture probability, and on the interface trap level density near the Fermi level at the surface. C_T, G_n, and G_p denote the capacitance associated with the trap, the capture and emission rates to and from this level. When the MOS is measured in depletion, the minority carrier response is neglected when compared to the majority carrier one and the circuit is simplified greatly. The components of the measured admittance can be expressed as

$$\frac{Gp}{\omega} = C_T \omega\tau[1+(\omega\tau)^2]^{-1}$$

$$\text{and } C_p = C_T[1+(\omega\tau)^2]^{-1} + C_D$$

$$\text{where } \tau = \frac{C_T}{G_n}$$

Plotting these components as a function of frequency ω it is observed that the conductance is maximum when $\omega\tau = 1$.

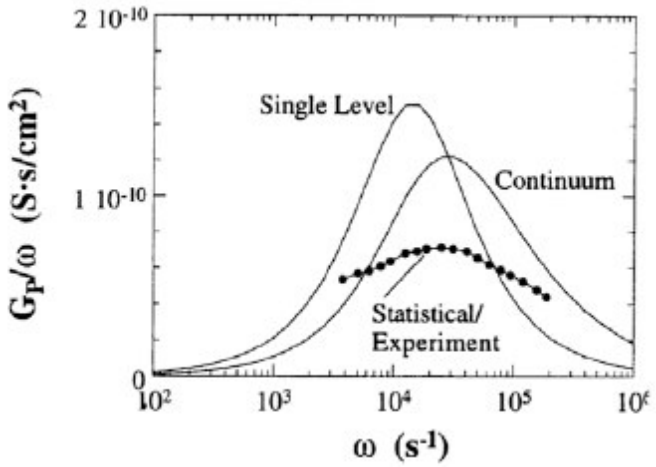

Fig. 5.3 Conductance measurements for Si/SiO_2 capacitors. $D_{it}=1.9\times10^{9}$ $cm^{-2}eV^{-1}$.

With a distribution of such single level traps within the band gap of the semiconductor, the equivalent circuit associated may be assumed to be a parallel combination of the single trap level case and by converting the summations into integrals the following relationships are obtained for the MOS capacitor biased in depletion.

$$C_p = C_{it}(\omega\tau_n)^{-1}\tan^{-1}(w\tau_n) + C_D$$

$$\frac{Gp}{\omega} = C_{it}(2\omega\tau)^{-1}\ln[1+(\omega\tau)^2]$$

The conductance is now maximum when $\omega\tau_n = 1.98$. The interface trap density hence provides for a direct measurement of the interface state density as well as the time constants associated with the trap levels. The above equations get modified further if surface modulation in the potential is assumed. This leads to a flattening of the Gp/ω curves.

5.2.2 Experiment

A 500-nm-thick SiO_2 film was thermally grown on the lightly doped n-type (100) bulk Si substrate at 1100°C and then was patterned by dry-etching followed by

wet-etching to define desired locations for Ge growth. Ge epitaxial layers were selectively grown directly on Si through the patterned SiO_2 windows. For the light n-type doping, arsine was used during the deposition. The initial arsenic doped Ge layer was grown at 400°C at 8Pa, yielding a 400-nm-thick film. This was followed by annealing for 30 minutes at 825°C in H_2 ambient. The growth temperature was then decreased to 600°C and Ge growth was continued for the formation of a 1-μm-thick in-situ arsenic doped Ge layer followed by another 825°C hydrogen annealing.

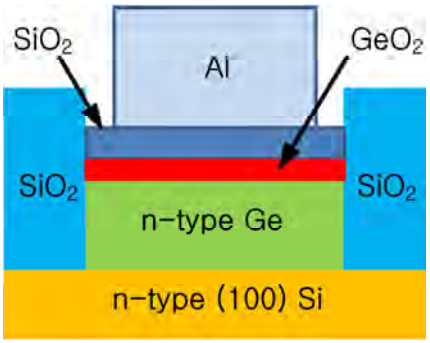

Fig. 5.4 Schematic cross section of Ge MOSCAP

The resulting root mean square (rms) roughness measures around 0.8 nm by atomic force microscopy (AFM) scan over 10×10 μm^2 area. Multi-step Ge growth and heteroepitaxy effectively reduced the threading dislocation density down to ~1× 10^7 cm^{-2} based on the plan view TEM. Defect density decreases with the window size, since more dislocations glide and are trapped at (311) facet surface near SiO_2 during annealing, and do not reach the surface, where devices are fabricated (Fig 5.5 [14, 15]).

The surface of Ge was oxidized at 400°C for 90 sec in a TEL Trias SPA plasma processing system using oxygen radicals to obtain a GeO_2 passivation layer, and then 20nm SiO_2 gate dielectric was deposited by LPCVD at 300°C [17]. For the gate electrode, Al is deposited by using Metallica. Finally, a forming gas annealing (FGA) process at 350°C is performed for 30min.

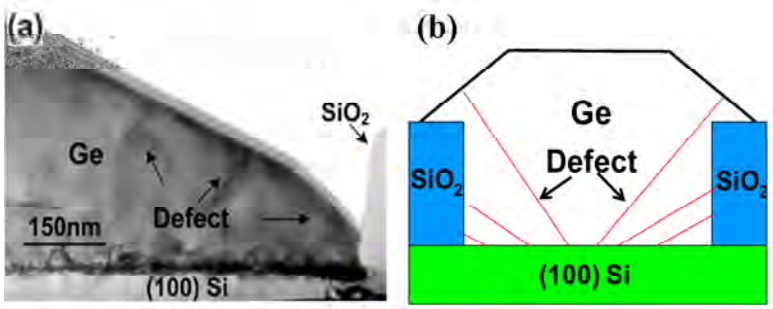

Fig. 5.5 (a) Cross-sectional TEM image of ~ 500nm selectively grown heteroepitaxial Ge layer on Si by MHAH method. (b) Cross-sectional schematic of selectively grown Ge layer on Si at the small window size.

5.2.3 Electrical Characterization

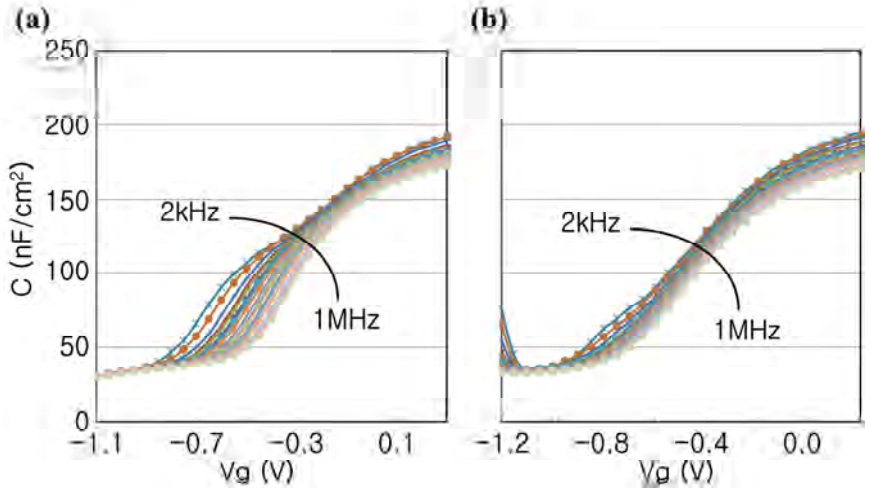

Fig. 5.6 Measured C-V on Al/SiO_2/GeO_2/Ge capacitor at 233K (a) before and (b) after the FGA annealing.

To extract the surface trap density, C-V characteristics were measured on the epitaxially grown n-type Ge layer, before and after the FGA annealing (Figure 5.6). The result shows that the FGA annealing effectively suppressed the trapping and de-trapping of charge, with minimal hysteresis of 25 mV. Compared with the sample without the FGA annealing, FGA annealed sample shows no significant hump due to the interface traps, on the C-V measurement, indicating that the interface has better quality. The inversion capacitance at lower frequencies was measured to be equal to

the oxide capacitance. This effect disappeared when the measurements were performed at lower temperatures around 233 K.

Interface trap characteristics were measured using the conductance method described in section 5.2.1.2. Fig. 5.7 shows the Gp/ω-f characteristics obtained by performing G-V measurements on the samples at 233K. Peak feature is clearly observed in the conductance/frequency as a function of frequency curves. Fig. 5.8 shows D_{it} distribution for GeO_2 interfacial layer. This GeO_2 interfacial layer shows significantly reduced D_{it} of 3×10^{11} $cm^{-2}eV^{-1}$ after FGA annealing.

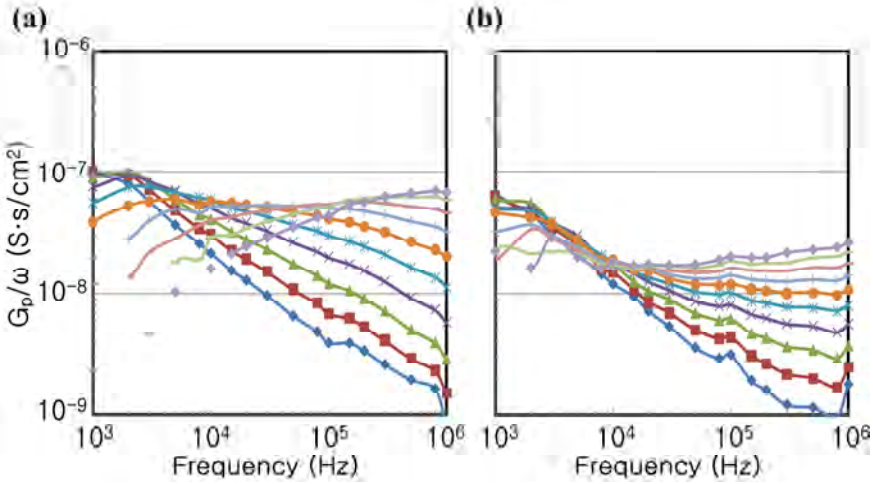

Fig. 5.7 G_p/w-f characteristics of Al/SiO2/GeO2/n-Ge MOS capacitor measured at 233K (a) before and (b) after FGA annealing.

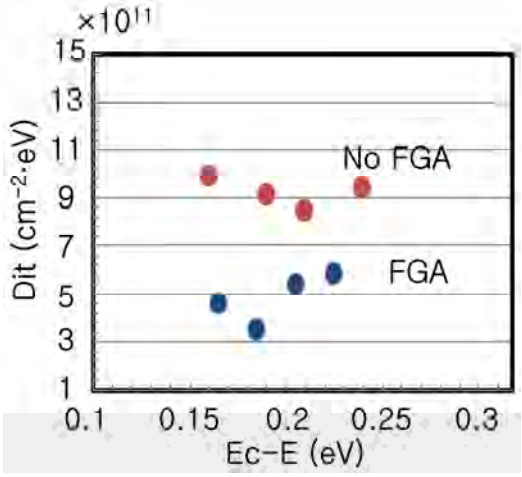

Fig. 5.8 D_{it} distribution in Ge bandgap for GeO_2 in Al/SiO_2/GeO_2/n-Ge.

5.3 Bulk Ge Transistors

5.3.1 Process Flow

5.3.1.1 Ge p-MOSFET

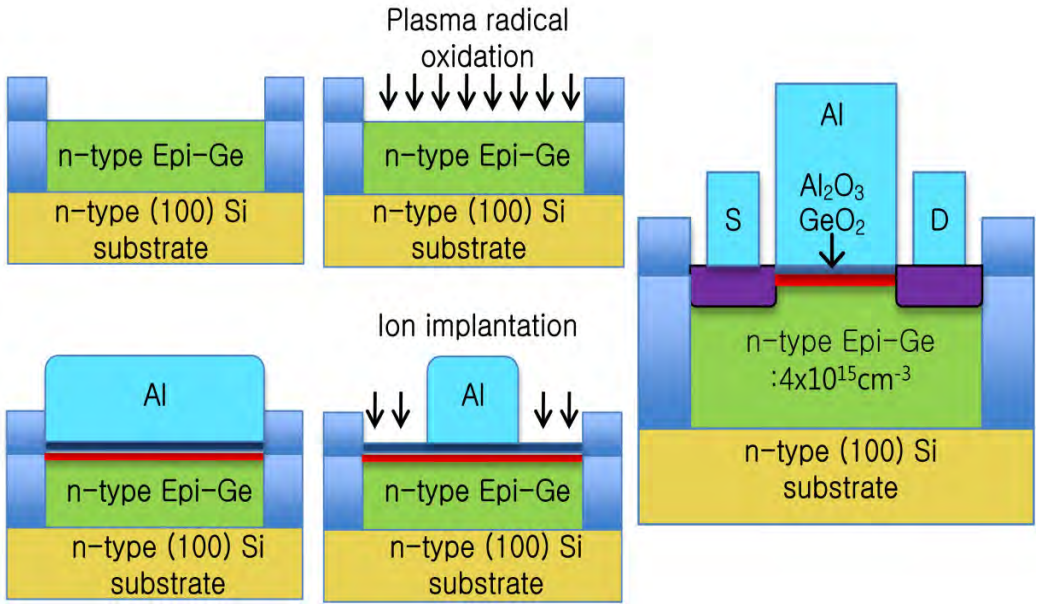

Fig. 5.9 Process flow for fabrication of Ge pMOSFETs with high-k and metal gate.

We begin the process with lightly doped n-type (100) bulk silicon wafers. A 500-nm-thick SiO_2 film was thermally grown on the Si substrate at 1100°C and was then patterned by dry-etching followed by wet-etching to define desired locations for Ge growth. Ge epitaxial layers were selectively grown directly on Si through the patterned SiO_2 windows. For the light n-type doping, arsine was used during the deposition. The initial arsenic doped Ge layer was grown at 400°C at 8Pa, yielding a 400-nm-thick film. This was followed by annealing for 30 minutes at 825°C in H_2 ambient. The growth temperature was then decreased to 600°C and Ge growth was continued for the formation of 1-μm-thick in-situ arsenic doped Ge layer followed by another 825°C hydrogen annealing.

pMOSFETs using GeO_2 and Al_2O_3 as the dielectric and aluminum (Al) as the gate electrode were fabricated. The selective epitaxially grown Ge layer was in situ doped

with As during the deposition step, n-type Ge substrate with doping density of 3×10^{16} cm^{-3}. The surface of Ge was oxidized at 400°C for 90 sec in a TEL Trias SPA Plasma Processing System using oxygen radicals to obtain a GeO_2 passivation layer, and then 4.5nm Al_2O_3 high-k gate dielectric was deposited by atomic layer deposition (ALD) at 350°C using $Al(CH_3)_3$ and O_3. The dielectric substrate interface D_{it} for $Al/Al_2O_3/GeO_2$ gate stack on the epitaxial Ge layer was ~ 3.5×10^{11} cm^{-2} eV^{-1}. This value is near the D_{it} value for the same gate stack on bulk Ge [16]. Al was deposited as a gate electrode. After gate definition, boron (BF_2) was implanted to form self-aligned source/drain. The dopants were activated by the forming gas annealing (FGA) at 400 °C for 30 min. After annealing, the contact windows were opened, and Ti/Al were deposited and patterned by lift-off process to form ohmic contacts. The fabricated devices have a ring-type structure with gate length of 15 μm.

5.3.1.2 Ge n-MOSFET

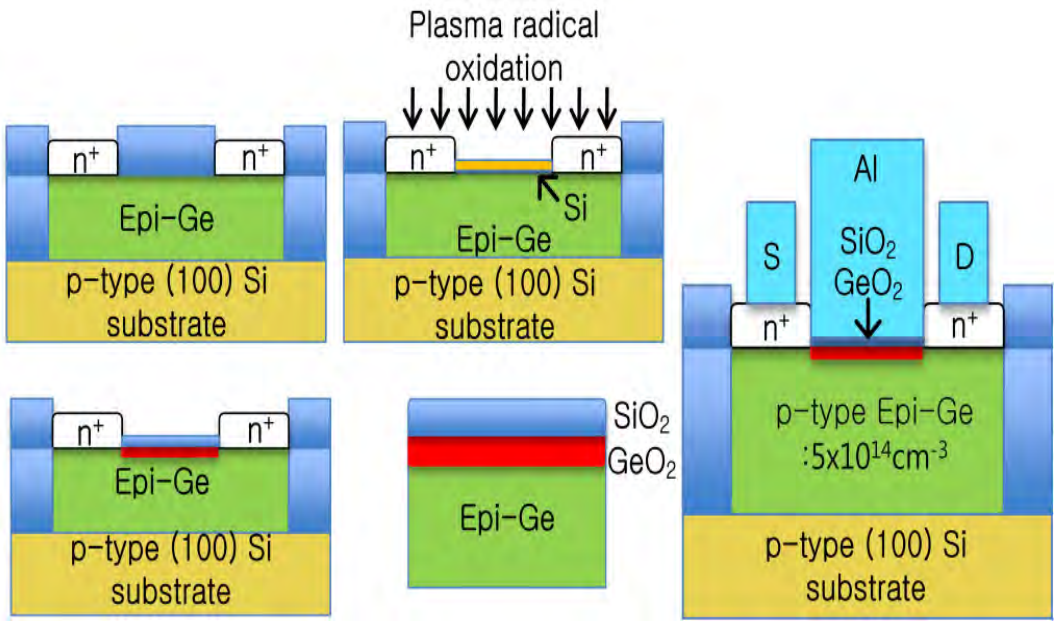

Fig. 5.10 Process flow of Ge nMOSFETs with raised S/D.

Fig. 5.10 shows the schematic process flow to fabricate n-type raised S/D MOSFET. A 500-nm-thick SiO_2 film was thermally grown on a lightly doped p-type

(100) Si substrate at 1100 ^{o}C. The SiO_2 film was then patterned by dry-etching followed by wet-etching to define desired locations for Ge growth. This wafer was cleaned according to the standard Si wafer cleaning process and immediately loaded into an Applied Materials Centura RP-CVD epitaxial reactor. A hydrogen bake at 900^{o}C was carried out to ensure no native oxide remained on the Si surface. The initial Ge film was grown at 400^{o}C and 8 Pa, yielding a 400-nm-thick film. This was followed by annealing in H_2 ambient for 30 min at 825^{o}C. The growth temperature was increased to 600^{o}C for the second Ge layer. Finally, a 15 min H_2 bake at 750^{o}C completed the intrinsic Ge epitaxial process. This intrinsic Ge epitaxial layer showed p-type 4×10^{15} cm^{-3} of electrically activated concentration. The root mean square (rms) roughness of the resulting film was measured to be ~0.6 nm by atomic force microscopy (AFM) scans on 10×10 μm^2 area. Due to the multi-step Ge growth and hydrogen annealing on the selective area, the grown layer showed low defect density, having a threading dislocation density of ~1×10^7 cm^{-2} based on the plan view TEM [8]. SiO_2 layer was deposited at 300^{o}C and patterned for the source/drain area. An *in-situ* doped n-type Ge layer with diluted 1% phosphine doping was selectively grown at 600^{o}C on the intrinsic Ge layer for 1min to form n^+/p raised S/D. The gate area is opened by HF wet-etching for the gate stack. The thin Si layer (2nm) was grown at 500^{o}C on the opened gate area at RP-CVD epitaxial reactor. The surface of gate area was oxidized at 500^{o}C in a TEL Trias SPA Plasma Processing System using oxygen radicals to obtain a GeO_2 (1nm) and SiO_2 (2nm) as a passivation layer and a dielectric layer, respectively. Al was deposited as a gate electrode. After gate definition, the contact windows were opened, and Ti/Al ohmic contacts were deposited and patterned by lift-off process. The fabricated devices have a ring-type structure with 100 μm of gate length.

5.3.2 Ge Transistor Characterization

5.3.2.1 Ge p-MOSFET

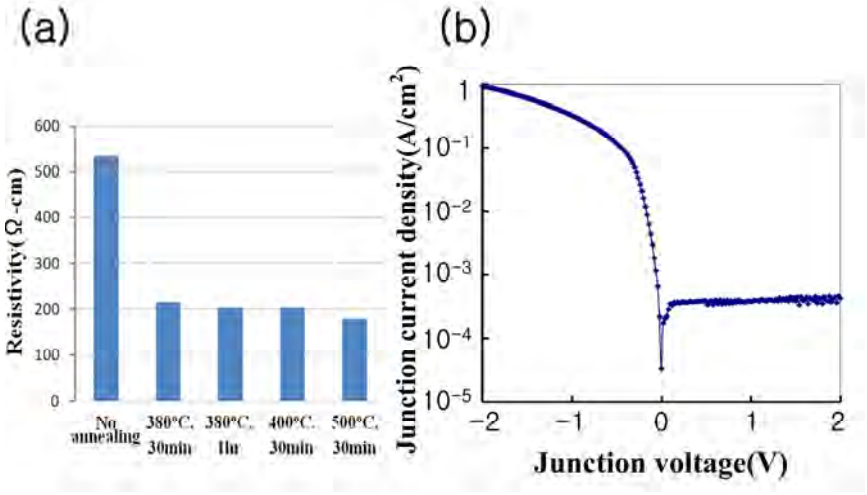

Fig. 5.11 (a) Four-point probe measurement of boron implanted Ge after FGA annealing showing the reduction in sheet resistance. (b) Junction current density of P+/N junction after 400°C annealing for 30 min.

In Fig. 5.11(a), Four-point probe measurements show a huge reduction in sheet resistance after FGA annealing at and beyond 380°C. Annealing at temperature above 400°C does not show significant change in sheet resistance. Annealing temperatures as low as sub-400°C have been reported in fabrication of Ge MOSFETs [17, 18]. As shown in Fig 5.11(b), with a post-implant anneal at 400°C for 30 min, the p+/n junction diodes on the selectively grown Ge substrate have a low leakage current density of 10^{-4} A/cm^2 with high I_{on}/I_{off} ratio, which is considered acceptable for device operation.

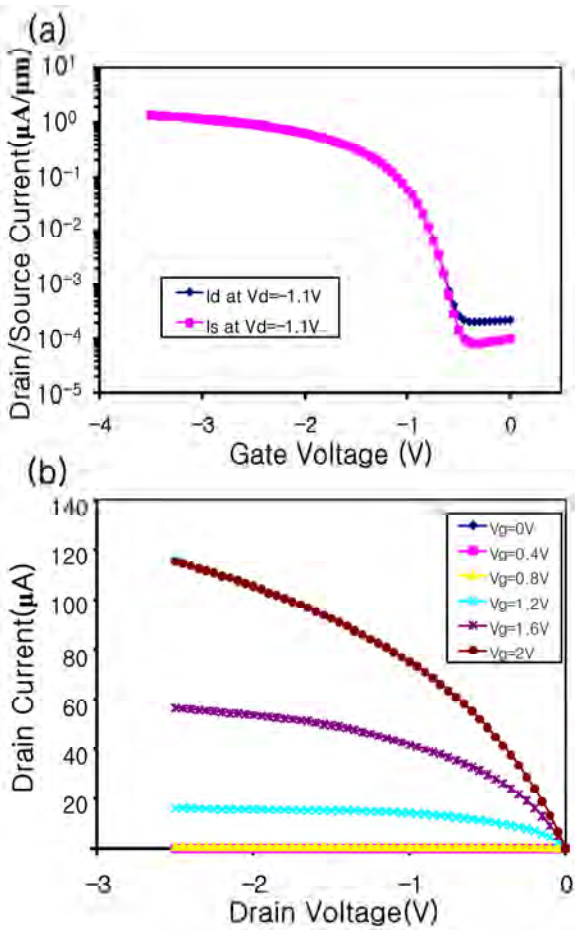

Fig. 5.12 (a) Measured I_D/I_S-V_G characteristics at -1.1 V drain bias and (b) measured I_D-V_D characteristics for Ge pMOSFET with L_G=15μm.

Fig 5.12 shows the measured I_D/I_S-V_G and I_D-V_D characteristics, respectively, of the Ge pMOSFETs with W/L ratio of 200μm/15μm. The gate leakage current is shown to be low as ~10^{-9}A/cm^2. This gate leakage is negligibly small compared to the drain or source current. Because off current minimization and the maximization of I_{on}/I_{off} ratio are one of the challenging issues concerning Ge and GeOI pMOSFETs, I_{on}/I_{off} measurement is performed and shown in Fig 5.12. In Fig 5.12(a), the Ge pMOSFET provides a reasonable I_{on}/I_{off} ratio of 6.3×10^3 at -1.1V drain voltage and shows the off current density of 2×10^{-4} μA/μm with 15 μm gate length. In addition, it exhibits a high I_{on} (1.39μA/μm at -3V gate voltage) in the drain current measurement. The difference between source and drain current at low gate voltage is due to the junction leakage current of drain and substrate.

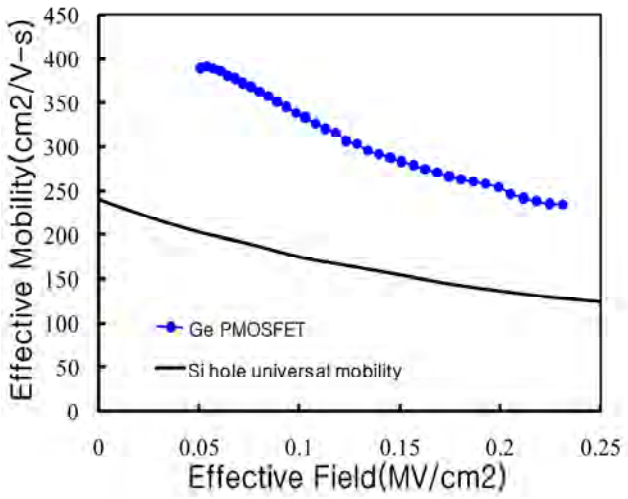

Fig. 5.13 (a) Effective hole mobility as a function of effective field measured from Ge pMOSFETs and Si universal hole mobility.

To determine the effective mobility (μ_{eff}), drain current (I_D) and the inversion charge (Q_n), equation for $\mu_{eff}=I_D/(W/L)V_{DS}Q_n$ was used [19]. I_D as a function of the gate bias (V_G) was measured at drain-source voltage of -50 mV. Split C-V measurement was carried out at 100 kHz using a ramp rate of 50 mV/s to determine the inversion charge density in the channel, using $Q_n= C_{inv}\bullet dV_g$. In Fig 5.13, effective mobility versus effective E-field plot is extracted from the 15 μm gate length pMOSFET. For comparison, the Si universal hole mobility curve is also shown. Ge pMOSFETs show ~80% mobility enhancement over the Si universal hole mobility. A peak mobility of 391 cm^2/Vs at 0.051 MV/cm was observed as shown in Figure 4. To the best of our knowledge, this is one of the highest mobilities which have been reported on unstrained-channel Ge pMOSFETs [17, 18, 20-23]. The similar peak hole mobility of ~400 cm^2/Vs has been recently reported for Ge pMOSFET using thermally-oxidized GeO_2 interfacial layers [23]. Our results also outperform data of p-MOSFETs on MHAH-grown Ge layer on Si with GeO_xN_y gate dielectrics [21]. However, short channel p-MOSFETs show relatively low mobility due to the substrate doping to control the short channel effect [5-8]. This high effective mobility indicates the high quality of Ge layer on Si by the selective MHAH technique.

5.3.2.2 Ge n-MOSFET

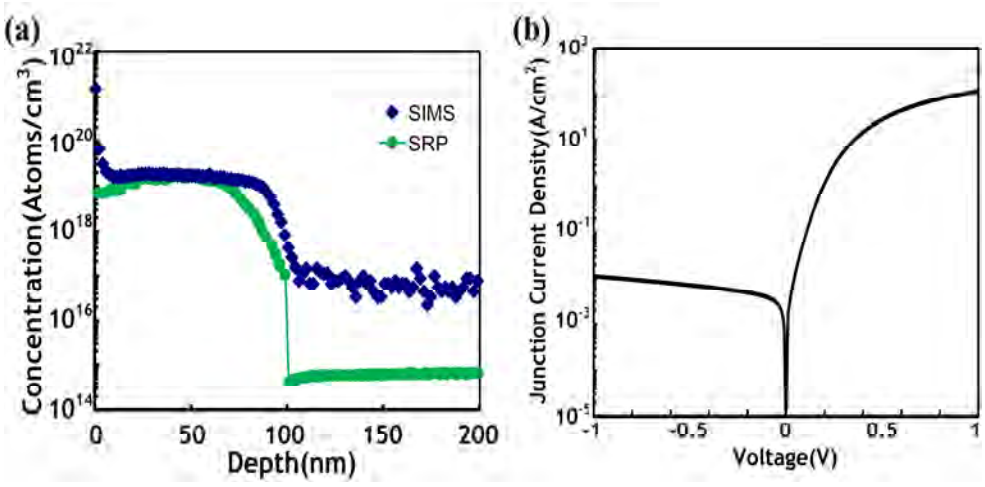

Fig. 5.14 (a) SIMS and SRP depth profiles of P in 600 ^{o}C *in-situ* doped Ge layer growth for 1min. (b) Junction current density of n^{+}/p junction diodes using 600 ^{o}C/1min *in-situ* doping.

Figure 5.14(a) shows the depth profiles of phosphorus (P)-doped Ge layers grown under 600^{o}C for 1min to form shallower and abrupt junction. Both secondary ion mass spectrometry (SIMS) and spreading resistance profiling (SRP) data are presented. n-type dopants diffused into the intrinsic Ge layer up to 35nm due to 600^{o}C *in-situ* deposition for 1 min from the initial interface. At this condition, the resultant n^{+}/p junction has a junction depth of 97nm and a peak electrically activated concentration of $2\text{x}10^{19}$ cm^{-3}. This *in-situ* doped profile also exhibits an abrupt edge near n^{+}/p junction from SRP data yielding a slope for the decay of the phosphorus concentration of 13 nm/decade. SIMS and SRP data confirm ~100% dopant activation without any post annealing step after 600^{o}C 1min *in-situ* doped Ge layer growth.

In Fig 5.14(b), the n^{+}/p junction diode formed by 600^{o}C *in situ* doping shows a high performance diode characteristic having $1.1\text{x}10^{4}$ on/off ratio and high forward current density (120A/cm^2 at 1V). To the best of our knowledge, this is one of highest forward current densities and on/off ratios [9-11].

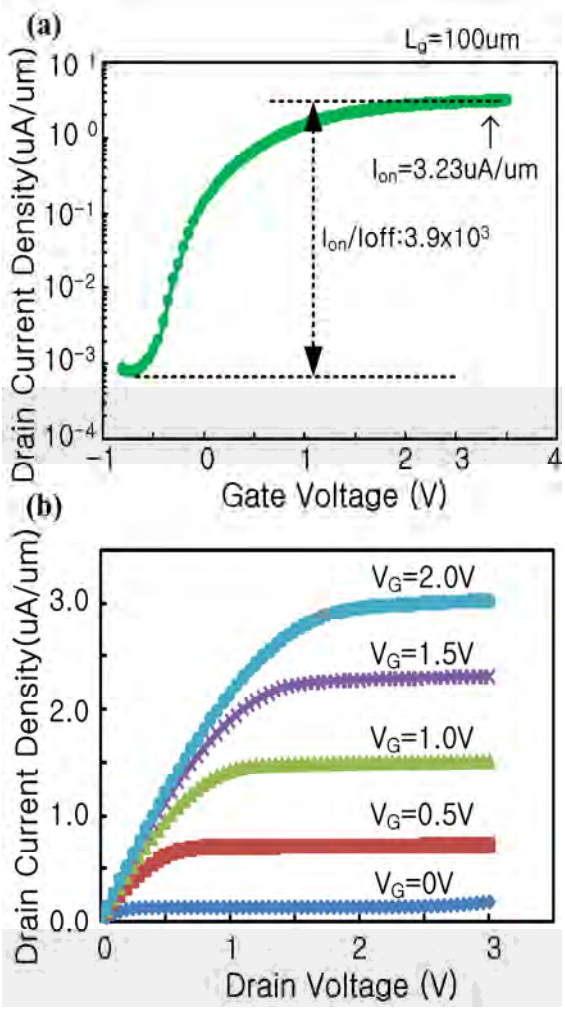

Fig. 5.15 (a) Measured I_D-V_G characteristics at 1.2 V drain bias and (b) measured I_D-V_D characteristics for Ge nMOSFET with L_G=100μm.

Figure 5.15 shows the measured I_D/I_S-V_G and I_D-V_D characteristics, respectively, of the Ge nMOSFETs with W/L ratio of 130μm/100μm. Because suppressing off current density and maximizing I_{on}/I_{off} ratio are challenging issues concerning Ge nMOSFETs, I_{on}/I_{off} measurement is performed and shown in Fig 3. In Fig 5.15(a), the Ge nMOSFET provides one of the highest I_{on}/I_{off} ratios of 4×10^3 at 1.2V drain voltage and shows the off current density of 6×10^{-4} μA/μm for 100 μm gate length [12-14]. In addition, it exhibits high I_{on} (3.23μA/μm at 3V gate voltage) in the drain current measurement.

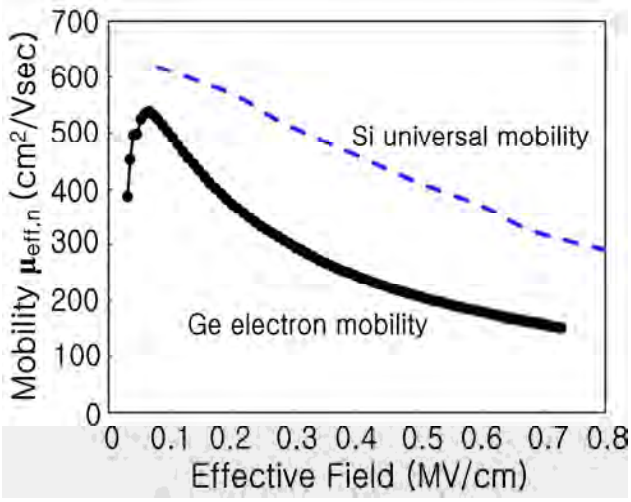

Fig. 5.16 Effective electron mobility as a function of effective field measured from Ge nMOSFETs and Si universal electron mobility.

The effective carrier mobility can be expressed as a function of drain current (I_D) and inversion charge (Q_n), as $\mu_{eff}=I_D/(W/L)V_{DS}Q_n$ [15]. To extract the carrier mobility, I_D and Q_n were measured from the device. I_D as a function of the gate bias (V_G) was measured at drain-source voltage of 50mV. Split C-V measurement was carried out at 100kHz using a ramp rate of 50mV/s to measure the inversion charge in the channel ($Q_n= C_{inv}\bullet dV_g$). In Fig 5.16, effective mobility versus effective E-field is extracted from the 100μm gate length nMOSFET. For comparison, the Si universal electron mobility is also shown. Ge nMOSFETs still show less effective electron mobility over the Si universal electron mobility. However, a peak mobility of 540cm^2/Vs at 0.07 MV/cm was observed as shown in Fig 5.16. To the best of our knowledge, this is one of the highest mobilities reported on (100) Ge to-date [12-14].

5.4 Conclusion

We have successfully demonstrated high-mobility Ge p-MOSFETs with high-k dielectric and metal gate by selectively growing Ge through patterned SiO_2 on Si using the selective MHAH technique which allows high quality Ge layer on Si. The hole mobility is enhanced by ~80% compared to the Si hole universal mobility. We have also demonstrated high-performance Ge n-MOSFETs with raised S/D by selectively growing Ge through patterned SiO_2 on Si. The novel n-MOSFETs show the highest electron mobility reported on (100) Ge to-date. Furthermore, these devices provide an excellent I_{on}/I_{off} ratio (4×10^3) with very high I_{on} of 3.23μA/μm.

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CHAPTER 6:

High Efficiency P-I-N Photodetectors on Selective-area-grown Ge for Monolithic Integration Under Biaxial and Uniaxial Strain

6.1 Introduction

Si based devices for optical applications have widely been researched. However, developing a Si photodetector that operates in the 1.3-1.55μm wavelength range is a challenging task, because of its relatively large indirect (~1.1eV) and direct (~3.4eV) band gap energies. Since Ge naturally has smaller direct bandgap energy of 0.8eV, corresponding to ~1.55 microns wavelength, and this makes Ge a strong candidate for optical application. Also, Ge can be easily integrated with existing Si complementary metal oxide semiconductor (CMOS) technology, further making it an attractive material for optical applications.

In particular, Ge optical detectors on Si are being aggressively researched as a potential solution for optoelectronic integration application. As a result, several heteroepitaxial techniques have been introduced to grow Ge on to Si. For example, employing super lattice buffer layers to grow Ge layers effectively reduced the large lattice mismatch between Si and Ge, yielding optical detectors with quantum efficiency of 40% at 1.3μm [1]. Cyclic thermal annealing is another method of heteroepitaxial growth, with reported responsivity of 0.56A/W at 1.55μm wavelength for 1-μm-thick Ge films grown on Si [2]. Also, molecular beam epitaxy (MBE) is yet another method to grow Ge on Si, and it can create thin strain-relaxed buffers on silicon substrate. This method shows external quantum efficiency of 2.8% at 1.55μm [3]. These methods are focused on the bulk heteroepitaxial growth on Si. However,

selective-area-heteroepitaxy is a promising approach for the monolithic integration of Ge based optoelectronics on Si CMOS VLSI platform and thus needs to be thoroughly studied. Several integration methods based on selective-area-heteroepitaxy have been suggested for monolithic integration with waveguide. Evanescently coupled Ge waveguide photodetector demonstrates responsivity of 0.89 A/W at 1550nm and dark current density of 25mA/cm^2 at -1V [4]. Butt-coupled Ge photodetector integrated in SOI rib waveguide showed a responsivity as high as 1 A/W at wavelength of 1550nm and low dark current density of 60mA/cm^2 [5].

In this chapter, we demonstrate a normal incidence *p-i-n* Ge photodiode by selectively growing Ge through patterned SiO_2 window on Si using the multiple hydrogen annealing for heteroepitaxy (MHAH) technique. We report a high efficiency *p-i-n* photodiode with a high responsivity over broad detection spectrum, making monolithically integrated on-chip or chip-to-chip optical links more feasible. We also demonstrate uniaxial tensile and compressive strain of Ge p-i-n photodiodes on Si using four-point bending structures. The resulting shift of the Ge direct bandgap is investigated through the photocurrent absorption spectrum shift in these photodiodes.

6.2 Experiment

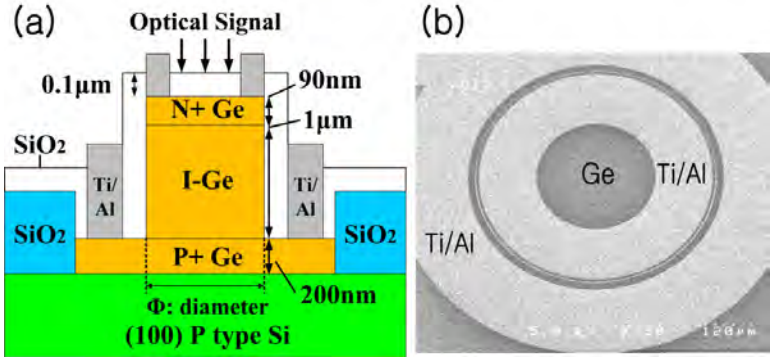

Fig. 6.1 (a)Schematic cross section of normal incidence Ge/Si p-i-n photodiode. (b)Scanning electron micrograph of the circular mesas of the photodiodes. The circular p-i-n device has the ring-shaped contact with ring width of 50 μm.

Fig. 6.1(a) shows the schematic cross section of a Ge *p-i-n* photodiode. A 500-nm-thick SiO_2 film was thermally grown on a lightly doped p-type (100) Si substrate at 1100 ^oC. The SiO_2 film was then patterned by dry-etching followed by wet-etching to define desired locations for Ge growth. Ge epitaxial layers in a *p-i-n* structure were selectively grown directly on Si in windows opened through the SiO_2 layer. To obtain abrupt junctions and good electrical contact, a 200-nm-thick heavily in-situ boron-doped Ge layer was deposited initially [6] at 400^oC and 8Pa. This was followed by annealing for 30 minutes at 800^oC in H_2 ambient. The growth temperature was then increased to 600^oC for the formation of 1-μm-thick intrinsic Ge layer followed by another 800^oC hydrogen anneal. Finally, a heavily doped 90 nm thick n^+-type Ge layer was grown at 600^oC. To avoid recombination in the n^+ Ge layer, we needed a shallow n^+ layer and an abrupt n^+/i junction. To achieve this with a high level of n-type dopant activation, n+ layer was in-situ doped with diluted 1% phosphine. The resulting n^+ junction has a depth of 97nm and a peak electrically activated concentration of $2x10^{19}$ cm^{-3} [7]. Because fast n-type dopant diffusion during the high temperature process makes it difficult to fabricate p-i-n structure in Ge photodiodes, we fabricated top-most n+ layer without post hydrogen annealing to prevent phosphorus from diffusing inside 1-μm-thick intrinsic Ge layer [8,9]. The root mean square (rms) roughness of the resulting film was determined to be ~0.67 nm by 10×10 μm^2 area atomic force microscopy (AFM) scans. The samples annealed in nitrogen at 825°C exhibited no reduction in surface roughness [10]. Due to the selective heteroepitaxy and hydrogen annealing, the Ge layer had a low threading dislocation density count of 1×10^7 cm^{-2} based on the plan-view TEM, which is suitable for optoelectronic applications. The *p-i-n* Ge photodiodes were realized as mesa structures from 150 to 300 μm diameter. The mesa structures were patterned by HBr/Cl_2 reactive ion etching (RIE) of the Ge layer to a depth of 1 μm. On top of this Ge film, a 100 nm thick low temperature silicon oxide (LTO) layer was deposited at 300^oC for surface passivation. Windows for the contacts were then patterned on the oxide and etched in HF, followed by metal deposition using electron-beam metal evaporation and photoresist lift-off. About 25nm

of Ti was used as contact material, topped with ~45 nm of Au. Figure 6.1(b) shows the SEM top view of the resulting *p-i-n* Ge photodiode.

6.3 Results and Discussion

6.3.1 Electrical Characteristics

The dark current density of the photodiode not only indicates the material quality but also determines optical receiver sensitivity [11, 12].

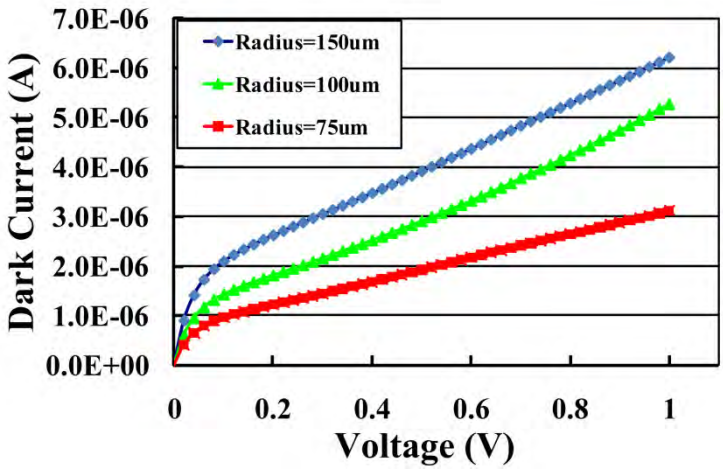

Fig. 6.2 Dark current vs. reverse bias curves of the circular shape mesa Ge/Si *p-i-n* photodiodes.

Figure 6.2 shows the dark current-voltage (I-V) characteristics of photodiodes with various mesa radii. For large photodiodes with radius of 150 μm, the dark current density is 9.9 mA/cm^2 at a reverse bias of 1 V. The dark current can be related to bulk dark current density (J_{bulk}) and the peripheral surface leakage density (J_{surf}) through

$$I_{dark} = J_{bulk} Area + J_{surf} B\sqrt{Area}$$

where B is $\sqrt{4\pi}$ for a circular photodiode.

For the diode operating at 1 V reverse bias, the extracted J_{bulk} and J_{surf} are shown to be 3.2 mA/cm^2 and 62 μA/cm, respectively. This very low bulk current density of 3.2 mA/cm^2 confirms the excellent Ge crystal quality and the shallow and abrupt n^+ junction in Ge with a high level of activation of n-type dopant, using in-situ

phosphorus doping during the epitaxial growth.[13, 14] These are among the lowest reported dark current density values among the Ge *p-i-n* photodiodes.[2,3,15,16,17]

6.3.2 Origin of Residual Tensile Strain

The Ge layers grown on Si are relaxed at the growth/anneal temperature, through defects and dislocations. As the samples are cooled down to the room temperature, due to the different thermal expansion coefficients between Ge and Si, Ge layers experience strain (Figure 6.3). For Ge, linear thermal expansion coefficient is $\Delta a/a(Ge)=5.8\times10^{-6}\ \Delta T\ (^{o}C)$, while for Ge, $\Delta a/a(Si)=2.6\times10^{-6}\ \Delta T\ (^{o}C)$ [18], and this difference causes the lattice mismatch between Si and Ge to increase with temperature: 4.18% at room temperature, 4.38% at 600^{o}C and 4.45% at 825^{o}C. Our films are annealed in hydrogen ambient at 825 ^{o}C and cooled down to the room temperature. With decreasing temperature, Ge tends to contract faster than Si, and experience 0.14%biaxial tensile strain form the Si substrate. It has been suggested that this phenomenon occurs most probably because the perpendicular lattice parameter of our Ge layers shrinks more easily during the cooling-down phase than the in-plane one, whose temperature behavior is somewhat influenced by the Si substrate underneath.

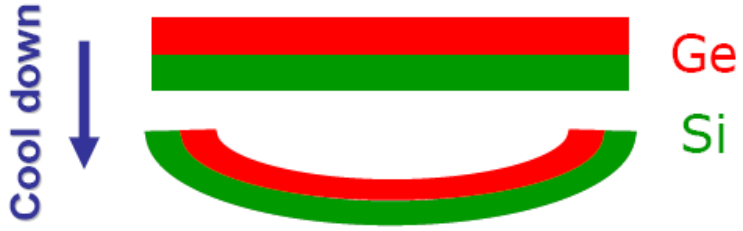

Fig. 6.3 Schematic illustration of mismatch between coefficients of thermal expansion between Si and Ge.

6.3.3 Effects of Strain on Ge Band Structure

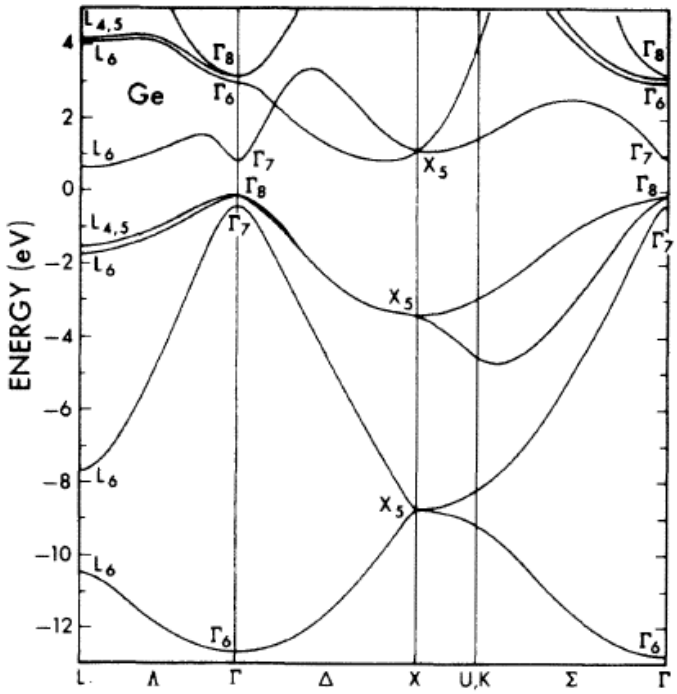

Fig. 6.4 Band structure of Ge calculated by Chelikowsky and Cohen [19].

Figure 6.4 shows the energy-momentum (E-k) diagram for unstrained Ge. As we apply stain on Ge, band structure changes (Fig. 6.6). Change in the band structure with strain is plotted on Figure 6.5 [20]. The conduction band minimum at the zone center is denoted by $\Gamma_{7,c}$. The valence band maxima for light holes and heavy holes are denoted by $\Gamma_{8,v1}$ and $\Gamma_{8,v2}$, respectively. The direct band gap, defined as the energy difference between the conduction band and the valence band at the zone center, is highlighted. As shown on the figure, conduction band maximum increases and valence band minimum decreases, and as a result, direct band gap shrinks with increasing tensile strain. In addition, the effective masses are also slightly modified due to the strain.

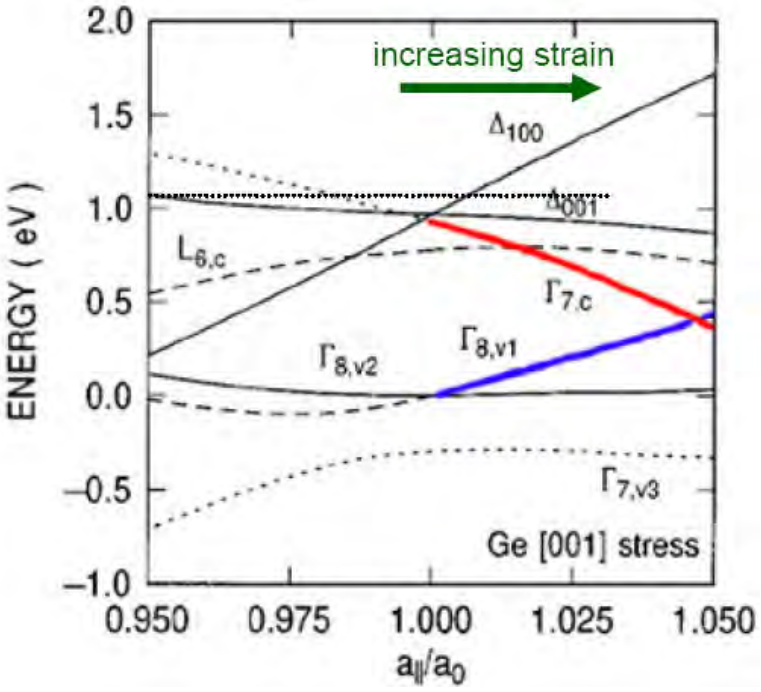

Fig. 6.5 Deformation of band structure of Ge with biaxial strain calculated by Fischetti. The change in the conduction band minima at the zone center and the valence band maxima for light holes with increasing biaxial tensile strain are highlighted by red and blue, respectively.

Figure 6.7 plots the simulation results for the band gap change with applied strain. This confirms that under tensile strain, band gap decreases. Band gap shrinkage causes increase in the absorption strength, owing to an increase in the available density of states around the band edge. Also, due to the smaller band gap, photons with smaller wavelength, which cannot be detected by unstrained Ge detectors, can be absorbed.

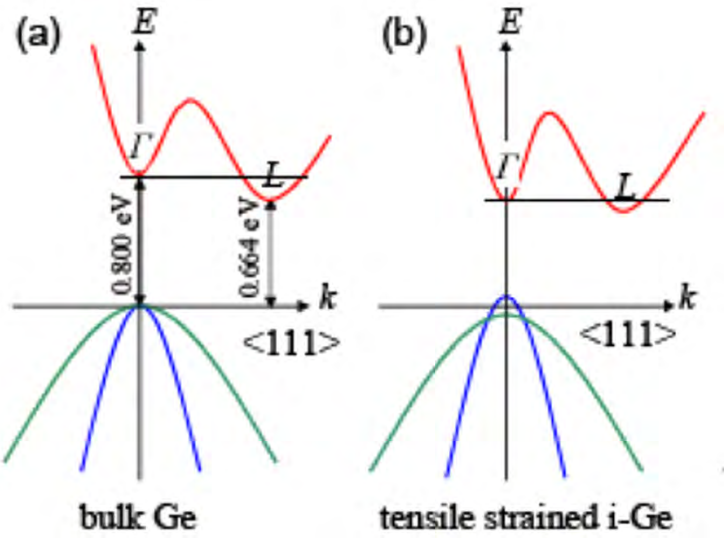

Fig. 6.6 Illustration of the change in the bands with biaxial tensile strain in the Ge film.

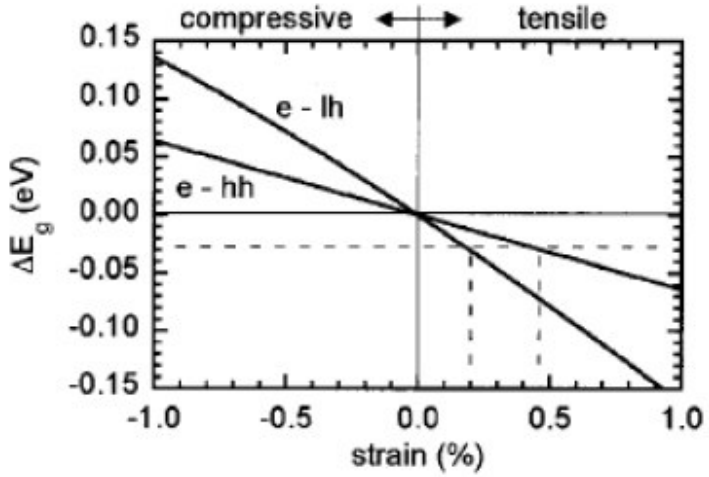

Fig. 6.7 The change in the direct gap energy of Ge calculated [21].

6.3.4 Optical Characteristics under Biaxial Strain

Figure 6.8 shows responsivity ($\Re$) versus reverse bias (V) plot for the Ge *p-i-n* photodiode operating at 1.55μm with 140μW light incident power. The active absorption area of the device is $\pi\times10^4$ μm^2 and the thickness of the absorbing Ge layer is 1μm. A responsivity of ~ 0.67 A/W was measured for a reverse bias of 1 V, corresponding to 53.6% external quantum efficiency (η). The residual strain in this

selectively grown Ge is 0.141 % as determined by Raman spectra measurement, while that of the bulk grown Ge is 0.204 %. The extracted tensile strains in both cases arise from the difference in thermal expansion coefficients between Ge and Si. During the cooling stage after Ge deposition, the decrease in lattice constant of Ge is suppressed by that of the Si substrate, generating residual tensile strain in Ge layer [21]. The lower tensile strain value in the selectively grown Ge compared to bulk grown Ge can be explained by the Ge confinement by SiO_2, which has compressive strain. However, more detailed study is needed to verify this effect. This 0.141 % tensile strain reduces the direct bandgap of Ge from 0.801 to 0.781 eV, extending the effective photodetection wavelength. The responsivity of the *p-i-n* Ge photodiode is further improved on the bulk grown Ge because of the higher tensile strain of the bulk grown Ge. This responsivity of 0.67A/W at 1.55um is the highest value among reported selective area grown Ge *p-i-n* photodiodes. [15, 22] The responsivity at 0V bias is also about 93% of the maximum responsivity measured, indicating excellent carrier collection efficiency [23].

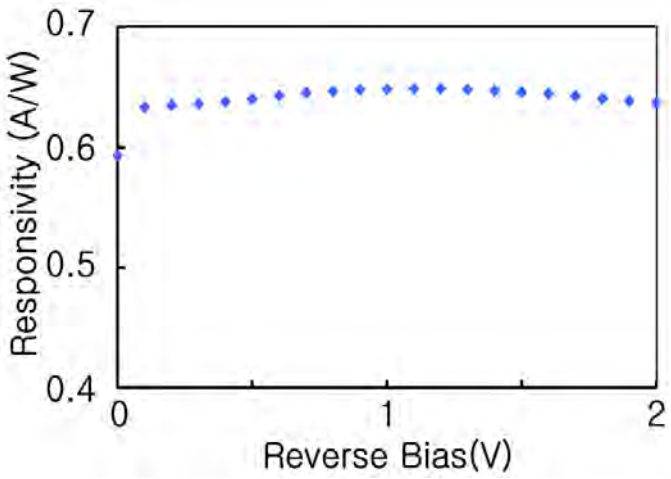

Fig. 6.8 Photodetector responsivity at λ=1.55 μm versus reverse bias for the mesa Ge p-i-n photodiodes with a radius of 100 μm.

From the responsivity, the absorption coefficient (α) of the tensile strained Ge can be derived. Responsivity ($\Re$) and reflectivity (γ) of the device can be related to α at a certain photon energy by

$$\alpha = -\frac{1}{t_{Ge}} \ln(1 - E \bullet \frac{\Re}{(1-r)})$$

where t_{Ge}=1μm is the thickness of undoped Ge film, and E is the photon energy.

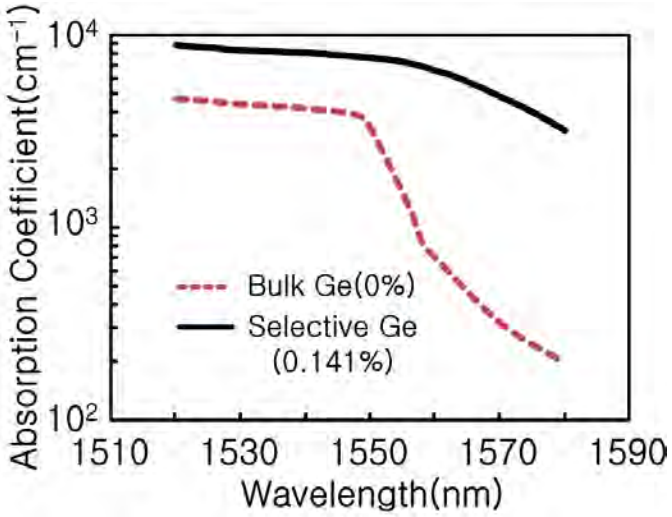

Fig. 6.9 Absorption coefficient at 2V reverse bias versus photon wavelength. Absorption coefficient (α) is extracted from measured responsivity assuming 90% internal efficiency. The α for bulk Ge is plotted for reference.

Figure 6.9 shows the extracted absorption coefficient versus wavelength. For comparison, the absorption curve of the unstrained Ge photodiodes is also included [17]. The spectral responsivity shows that the optical characteristics of the selectively grown Ge layer is affected by the residual tensile strain. It is clear that the absorption edge of strained-Ge has shifted toward longer wavelengths. Spectral measurement verified the red shift of the absorption edge corresponding to 0.141 % tensile strain, which leads to enhanced absorption efficiency. The increase in absorption coefficients greatly improves the responsivity of the Ge photodiodes on the selectively grown Ge for monolithic integration on Si. Moreover, MHAH-Ge layers can absorb the same amount of light intensity in thinner layers thanks to high absorption coefficient. For

instance, at λ=1550nm, the intrinsic layer could be made half the thickness compared to that of bulk-Ge detectors, resulting in shorter transit times for carrier collection, hence higher speed of operation.

6.3.5 Optical Characteristics under Uniaxial Strain

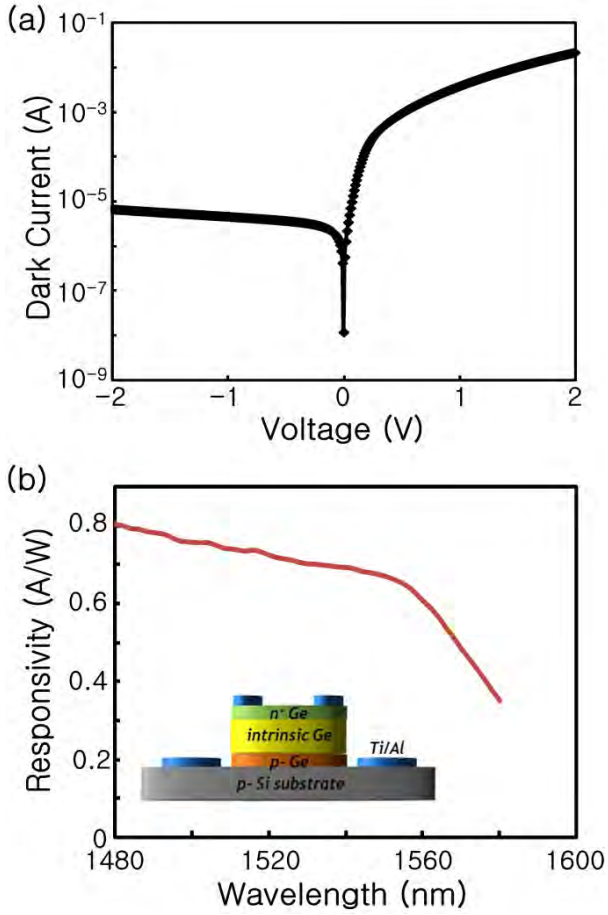

Fig. 6.10 (a) Dark current versus reverse bias for circular shape mesa Ge/Si p-i-n photodiodes. (b) Photodiode responsivity at 1V reverse bias versus wavelength.

Figure 6.10 shows the I-V characteristics and responsivity spectra of selectively grown Ge p-i-n photodiodes on Si without any external uniaxial bending. These I-V characteristics show a high performance diode with low reverse current density (10

mA/cm^2 at -1V) and 1x10^4 on-off ratio. This low dark current density indicates the high quality of the Ge epitaxial film. We measured a responsivity of ~0.67 A/W at 1550 nm wavelength under 1V reverse bias in Fig 6.10 (b). This high responsivity could be attributed to the 0.141% biaxial tensile strain in the Ge film.

To impose external uniaxial tensile strain in the Ge photodiodes, a four-point bending structures as shown in Figure 6.11(a) were used. The amount of the stress (σ_c) in the film can be extracted by

$$\sigma_c = \frac{-3dz \cdot E \cdot t}{a(3L-4a)}$$

where *dz* is the displacement of the wafer, *E* is the Young's modulus, and *t* is the wafer thickness (0.5mm), *a* is the distance between the two adjacent inner and outer points, and *L* is the distance between two outer points [24]. By increasing the displacement of the wafer, we can increase the uniaxial stress that is applied to the sample.

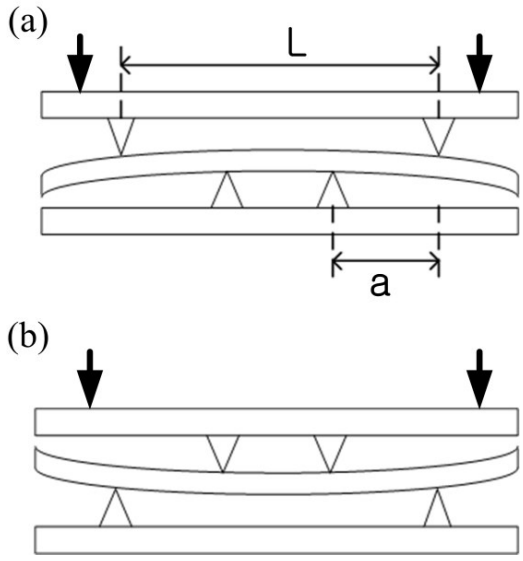

Fig. 6.11 Schematic diagrams of 4-point bending structures for (a) uniaxial tensile strain and (b) uniaxial compressive strain.

The wafer was loaded in the <110> direction on the four-point bending apparatus. The maximum values of tensile stress was limited to 113MPa, corresponding to a 0.082% tensile strain in the Ge layer by the wafer breakage due to the high stress. The

optical absorption spectra were measured while the wafer was under uniaxial tensile stress, as shown in Fig 6.12(a). The uniaxial tensile stress effectively shifts the absorption spectra toward higher wavelength from the absorption edge. At the same time, the responsivity at 1550nm wavelength increases from 0.67 to 0.75 A/W with 0.082% tensile strain (113MPa).

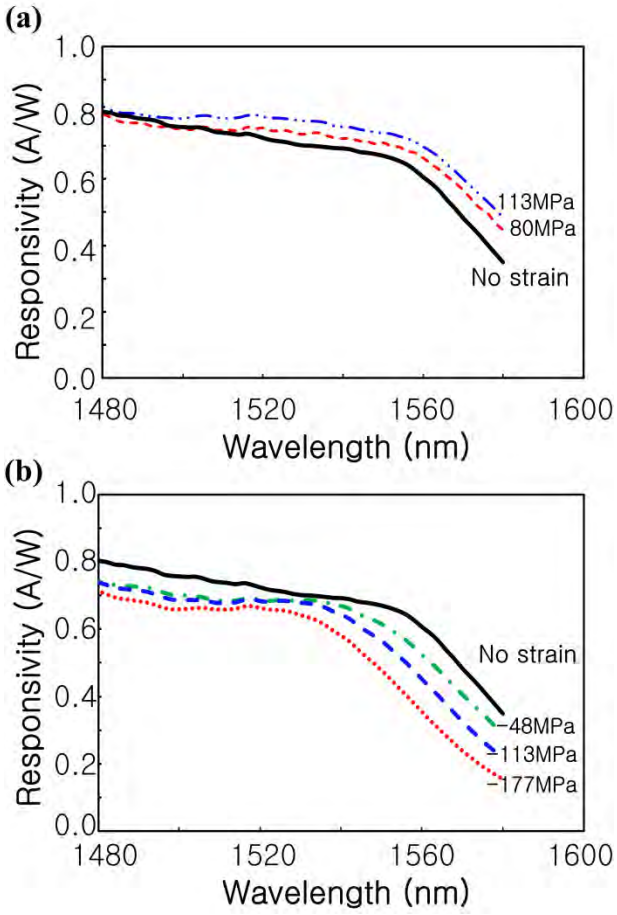

Fig. 6.12 Photodiode responsivity at 1V reverse bias versus wavelength under (a) uniaxial tensile and (b) compressive stress in the <110> direction.

A similar four-point bending structure, as shown in Figure 6.11(b) can impose compressive stress to the sample. The maximum applied compressive stress in our measurement is 177MPa, corresponding to a 0.129% compressive strain in the Ge layer. As shown in Figure 6.12 (b), the absorption edge shifts linearly under

compressive stress. And the responsivity at 1550nm decreases to 0.477A/W under 0.129% uniaxial compressive strain.

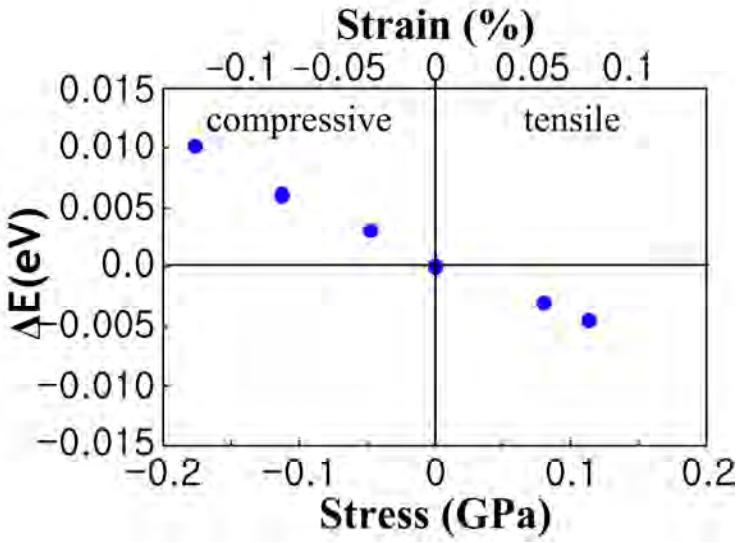

Fig. 6.13 Photon energy shift of uniaxially strained p-i-n Ge photodiodes as a function of uniaxial strain in <110> direction.

The dependence of the absorption edge in eV on uniaxial stress is extracted from the photocurrent spectra and plotted in Figure 6.13. For the tensile stress case, the photon energy moves toward lower energy while the energy shifts toward higher energy for compressive stress. In the uniaxial tensile strain case in <110> direction, the strain reduces the direct band gap of Ge layer, leading to the shift in the absorption edge towards the lower energy regime. Also, the compressive strain increases the direct band gap of Ge, making the spectrum shift in the absorption edge toward higher energy.

Also plotted in Fig. 6.14 are the direct band gap energy changes simulated by the Non-local Empirical Pseudopotential method. In the simulation, 0.14% biaxial tensile strain is considered, in addition to various different uniaxial strain values. The solid line is the predicted band gap energy change between the top of the heavy-hole valence band and the bottom of the conduction band at the Γ point. And the dashed line is the predicted band gap energy change between the top of the light-hole valence band and the bottom of the conduction band at the Γ point. Even without any uniaxial strain, the valence band splits into heavy-hole and light-hole bands and the direct band

gap energy is reduced due to 0.14% residual biaxial tensile strain. Under the uniaxial tensile strain, the observed photon energy shift from the absorption edge is related the light hole transition.

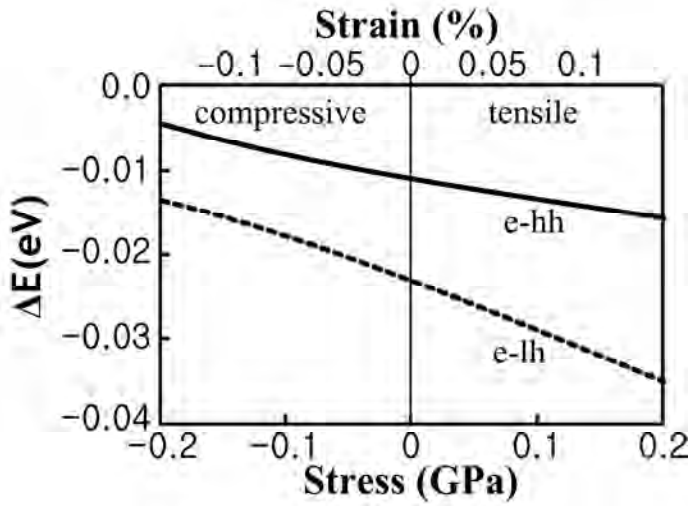

Fig. 6.14 Band gap energy shift of uniaxially strained p-i-n Ge photodiodes as a function of uniaxial strain in <110> direction of simulation.

6.4 Conclusion

We have demonstrated a 0.14 % tensile strained normal incidence Ge *p-i-n* photodiode selectively grown on Si for monolithic integration. A low bulk dark current density of 3.2mA/cm^2 indicates good Ge film quality and a highly activated in-situ doped *n*+ layer. Responsivity of 0.67 A/W was achieved at 1.55μm wavelength. The 0.14 % residual tensile strain in the selectively grown Ge resulted in enhanced efficiency in the near infrared regime and shifted the absorption edge to longer wavelengths. This high efficiency even at low reverse bias makes this technology a promising candidate for monolithic integration of Ge optoelectronics on Si for optical communication. We have also demonstrated a uniaxial tensile and compressive strained Ge p-i-n photodiode integrated on Si by using four-point bending structure. The responsivity at 1550nm increases from 0.67 to 0.75 A/W with uniaxial tensile

strain and decreases to 0.477 A/W under compressive strain. These uniaxial tensile or compressive strains cause the absorption spectrum to shift toward lower or higher energy because they reduce or increase the direct band gap of the Ge layer, respectively.

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CHAPTER 7:

Conclusion

In this dissertation, Ge CMOS and optical detector technologies for monolithic integration of Ge devices on Si platform based on selective heteroepitaxial growth of Ge have been discussed in detail. Main contributions of this work are summarized in this chapter.

7.1 Contributions

(1) Ge heteroepitaxial growth process was extensively investigated using TEM, AFM, and SEM. Selective Ge epitaxial growth process using the MHAH technique was developed for monolithic integration of Ge devices on Si platform. Hydrogen annealing and the selective growth can be used to reduce the dislocation density and surface roughness. Also, over-lateral Ge growth process using the MHAH technique was developed for Ge-on-insulator structure with reduced threading dislocation density and surface roughness.

(2) Ge in-situ doped epitaxial growth technique for high performance n+/p junction was investigated. Abrupt and box shaped junctions with high level activation of P were accomplished using *in-situ* doping technique. This process will be feasible for ultra shallow junctions. The fabricated Ge n^+/p junction diodes showed excellent electrical characteristics with 1.1×10^4 on/off current ratio and high forward current density.

(3) Ge MOSFETs technologies were developed for monolithic integration. High-mobility Ge p-MOSFETs with high-k dielectric and metal gate were fabricated using

the selective MHAH technique. Hole mobility was enhanced by ~80% compared to the Si hole universal mobility. High-performance Ge n-MOSFETs with raised S/D were also fabricated. The novel n-MOSFETs showed highest electron mobility reported on (100) Ge to-date. Furthermore, these devices provided an excellent I_{on}/I_{off} ratio with very high I_{on} of 3.23 μA/μm.

(4) Ge optical detector technologies were developed for monolithic integration with Si platform. High efficiency p-i-n photodiodes on selective-area-grown Ge were fabricated. Low bulk dark current density of 3.2mA/cm^2 indicates good Ge film quality and a highly activated in-situ doped *n*+ layer. Responsivity of 0.67 A/W was achieved at 1.55 μm wavelength due to the residual tensile strain. The uniaxial tensile and compressive strain effects were extensively investigated on Ge p-i-n photodiode by using four-point bending structure. The responsivity at 1550 nm increased due to the direct bandgap change under the uniaxial tensile strain.

7.2 Recommendation for future work

In this dissertation, selective Ge heteroepitaxial growth and in-situ doped growth techniques were developed and studied to fabricate high performance Ge CMOS and photodiodes. However, a lot of works still need to be done in order to improve Ge MOSFETs' and optical detection's performance.

(1) In chapter 3, selective Ge growth technique through the SiO_2 window was introduced for high quality Ge layer. High resolution TEM analysis was done to see the Ge sidewall crystal quality between Ge and SiO_2. However, the electrical characterization will be a very interesting topic. MOSCAP structure based on Ge layer sidewall will work nicely for this characterization.
(2) In chapter 3, over-lateral Ge growth for GOI structure was also suggested. During the over-lateral growth process, we observed the void on the SiO_2 sidewall. Therefore, the GOI structure for the device fabrication is limited by this void

formation. If this void formation can be removed, we can use this GOI structure for more various CMOS and optical device applications.

(3) N-type in-situ doping technique was developed for Ge n+/p junction in chapter 4. To characterize and analyze this, SIMS and SRP analysis were used. And n+/p junction diode showed high performance. However, for the device application, we also have to consider contact resistance. Therefore, we need to analyze the contact resistance based on in-situ doping technique. Due to the high diffusivity of n-type dopant, we also need to characterize n-type dopant diffusion after high temperature annealing.

(4) Ge n-MOSFETs with raised S/D were demonstrated in the chapter 5. We solved the problem of high series resistance in S/D. We also need to investigate the parasitic capacitance reduction in this n-MOSFET.

(5) In chapter 6, high efficiency p-i-n Ge photodiodes were demonstrated for monolithic integration. Ge photodiodes were fabricated on the selectively grown Ge layer through the SiO_2 window. This technology can be further exploited in conjunction with the SOI or polymer based waveguide schemes to realize a waveguide photodiode photodetector integrated on a Si chip. We demonstrated the effect of externally applied uniaxial stress, however, further work is needed to develop a processing technique to incorporate uniaxial tensile stress.