FLUORINE PASSIVATION OF DEFECTS IN GERMANIUM DEVICES

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Abstract

Despite the first point contact transistor ever to be made, germanium (Ge) based transistors were abandoned a few years after its birth and were replaced by silicon. Only after 40 years of successful silicon based CMOS scaling from ~10μm to sub-μm regime, Ge is again gaining interest from semiconductor industry as a next generation semiconductor material, mainly due to it's higher and more symmetric electron and hole mobility than silicon (Si) counterpart and its process compatibility to current Si technology. However, due to its low band-gap (0.66eV) and fragile nature, Ge is affected severely by the presence of defects within the crystal and on the surface. For complementary-metal-oxide-semiconductor (CMOS) and opto-electronic devices such as Ge based photo detectors and lasers, effects of these defects mainly manifest in the form of electron and hole mobility degradation, low activation of n-type dopant in the source and drain, high leakage current under "off"-condition, and shorter carrier lifetime, which all hinder the successful adaptation of Ge devices by the industry. Over the years, various works have been done in identifying the nature of these defects. However, effective method of eliminating or reducing the presence of these defects is yet to be seen.

In this dissertation, passivation of Ge defect sites using fluorine (F) is proposed and investigated first. Fluorine, being the most reactive element in the periodic table has high potential to bond with the Ge defect sites, thereby eliminating their degenerate effects. But before incorporating F into the Ge defect sites, properties of Ge defects and its impact on electrical properties are thoroughly investigated. For the second part, the electrical effects of defects within bulk Ge are experimentally investigated, by intentionally inducing defects by Ge ion implantation. Here, the F is introduced to the defective Ge by ion-implantation, followed by additional thermal anneal step in order for F to bond with Ge defect sites. For the third part, this method is applied to n+/p Ge diode and Ge n-MOSFET fabrication, and the effects of F passivation are investigated in terms of electrical performance. In the fourth part, the effect of F passivation is further investigated in aspect of carrier lifetime through F treated Ge p-n diode.

Acknowledgements

The past seven-year journey towards a PhD. degree at Stanford was not a straight one. If felt like being thrown on to an empty white plane with infinite freedom to wander around with no restrictions. There was no set of objectives to turn my direction to. I would have been lost, if it were not for the people that I had the privilege to meet along the journey.

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have his opinion on the problem in a different view, and his vast knowledge on Ge/high-k oxide interfaces greatly accelerated my research. I thank Professor Yoshio Nishi and Professor Philip Wong for their academic advice and support, as their doors were always open for discussion.

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Chapter 1

Introduction

1.1 Motivation

Germanium (Ge), despite being the semiconductor material that was used in the first historical point contact transistor, was quickly abandoned and was replaced by silicon (Si). The main reason behind this was that Ge had a poor native oxide called germanium dioxide (GeO_2), which was non-ideal as a gate oxide material and for surface passivation. In addition, GeO_2 was very fragile in nature, even dissolving in water, which made Ge based device processing impractical. Silicon (Si), a sister material of Ge on the other-hand, had a very strong and robust native oxide called silicon dioxide (SiO_2). Many scholars and people in industry today agree that it played a formidable contributing role that enabled the era of Si based CMOS scaling. Si based

devices became the mainstream semiconductor material for the next 40 years, impacting our daily lives immensely. Figure 1.1 shows a simple trend of Si based MOSFET scaling over these years. As the scaling continued below sub 1μm, the Si community found it ever increasingly difficult to continue this trend, as problems like short channel effect (SCE) and parasitic resistance became increasingly more dominating in eclipsing the performance. Nevertheless, thanks to innovative ideas and technologies such as strained channel, high-κ gate dielectric, metal gate, and FinFETs, the dimension continued to scale down to sub 100 nm. As we now approach the sub 10nm regime, the Si based CMOS technology will eventually be limited by low on current (I_{on}).

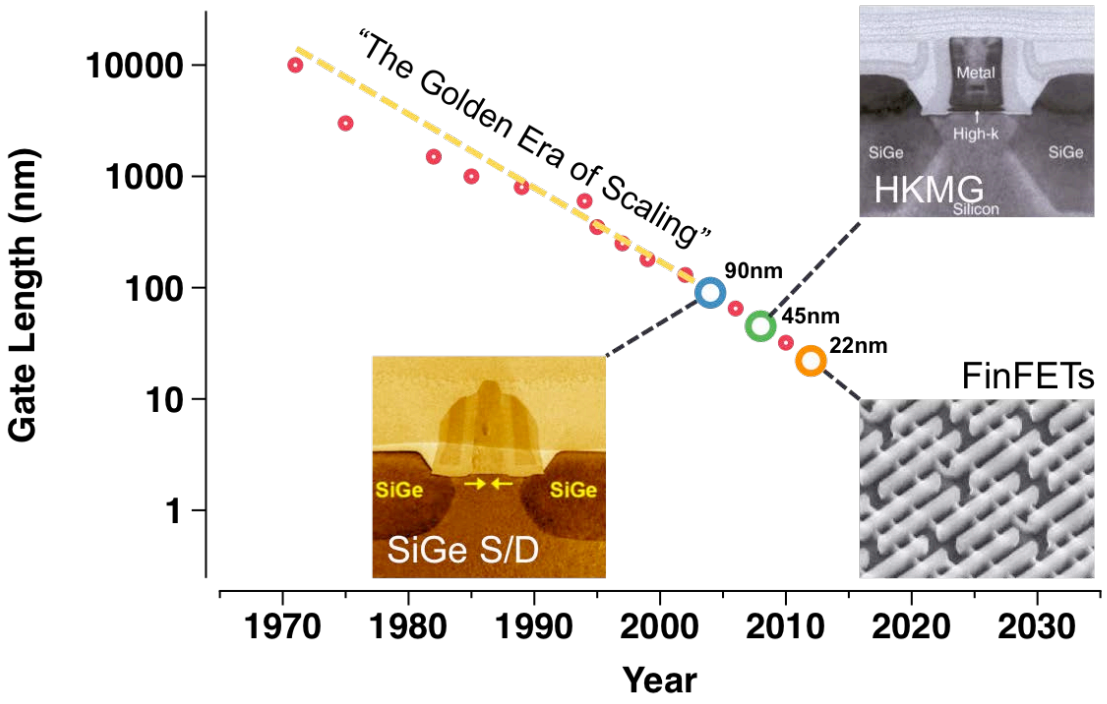

Figure 1.1 Trend of Si CMOS scaling from the 1970s to present, showing the gate length decreasing with progressing years.

As the device community prepares for this inevitable end, other device structures and materials are being sought to ensure continued improvement of transistor performance. Among these, Ge began to regain the interest that it had lost 40 years ago. For a start, Ge has higher and more symmetric electron and hole mobility compared to Si as shown in Table 1.1. This enables the Ge based transistors to operate faster than Si transistors under ideal conditions. It is also compatible with currently existing Si based processing techniques, making it easier to adapt to current industry. Although III-V materials such as GaAs have better properties in terms of mobility, III-V material act as contaminates in Si, making it a challenge to combine with Si based transistors.

Mobility (cm^2/V-s)	Si	Ge	GaAs
Electron	1500	3900	8500
Hole	475	1900	400

Table 1.1 Comparison of mobility between Si, Ge, and GaAs. Mobility for electron and hole for Ge is higher than Si, while being more symmetric.

Interest on Ge based transistors quickly began to expand in the early 2000s, and soon researchers identified the following problems to be solved if Ge based technologies were ever to be introduced to the industrial market.

1. Gate oxide replacement for GeO_2.

2. Heavy n-type doping in source and drain for Ge n-MOSFET.

3. Low contact resistance between metal to S/D interface for Ge n-MOSFET.

4. Leakage current reduction.

For problems concerning the gate dielectric, intensive research has been done using high-κ gate dielectrics such as aluminum oxide (Al_2O_3) [4], hafnium oxide (HfO_2) [5], and zirconium oxide (ZrO_2) [6] as a replacement oxide for GeO_2. Among these, Takagi et al. recently managed to show a high quality sub 1 nm gate dielectric comprised of thin GeO_2 and Al_2O_3 [7] where the interface defects go down as low as $\sim 10^{10}/cm^2$.

For scaling Ge based transistors, one requires a heavily doped source and drain. For Ge p-MOSFET, S/D doping is not a big problem, for one could achieve electrically active doping of over 1 x $10^{20}/cm^3$ using boron (B). In addition, p-type dopant such as B do not diffuse much during activation around 400 °C, making shallow junction easily achievable [8]. However, problem arose in doping the S/D of Ge n-MOSFET with n-type dopants such as phosphorus (P), arsenic (As), and antimony (Sb). Because of n-type dopant deactivation phenomenon, it was very hard to achieve doping concentration of over 5 x $10^{19}/cm^3$ and to make it worse, the n-type dopant seemed to diffuse very fast while its activation process at above 400 °C. Obviously, this made Ge p-MOSFET technology to be more developed than the Ge n-MOSFET counterpart. However, for full Ge CMOS implementation, one needs both Ge n- and p- MOSFETs.

High contact resistance between n-type Ge contact metal is also a challenge. As shown in Figure 1.2 (referenced from [1]), because of Fermi level pinning phenomenon, the metal Fermi level is always pinned near the valence band of Ge regardless of the metal contact. This helps Ge p-MOSFETs where the main conduction is by holes, which face near zero-Schottky barrier as a result of pinning. However, for Ge n-MOSFETs the electrons will always see a large barrier between the metal and the semiconductor, which causes a problem when the Ge MOSFETs are scaled down as shown in Figure 1.3 (referenced from [2]).

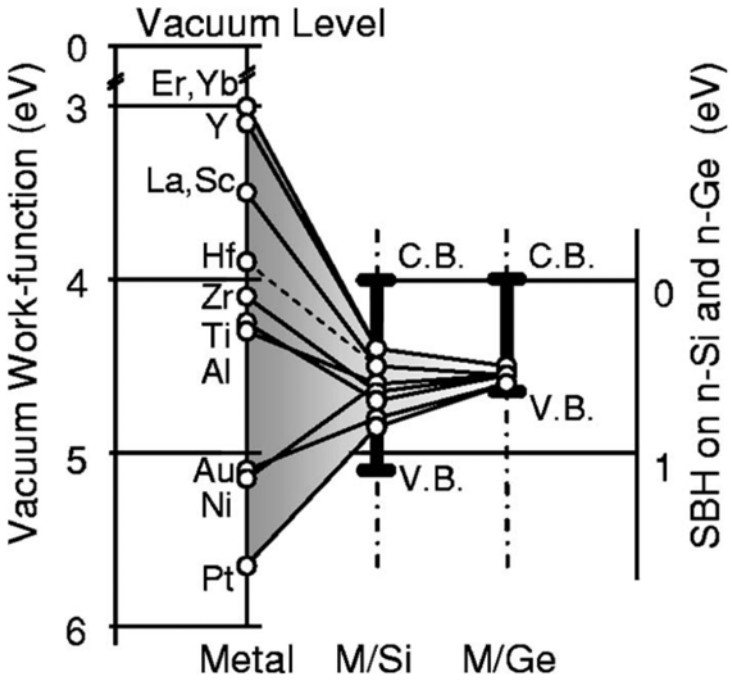

Figure 1.2 Work function of metals and their Schottky barrier height when contacted with Ge. Because of Fermi level pinning, the energy level of the contact is pinned near the valence band of Ge, regardless of metal work function [1].

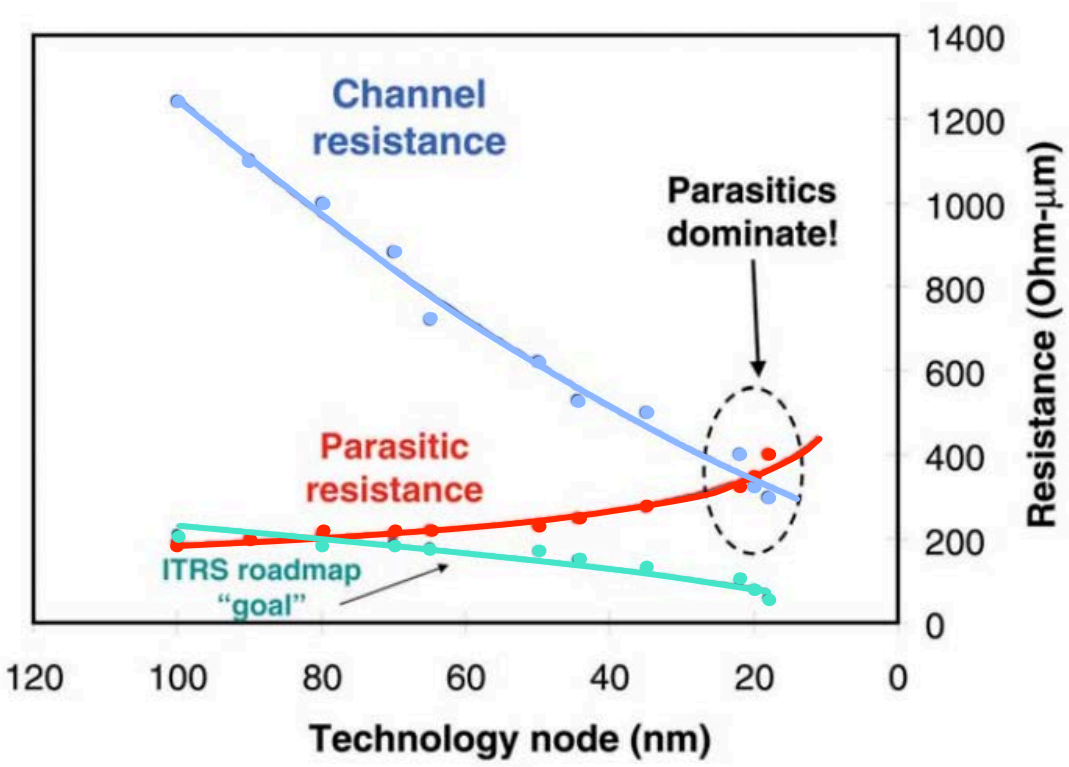

Figure 1.3 Comparison of channel resistance and parasitic resistance, according to technology node [2].

Leakage in the junction will also be one of the problems that Ge based transistor technology will have to overcome. Ge has a relatively lower bandgap of 0.66 eV, which is about half the value of Si bandgap of 1.12 eV. This means that Ge will be more vulnerable to leakage problems due to band-to-band tunneling and trap assisted thermal recombination and generation.

For each problem mentioned above, extensive research has been done to find out the fundamental reasons behind these problems, which indicated that presence of defects within the Ge crystal or the surface is one of the main problems. If we were to

presume that Ge is more fragile in nature than Si, it would naturally be more vulnerable to damage during a MOSFET fabrication. Especially, ion implantation and gate oxide deposition process will be the key area where defects will be created and affect the transistor performance. Therefore, it will be critical to reduce the presence of these defects. Although there are numerous ways of reducing or eliminating these defects, in this dissertation, the method is mainly focused on using fluorine (F) as passivating element for both bulk and surface defects within Ge.

1.2 Organization of the Dissertation

Chapter 2 explains the basic background information on defects in Ge and their role as in its electrical characteristics. It will also cover how they degrade Ge based MOSFET performance. Motivation of using F as a passivation element will also be explained.

Chapter 3 covers the experimental evidence that defects created within the Ge crystal electrically act as acceptor sites, thus acting as p-type dopants. Discussion on the healing processes of the defect site by thermal anneal will be covered along with using F to passivate the defect sites.

Chapter 4 implements the F passivation method discussed in chapter 3 to phosphorus (n-type) doped Ge and investigate the effects of F in enhancing the overall dopant activation and retarding the diffusion process. Following this discussion, we

apply this passivation method to a simply n+/p diode and investigate its current-voltage characteristics.

Chapter 5 focuses on using F passivation to Ge p- and n-MOSFET devices for electrical performance enhancement, mainly mobility enhancement in the channel and parasitic resistance reduction in the source and drain regions. In addition, carrier lifetime enhancement by F passivation in a n+/p diode is investigated, for the possibility of its application to opto-electronic devices.

Chapter 6 summarizes the key achievements from the previous chapters and concludes the dissertation with suggestions to future works.

Chapter 2

Defects and their Role in Ge Based Devices

2.1 Introduction

In this chapter we will introduce the basic terminology of defects within a given crystal and explain the role they play in Ge crystal. Going further into the chapter, their impact on Ge based MOSFET and how they are created during fabrication will be discussed. In this dissertation, it will be found that vacancy defects and surface defects will be the main culprits that degrade the performance of Ge based devices. In addition, previous efforts to minimize the defects will also be mentioned.

2.2 Defects in a Semiconductor Crystal

Crystallographic defects can be classified according to their dimensions; point defects being zero dimensional defects, line defects (1D), planar defects (2D), and bulk defects (3D). In this dissertation the attention will be focused on point defects and planar defects which affects the Ge based transistors more severely and much harder to eliminate completely.

2.2.1 Point defects

Point defects are basically where an atom lattice site is vacant in a crystal or is out of its ideal position. Figure 2.1, shows the type of point defects within a crystal. This could happen during a high temperature-annealing step, where the atom can randomly diffuse through the lattice. As the atom moves to a different location, the site it leaves might not be filled at the end, hence leaving an empty spot. This is typically called 'vacancy defect'. Self-interstitial defect is where an atom has managed to find it's stable state in an interstitial void between the lattice sites. This could happen during an ion-implantation process where an ion can displace the atoms in the crystal lattice as it collides with certain energy. Beside this types of defect, similar things can happen when an impurity atom that has been injected intentionally wanders through the lattice. If the atom in the interstitial void is an impurity atom, it will simply be called as an interstitial impurity atom. A substitutional impurity atom is an atom that seats in the proper crystal lattice site, the only difference being that it is an impurity atom.

Although this may seem non-ideal, it is through this impurity atom that we obtain the doping effects in semiconductors. For example, if a phosphorus atom seats in this lattice site, one extra electron will be unbound, which can contribute as a free electron in the crystal.

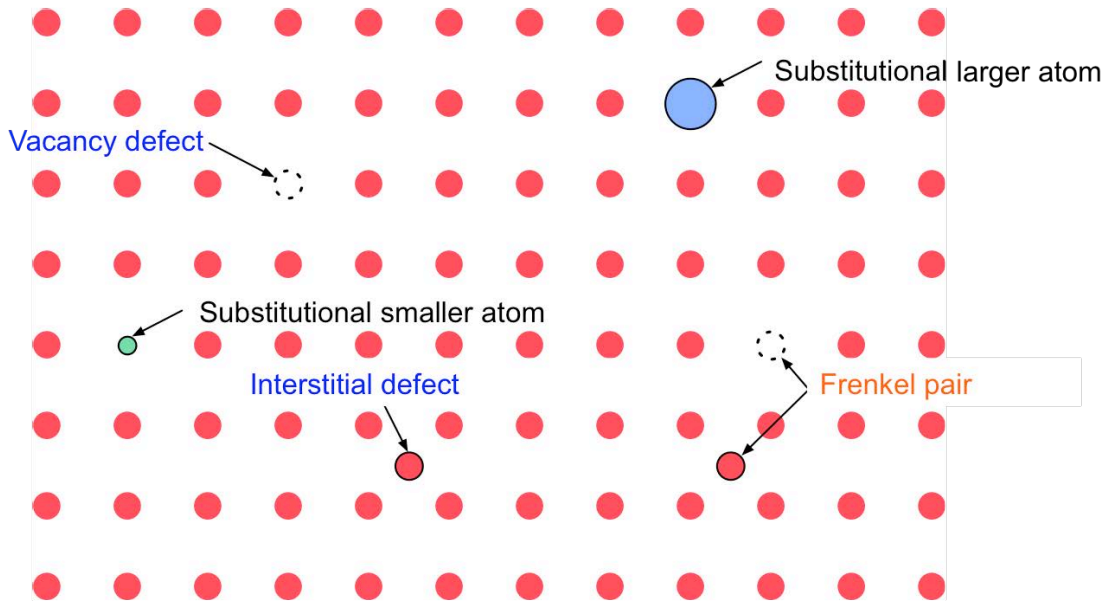

Figure 2.1 Illustration of point defects within a crystal lattice.

2.2.1 Surface (Planar) Defects

Surface defects can evolve into existence between two different boundaries of the same or different materials. The surface between the grain boundaries can have high concentration of defects because the crystal lattices of the adjoining grains are

differently orientated. The actual surface (the boundary between the crystal and ambient air) is also considered to have surface defects because the bonds of the crystal are terminated abruptly leaving the bonds 'dangling' as shown in Figure 2.2. A surface defect also exists between different materials neighboring each other, as the crystal structure is different and the interface between cannot be bonded perfectly. Deposition of different material such as SiO_2 on a Ge surface and the resulting interface with high surface defects would be an excellent example.

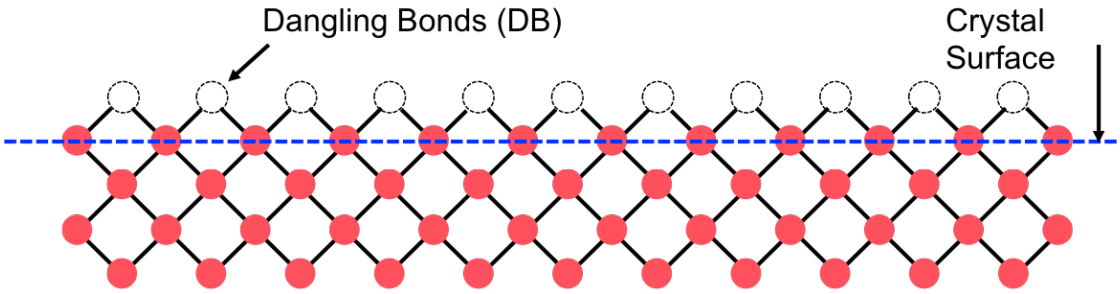

Figure 2.2 Illustration of dangling bonds in between the crystal surface and ambient environment. The abrupt termination of the bonds on the surface leaves the bonds 'dangling,' giving rise to allowed energy states in the bandgap acting as recombination sites for electrons and holes.

2.3 Electrical Characteristics of Defects in Germanium

2.3.1 Electrical Properties of Point Defects

Beside their structural irregularities, point defects introduce energy levels in the Ge bandgap. Substitution impurity atoms such as boron (B) and phosphorus (P) introduce an energy level near the valance band and the conduction band of Ge, respectively, thereby acting as an acceptor site or donor site. With this method we can accurately control the amount of impurity atoms that are added to Ge, this is what enables the doping phenomenon in Ge. However, vacancies and interstitial atoms also introduce energy levels in the Ge bandgap. Although there are some controversies on where exactly their energy levels lie within the Ge bandgap, it is generally concluded that vacancy introduces an energy level at 0.20 eV above the valence band and self-interstitial atom presents an energy level at 0.04 eV [3] below the conduction band as shown in Figure 2.3 (referenced from [3]). Defect levels introduced by vacancies present a source of degradation for Ge based MOSFETs, for they tend to be the main source of current leakage and n-type dopant deactivation phenomenon, which will be further explained in detail in the later chapters. This is especially the case because vacancies tend to travel to the surface while interstitials travel deep into the crystal bulk. Since MOSFET device operate near the surface of Ge crystal, it is more severely affected by presence of vacancies.

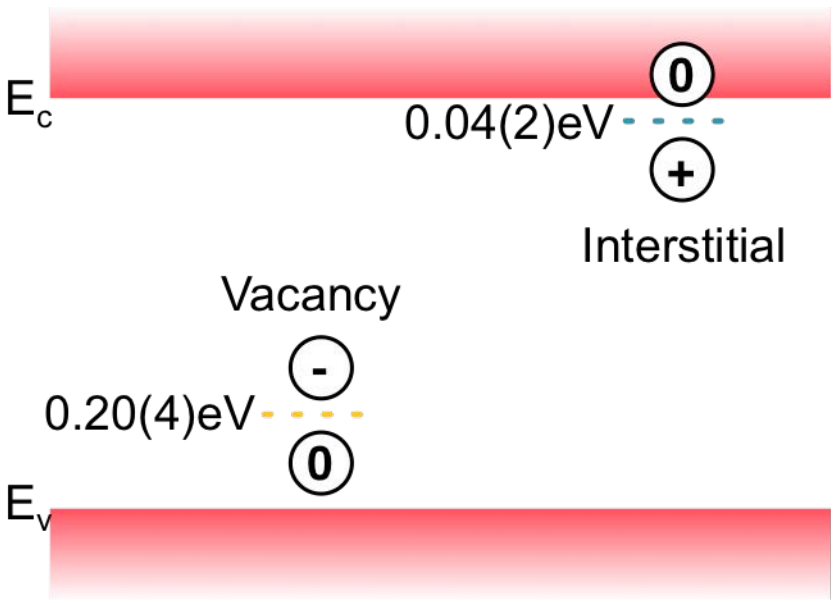

Figure 2.3 Energy states produced by vacancy and interstitial defects within the band gap of Ge and their position relative to valence and conduction band [3].

2.3.2 Electrical Properties of Surface Defects

Abrupt termination of Ge bond in the surface of crystal usually leads to the presence of dangling bonds (DBs). To elaborate, DBs in semiconductor results from an incomplete covalent bonding, where one side of the two atoms forming a covalent bond has one or more bonding sites than the other, resulting in a vacancy spot in the system. High density of DBs in a semiconductor device causes considerable degradation in its performance; they act as recombination sites, which reduce the lifetime of the carriers within an optoelectronic device and increases gate current leakage in a MOSFET. They also increase carrier scattering in the gate interface,

therefore reducing channel carrier mobility and might retain a fixed charge, which changes the threshold voltage.

2.4 Previous Efforts in Passivation of Defects in Germanium

Bulk defects in Si didn't impact the Si-MOSFET performance significantly, but it still remained as a source of junction leakage [9], for vacancy sites acted as recombination sites for the carriers. It also degraded the carrier lifetime [10], which was important for solar cell applications. Still, because most of the bulk defects can be annealed out at high temperatures over 900°C [11], which is around the typical dopant activation temperatures for Si MOSFETs, passivation of bulk defects did not draw too much attention to Si community. However for Ge, the impact of bulk defects was found more severe than Si counterpart. The main problem was that these bulk defects couldn't be annealed out completely. Little effort has been done to passivate these bulk defects. This dissertation provides one of the early reports in their passivation.

For surface defects, despite the excellent quality of Si/SiO_2 interface by thermal oxidation, Si based MOSFETs had DBs that was high enough to hinder the continuous scaling of Si based MOSFETs. However, as luck would have it, the Si based MOSFET community soon found that most of these DBs can be passivated by incorporating hydrogen. Forming gas that consists of nitrogen and hydrogen mixture significantly decrease the DB concentration by forming Si-H bond [12]. When the

research community was dealing with Ge again in 30 years later or so, they hoped that their accumulated knowledge in handling Si DBs with hydrogen passivation would help in terms of decreasing DB concentration in Ge. Although it was found that hydrogen passivation somewhat decreases the interface defect states, it was found experimentally, that the amount of improvement was not significant. Weber et al [13], also found that the bonds between Ge and H were too weak to be stable and would not significantly contribute to the passivation of interface defects. Therefore, many alternative methods of Ge interface passivation have been researched recently using oxygen [14], ozone [15], sulfur [16], and fluorine [17], [18]. Especially, high-pressure oxygen annealing by Takagi et al [7], shows promising results for Ge based MOSFET gate stack. Although fluorine has already been attempted for the application to passivate defects in Ge MOSFETs, results are yet to be seen.

Chapter 3

Fluorine Passivation of Vacancy Defects in Bulk Germanium

3.1 Introduction

Vacancy defects (V_{Ge}) in general can cause various problems in Ge based MOSFETs. When present in the source and drain (S/D) junctions, they act as recombination sites that increase the substrate leakage. In the channel region, they act as scattering centers degrading the carrier mobility. Particularly for n-type doped Ge regions, they cause deactivation of dopants that results in a lower carrier concentration than the chemical concentration [19]. They also enhance n-type dopant diffusion, making it difficult to achieve an ultra shallow junction [20]. For MOSFET fabrication,

ion-implantation process is a standard practice and during this stage, high concentration of V_{Ge} can be produced. Thus, for performance enhancement of Ge-based devices, it would be beneficial if these defect sites can be passivated. There are numerous studies showing decrease of vacancies when fluorine (F) is incorporated into silicon [21]-[23]. For the case of Ge, A. Chroneos et al. [24] have shown theoretically that F can form a strong bond with vacancies present in Ge, therefore can be used for passivation. However, experimental work is lacking in this area.

The aim of this work is to characterize and verify that vacancy defects in Ge can be effectively passivated by F incorporation. First, the electrical role that vacancy defects play by generating acceptor states in Ge was verified by intentionally creating the defects in an epitaxially grown Ge substrate. Next, thermal annealing was conducted to observe the annealing behavior of the vacancy sites. Finally, effect of F incorporation on the electrical behavior of the vacancy defects was investigated. Based on spreading resistance probe (SRP) measurements, we report a clear indication that not only F can passivate the vacancy defects that were intentionally created but also can reduce the native vacancy defect concentration present in as-grown epi-Ge.

3.2 Fabrication of Vacancy-Rich Ge Samples and Incorporation of Fluorine

For sample fabrication, undoped Ge films were grown heteroepitaxially [25] on a p-type Si to a thickness of ~1.7 μm. After the growth, ~20 nm of low temperature

silicon oxide (LTO) was deposited on top of Ge layer in order to prevent surface damage during the ion-implant step. For the first part of the experiment, Ge ions were implanted into Ge substrate at energy of 180 keV with three different doses of $1x10^{13}$, $1x10^{14}$, and $1x10^{15}$ ions/cm^2, respectively. The implant energy was chosen such that the defects are created well below the surface of Ge for reliable observation. Because Ge is a relatively a heavy element, 180keV was required to place the peak concentration depth at ~ 60nm within the Ge film. These as-implanted samples then went through SRP measurement to trace the defect trails in the substrate. If the vacancy defects exhibit acceptor type level within the band gap, the SRP will result in a trail of p-type carrier concentration. For the second part of the experiment, samples that were Ge ion implanted with $1x10^{15}$ cm^{-2} dose were annealed at three different temperatures of 400 °C, 500 °C, and 600 °C using rapid thermal annealing (RTA) tool for 10 seconds in a nitrogen ambient. These samples were again analyzed using SRP method to see if the vacancy defects can be effectively annealed out at high temperatures. The temperatures mentioned above were chosen because it is the typical range in which Ge based MOSFETs are fabricated. In the third part of the experiment, samples that went through Ge ion implant at 180 keV energy with a dose of $1x10^{15}$ cm^{-2} and 500 °C annealing were implanted with fluorine to a dose of $1x10^{14}$ cm^{-2} at 55 keV. The F dose and energy were chosen by using SRIM [26] simulation such that its peak is located at the peak of vacancy defect concentration (~80 nm) and has at least an order of magnitude higher peak concentration (~10^{19} cm^{-3}) than the amount of vacancy defect concentration present in the Ge film. Then the Ge-F implanted sample

went through a RTA process at 500 °C for 10 seconds in N_2 ambient. SRP analysis on as-implanted fluorinated sample and after RTA processed sample was done in order to assess the effect of F on the electrical activity of vacancy defects in the Ge film. In the last experiment, F was implanted into blank Ge film with a dose of $1x10^{13}$ cm^{-2} at 55 keV and was annealed at 500 °C for 10 seconds to see if F can further lower the native vacancy concentration present after heteroepitaxial growth of Ge on Si. Figure 3.1 illustrates all three parts of the experiment.

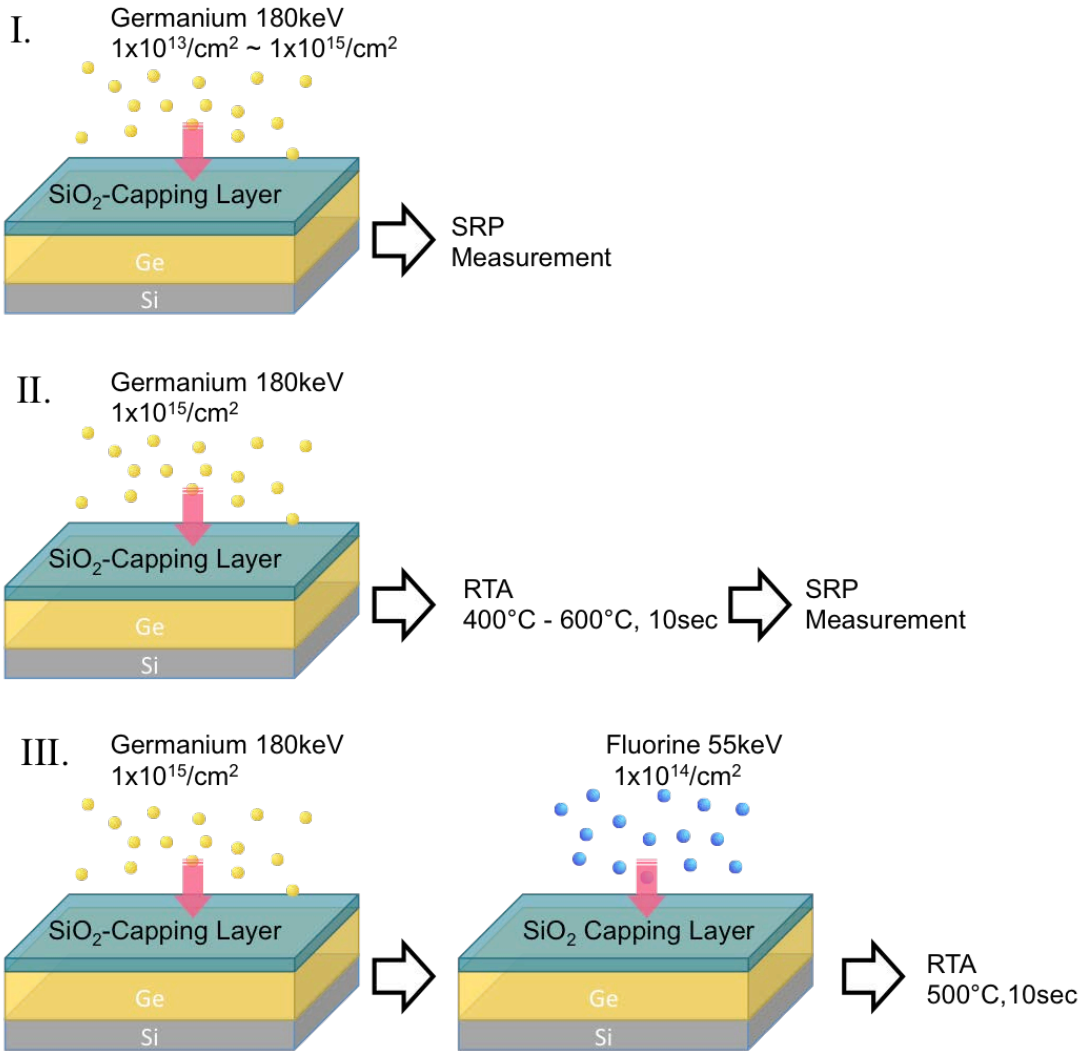

Figure 3.1 Fabrication of sample for three parts of the experiment on vacancy passivation by fluorine.

3.3 Electrical Characterization of Vacancy Defects in Germanium

As mentioned in the previous chapters, there are numerous works from different research groups that have investigated the electrical nature of point defects in Ge and it was shown that V_{Ge} introduces an acceptor-like charge state levels at 0.2 eV above the valence band [27]. Charge states for Ge self-interstitials (Ge_i) are controversial ranging from donor-like charge state levels between 0.02 and 0.06 eV below the conduction band [27] to 0.11 to 0.16 eV above the valence band[28]. There are also reports that Ge_i can exhibit electrically inert property[29]. Nevertheless, depending on the charge-state levels of defects and their concentration, these would act as if there are acceptors or donors present in the substrate. When Ge ions are implanted into Ge it would result in Frenkel pairs, which consist of i) V_{Ge} and ii) Ge_i. Because of this, the resulting effective carrier concentration and its type will be the sum of these two defects. Ideally, these Frenkel pairs recombine eventually and annihilate themselves out. But both V_{Ge} and Ge_i can be mobile with different speed, meaning that they can result in a spatial separation in the substrate due to ion recoil and preferential momentum[30]. In the case of Si, it leaves vacancies near the surface and interstitials deeper in the substrate. From this, we could expect for Ge the surface area to be p-type

due to V_{Ge} and depending on the Ge_i charge state, n-type concentration in the deeper region, especially the end-of-range (EOR) region. In Figure 3.2, SRP measurements of as-implanted Ge sample with three different doses ($1x10^{13}$, $1x10^{14}$, and $1x10^{15}$ cm^{-2}) of Ge ion are shown. When SRP measurements are done in conjunction with hot probe measurement[31] that can determine the type of the carrier in Ge samples ion implanted with Ge. V_{Ge} is expected to manifest as a trail of p-type carrier concentration at least for the surface region. Here, hot probe measurement confirms that all of the trails exhibit p-type carrier property. From this it can be deduced that Ge_i can be either neutral or a deep-donor state, which is hard to be ionized. The vacancy concentrations for all doses are below $1x10^{18}$ cm^{-3} range, with the lowest dose having the shallowest and highest peak concentration. This is counter-intuitive as we expect that more V_{Ge} will be created with higher dose. In addition, the surface region seems to exhibit lower carrier concentration despite the fact the ion implant damage profile should give a similar concentration level near the surface. However, this is believed to the artifact of amorphization of the Ge crystal that will give high resistivity values in the SRP analysis. Because SRP converts resistivity profiles into carrier concentration profile (assuming constant mobility), high resistance would translate into lower carrier concentration profile near the surface. This would also explain why the peaks (which is speculated to be the amorphous/crystal interface) are shifting deeper into the surface. At a higher dose more of the surface region would amorphize, which is confirmed by S. Koffel et al. [32], making it look as if the peak is shifting with higher dose. In fact, the value of suspected amorphized layer depth seen in the

SRP measurement (~100 nm, 150 nm, and 200 nm for $1x10^{13}$, $1x10^{14}$, and $1x10^{15}$ cm^{-2} dose, respectively) is similar to the work by S. Koffel et al. (~100 nm, 120 nm, 150 nm for $1x10^{13}$, $1x10^{14}$, and $1x10^{15}$ cm^{-2} dose, respectively), considering it was done at slightly higher energy of 180 keV instead of 150 keV (S. Koffel et al.). Thus, it is expected that when the amorphous layer starts to recrystallize with thermal annealing, the p-type carrier concentration by V_{Ge} would increase near the amorphous/crystal (a/c) interface.

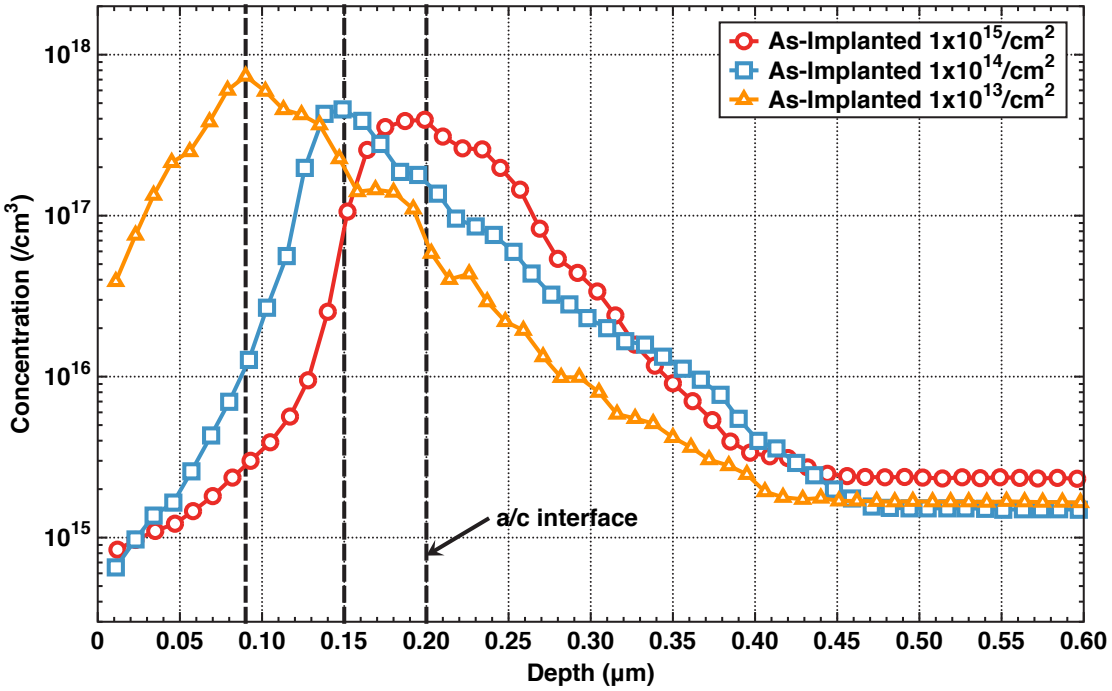

Figure 3.2 SRP profiles of Ge ion implanted Ge samples with three different doses of $1x10^{13}$, $1x10^{14}$, and $1x10^{15}$ cm^{-2}. All implants were done at 180 keV. Expected point of amorphous/crystalline interface is indicated as dashed lines.

To confirm this, SRP analysis is done on the samples with $1x10^{15}$ cm^{-2} dose which are annealed at three different temperatures of 400 °C, 500 °C, 600 °C and are shown in Figure 3.3. Since amorphous Ge is known to recrystallize at a temperature above 300 °C [33], there is a p-type concentration increase from the a/c interface after 400 °C annealing compared to the as-implanted sample. However, as the recrystallization process continues from the a/c interface to the surface, we also expect that V_{Ge} and Ge_i will recombine, being annihilated out during the process. This is clearly shown for samples that are annealed at 500 °C. As the surface layer recrystallizes, the effect of V_{Ge} manifests as increase in p-type carrier concentration while the peak value of the concentration is reduced from 400 °C annealed samples. Eventually at higher temperatures, V_{Ge} will be completely annealed out as the Ge atoms in the interstitial sites will combine with the V_{Ge} sites. It is shown in the SRP measurements that 600 °C annealing will completely recombine V_{Ge} with Ge_i in Ge and the carrier concentration is restored to the intrinsic level. However in many cases, 600 °C is considered as a high temperature processing regime for MOSFET and optical device fabrication in Ge. At this temperature n-type dopants will have diffused far into the substrate and other parts of the device, such as gate-stack, and cause degradation. In addition, presence of extrinsic dopants changes the behavior of V_{Ge} and Ge_i, implying that even at 600 °C the vacancies might not anneal out. That is where incorporating fluorine (F) can benefit the whole process. But to confirm this, we need to see that F incorporation can indeed reduce the V_{Ge} concentration in Ge. On the Ge sample that were dosed with $1x10^{15}$ cm^{-2} Ge ions and annealed at 500 °C, F ions

were implanted having 55 keV energy to a dose of $1x10^{14}$ cm^{-2}. Because it is believed that fluorine-vacancy (F_nV_m) cluster is more likely to form pure vacancy cluster based on binding energies [24], [34], [35], which are shown in Table 3.1, with proper annealing conditions, majority of the V_{Ge} sites could be passivated. In addition, the binding energy of F_nV_m is normally lower than of most of the dopant-vacancy pairs, suggesting that fluorination would be still effective under extrinsic doping. This is quite obvious considering that F is one of the materials with highest electronegativity.

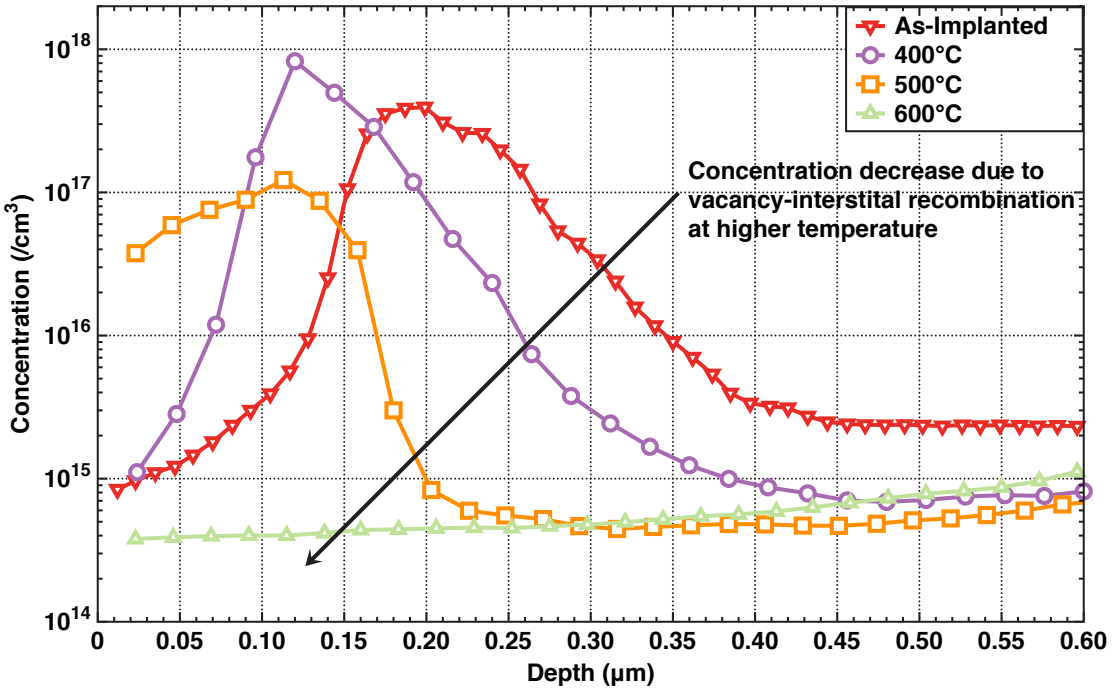

Figure 3.3 SRP profiles for different annealing conditions of 400 °C, 500 °C, 600 °C for 10 seconds in an N_2 ambient RTA. Here, Ge sample that was dosed with $1x10^{15}$ cm^{-2} Ge ion was used.

Defect Pair	Binding Energy (eV)
B-V	0.32[a]
Ga-V	-0.15[b]
In-V	-0.96[b]
P-V	-0.52[a]
As-V	-0.6[a]
Sb-V	-0.7[b]
F-V	-1.19[c]
F_2-V	-2.22[c]
F_2-V	-3.27[c]
F_4-V	-5.00[c]

[a]Reference 16.

[b]Reference 17.

[c]Reference 6.

Table 3.1 Binding energies of various dopant-vacancy pairs in Ge.

In Figure 3.4, SRP measurement are taken for as-F-implanted sample and F implanted sample that has gone through 500 °C annealing. In the as-F-implanted

sample there is an increase of p-type carrier concentration than the non-F-implanted control sample. However, this is not an unexpected result since F ion-implant process will create damage resulting in vacancies. Because F is a smaller and lighter atom than Ge, it induces fewer defects and hence does not amorphize the surface. This results in high p-type carrier concentration level (~10^{18} cm^{-3}) at the surface. To incorporate F into the vacancy sites, 500 °C RTA was done. According to the SRP results, incorporation of F gives a huge reduction of three orders of magnitude in V_{Ge} concentration. This is an indication that F is indeed effective in V_{Ge} passivation. In this aspect, it is plausible to presume that when F is introduced to virgin Ge substrate with no intentionally added V_{Ge}, it might even further reduce the background p-type concentration. To verify this, a light dose of $1x10^{13}$ cm^{-2} was added to virgin Ge substrate and was annealed at 500 °C. SRP measurement indicates that the active p-type concentration is around $6x10^{13}$ cm^{-2} near the surface, giving confirmation to our expectation. This reduction of background carrier concentration can be most helpful when we are trying to achieve an intrinsic region in a p-i-n diode fabrication.

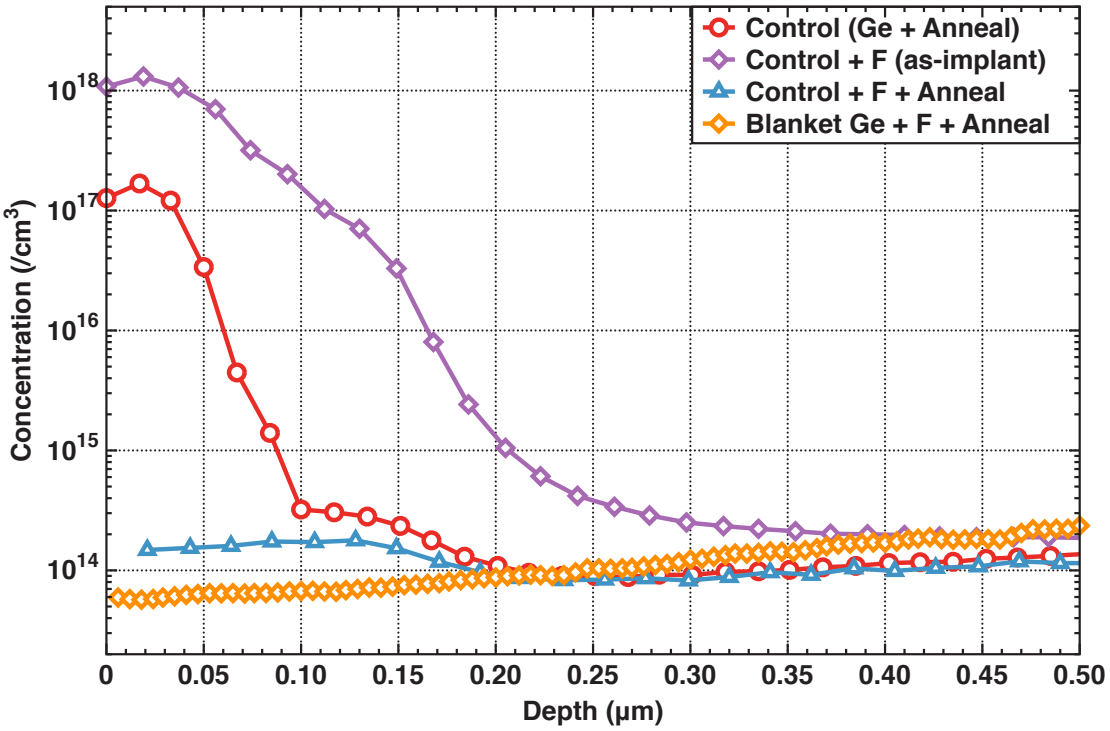

Figure 3.4 Effect of fluorine in passivating V_{Ge}. When F implanted sample is annealed, V_{Ge} is passivated and carrier concentration returns to the background p-type concentration. When F is implanted to a blanked Ge sample, it further reduces the background concentration.

3.4 Conclusion

In conclusion, it has been verified that vacancy defects in Ge indeed exhibit electrical characteristics of an acceptor. By using SRP analysis, we've confirmed that these defects have been shown to be present until 500°C annealing, while they are annealed out around at 600 °C. By incorporating F, these defects can be effectively passivated out even at 500 °C. This is important, because diffusion of n-type dopants

in Ge tends to be very fast above 600 °C, which makes it difficult to form a shallow junction in a Ge-MOSFET. Additionally, when F is incorporated into epitaxially grown intrinsic Ge, it further reduces the vacancy concentration, making it closer to being intrinsic. This passivation method can be used to further improve the performance of Ge based MOSFETs and p-i-n diodes, passivating out the vacancies in the junctions and the intrinsic region. This method also has potential of reducing the concentration of dangling bonds in the surface of Ge, thereby brining improvements in channel mobility and metal to S/D contact.

Chapter 4

Enhanced Activation and Suppressed Diffusion of Phosphorus by Fluorine in Germanium

4.1 Introduction

To date, it is a major challenge to achieve ultra-shallow source/drain junctions with low parasitic resistance in Ge n-MOSFETs. For p- MOSFETs, this would not be a difficult task to solve, because p-type dopants such as boron (B) have very low diffusivity in Ge [36] and can achieve high electrical activation. However this is a different story for n-type dopants such as phosphorus (P), arsenic (As) and antimony

(Sb). Studies indicate that vacancies (V_{Ge}) in Ge created during ion implant of n-type dopants in Ge, i) form electrically neutral donor-vacancy (D_nV) pairs that reduce the amount of electrically active dopants in Ge[19], and ii) facilitate enhanced diffusion[20] of dopants making it hard to achieve ultra-shallow junction. Achieving electrically active high dopant concentration level in Ge is motivated in order to lower the contact/series resistance in the n^+/p junction and for achieving efficient light emission from Ge for laser [37] and other optoelectronic applications [38], [39]. Activation study of n-type dopants by Chui et al.,[40] indicates the activated dopant fraction decreases as P implant dose increases and the achievable electrically active concentration of P by thermal annealing is limited to ~$5x10^{19}$ /cm^3. Recent work by Kim et al. [41] demonstrates the reverse correlation between dopant activation and number of V_{Ge} created by ion-implantation. Thus, it is plausible to conclude that in order to achieve high n-dopant activation and shallow junction, the concentration of V_{Ge} needs to be reduced. Many studies have shown decrease of vacancies when fluorine (F) is incorporated into silicon[21]-[23]. A. Cheronos et al. [24] have also predicted theoretically that presence of F might be able to form a stronger bond with V_{Ge} present in Ge, achieving higher activation and retardation of dopant diffusion. Our recent work [42] has also shown strong evidence that V_{Ge} can be effectively passivated by F in an undoped Ge. However, reduction of vacancies in an extrinsically P doped Ge is yet to be seen.

In this work, we aim to achieve both higher activation level and less diffusion by passivating the V_{Ge} defects in P doped Ge using F. First, we design the experimental parameters such as ion implant energy and dose of P and F by using SRIM [26] and mass action analysis. Investigation of dopant activation level and depth of diffusion is done by spreading resistance profiling (SRP) and secondary ion mass spectroscopy (SIMS) analysis. In addition, the crystalline quality of the samples that is related to amount of V_{Ge} in the system is examined by Raman spectroscopy. Through these results, clear indication that F not only increases total fraction of activated dopants in Ge but also retards the dopant diffusion is presented.

4.2 Fabrication of Vacancy-Rich Germanium

For our experiments, undoped Ge was first heteroepitaxially deposited [25] on (p-type (100) Si (0.1~0.9 ohm-cm) with a thickness of ~1.7μm. After Ge deposition, ~20nm of low temperature silicon oxide (LTO) was deposited on top of the Ge layer. The purpose of this thin oxide layer was to prevent the surface damage caused during the ion-implant process. After oxide growth, samples were implanted with P with $1.8x10^{15}/cm^2$ dose and at 90keV energy. The energy was chosen such that the peak concentration is approximately located 80nm below the Ge surface. Such deep implant depth was chosen to decouple the effects of out-diffusion and segregation in the surface region with the effect of F. After P implant, the samples were split into four groups and each was ion-implanted with different F dose: i) zero dose (control group), ii) $1x10^{14}/cm^2$ (low dose), iii) $1x10^{15}/cm^2$ (medium dose), and iv) $5x10^{15}/cm^2$ (high

dose). The sample groups are summarized in Table 4.1. Groups with F were all implanted with 55keV energy, which brings the peak of the F to the same depth as that of P peak concentration. All the dose and energy of the implants were designed based upon SRIM simulations. After subsequent ion-implant of P and F, all the samples were annealed for 10 sec by using rapid thermal annealing (RTA) equipment in N_2 ambient at 500°C. After stripping off the oxide by 2% HF solution, chemical and electrical dopant concentration of the samples were mapped as a function of depth by SRP. For definite study of retardation of P diffusion by F, SIMS analysis was done on samples in Table 4.1, which were additionally annealed at 500°C for 1 hour. For crystalline quality examination, Raman spectroscopy was used.

Sample Group (#)	Ion Species	F Dose (/cm^2)	Energy (keV)
1	P	$1.8x10^{15}$	90
2	P + F	$1.8x10^{15}$(P)+$1x10^{14}$ (F)	90 (P) / 55 (F)
3	P + F	$1.8x10^{15}$ (P)+$1x10^{15}$ (F)	90 (P) / 55 (F)
4	P + F	$1.8x10^{15}$ (P)+$5x10^{15}$ (F)	90 (P) / 55 (F)

Table 4.1 Ion Implant conditions for phosphorus and fluorine co-implant process. Phosphorus implant conditions are fixed and only fluorine dose is varied for the purpose of investigating its effect on vacancies.

4.3 Dopant Activation Enhancement of Phosphorous by Fluorine Passivation in Germanium

4.3.1 Theoretical Analysis of Vacancy Defect Passivation by Fluorine

Estimation of V_{Ge} concentration levels created by P implant in Ge is important to determine the amount of F dose needed for passivation, for overdose of F implant would create additional unwanted damage to the Ge crystal even though F is smaller and lighter element than P. For all experiments, P implant dose was fixed to $1.8x10^{15}/cm^2$ that would give peak concentration close to the maximum solid solubility of P in Ge ($1\sim2x10^{20}/cm^3$) in an as-implanted state. To first order, the peak concentration of the V_{Ge} present after this P implant (creation of V_{Ge} defects) and subsequent activation anneal (limited reduction of vacancies) was assumed to be around $5x10^{19}/cm^3$, based on previous studies showing only half activation of P dopants when the peak chemical concentration was determined to be $\sim1x10^{20}/cm^3$. Then, it can be roughly estimated that at least equal amount of F is needed to passivate the vacancies. To see if this concentration scheme will work, mass action analysis by iterative method was carried out. This analysis can map out the relative concentration of vacancy [V] to passivated F-V pairs [F_nV_m] at a given temperature. This relation[24] is given by

$$\frac{[F_nV_m]}{[F]^n[V]^m} = \exp\left(\frac{-E_b(F_nV_m)}{k_BT}\right) \quad (1)$$

where E_b is the binding energy of F_nV_m pair ($0 \leq n \leq 4$, $1 \leq m \leq 6$) that is likely to form, k_B is the Boltzman's constant and T is the temperature. The initial [F] and [V] concentrations were both set to $5x10^{19}/cm^3$ based upon the previous discussion. The binding energies used in this study were referenced from work by Chroneos et al [24]. As a note, the effect of P-V and P-F bond was not considered in the calculation, as the binding energy of this bond is higher than that of most F-V complexes. Figure 4.1 shows the relative concentrations of these complexes at temperature ranging from 300°C to 700°C, which is the usual range in Ge device fabrication. In this figure, we can see that for dopant activation temperature of 500°C, V_{Ge} concentration is reduced from its initial value of $5x10^{19}/cm^3$ to around $\sim 1x10^{18}/cm^3$ and most of the V_{Ge} combines with F to form F_nV_m complex. Although we can increase the F dose in the system to ensure all the vacancies are passivated, this is difficult in real experimental conditions using ion-implantation as higher dose of F means higher V_{Ge} due to the F implant itself. In addition, loss of F by out-diffusion during activation anneal has to be considered. Therefore, in order to avoid excessive damage by F implant and compensate for the out-diffusion, F implant dose was varied from low ($1x10^{14}/cm^2$) to high dose ($5x10^{15}/cm^2$).

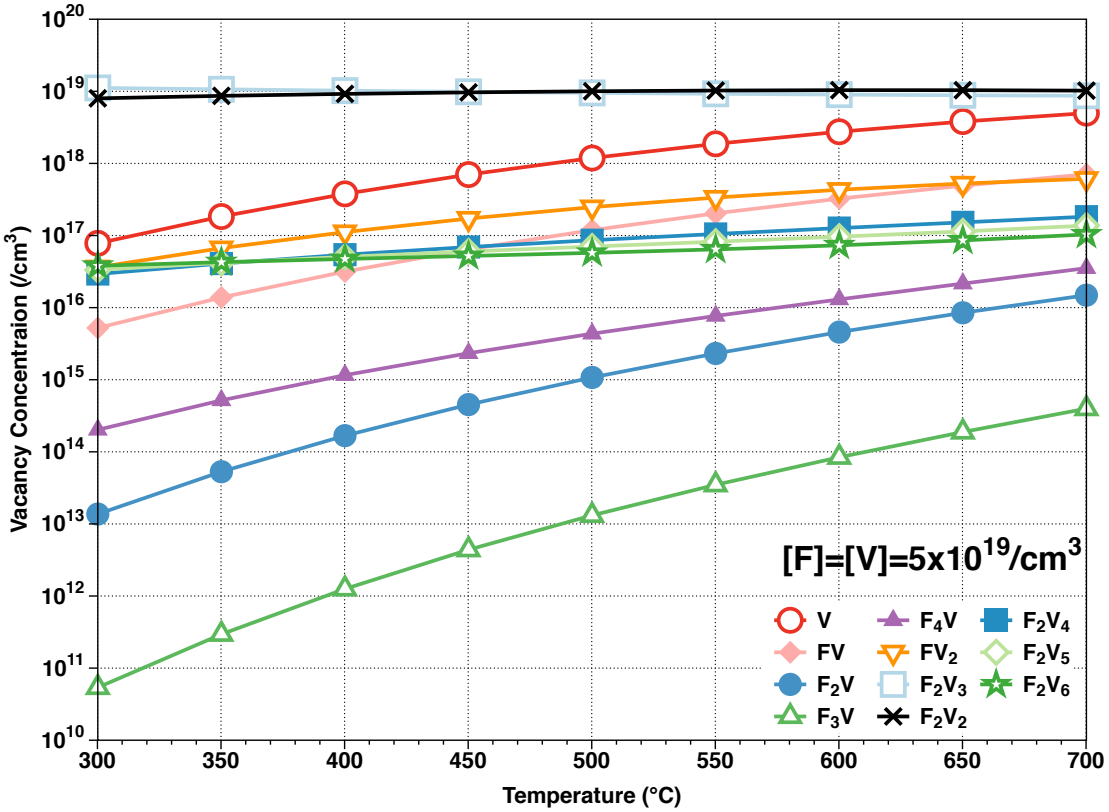

Figure. 4.1 Relative concentration of vacancies and fluorine-vacancy complexes vs. temperature. It can be seen that for our annealing temperature of 500 °C, vacancies are expected to be mostly passivated.

4.3.2 Experimental Analysis of Fluorine Passivation with One Step Annealing

To investigate the dopant activation effect by F in extrinsically doped (in our experiment, P) Ge, SRP analysis is performed for the four groups of samples shown in Table. 4.1. Figure 4.2 shows the SRP results for control sample and fluorinated samples. Here, sample with low F dose ($1x10^{14}/cm^2$) shows around ~2x improvement

in peak electron concentration (~$1x10^{20}/cm^3$), indicating that F passivates V_{Ge} in the region thereby enhancing the amount of active P concentration. As the F dose is increased to medium level ($1x10^{15}/cm^2$), we observe that in terms of peak concentration F is still effective in enhancing the dopant activation. If the F implant dose is increased to even higher ($5x10^{15}/cm^2$) range, degradation of dopant activation indicated by large deactivation at and near the surface leading to lower carrier concentration level than the control sample is observed. The reason for this is thought to be from increased damage to the sample during the F implant. Because we are implanting F dose ($5x10^{15}/cm^2$) that is even larger than the P dose ($1.8x10^{15}/cm^2$), there is a possibility that the introduced F concentration is not enough to passivate the V_{Ge} created during both P and F implants. Additionally, there is also a possibility that with $5x10^{15}/cm^2$ the Ge crystal is damaged to the point where the damage cannot be fully removed with annealing [43].

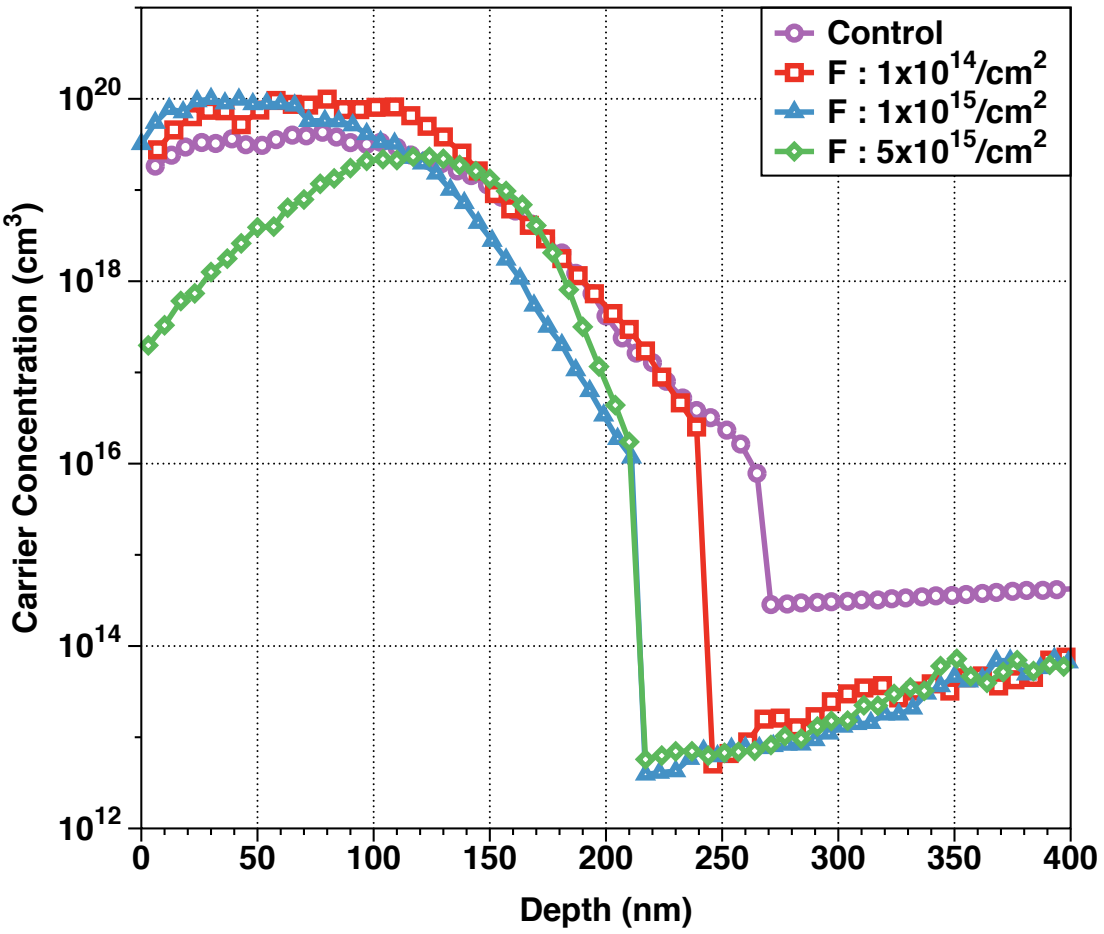

Figure 4.2 SRP profiles for samples in Table 4.1. Fluorine is mostly effective in passivation at low dose, while higher dose gives lower activation than even in the control sample.

SIMS is used to identify the chemical doping profile of F in the three groups of samples (Table 4.1) and is shown in Figure 4.3. Here, we see that in Region I, F is easily out-diffused or segregates to the oxide during annealing, leaving little amount of F to passivate the vacancies. This trend of out diffusion has also been report by

Impellizzeri et al. [44]. Notice that even with only 10sec of annealing at 500 °C, we observe 50%~90% of F is lost. The sharp dip or rise of concentration on the surface is speculated to be the remnant of SIMS inaccurate measurement due to mass interference [44]. Another interesting thing to mention is that there is a pile-up of F in the 150 nm – 250nm region. This pile-up is very similar to what Impellizzeri et al. [44] reported, where they explain that this is due to end-of-range (EOR) defect region that becomes more stable with the presence of F.

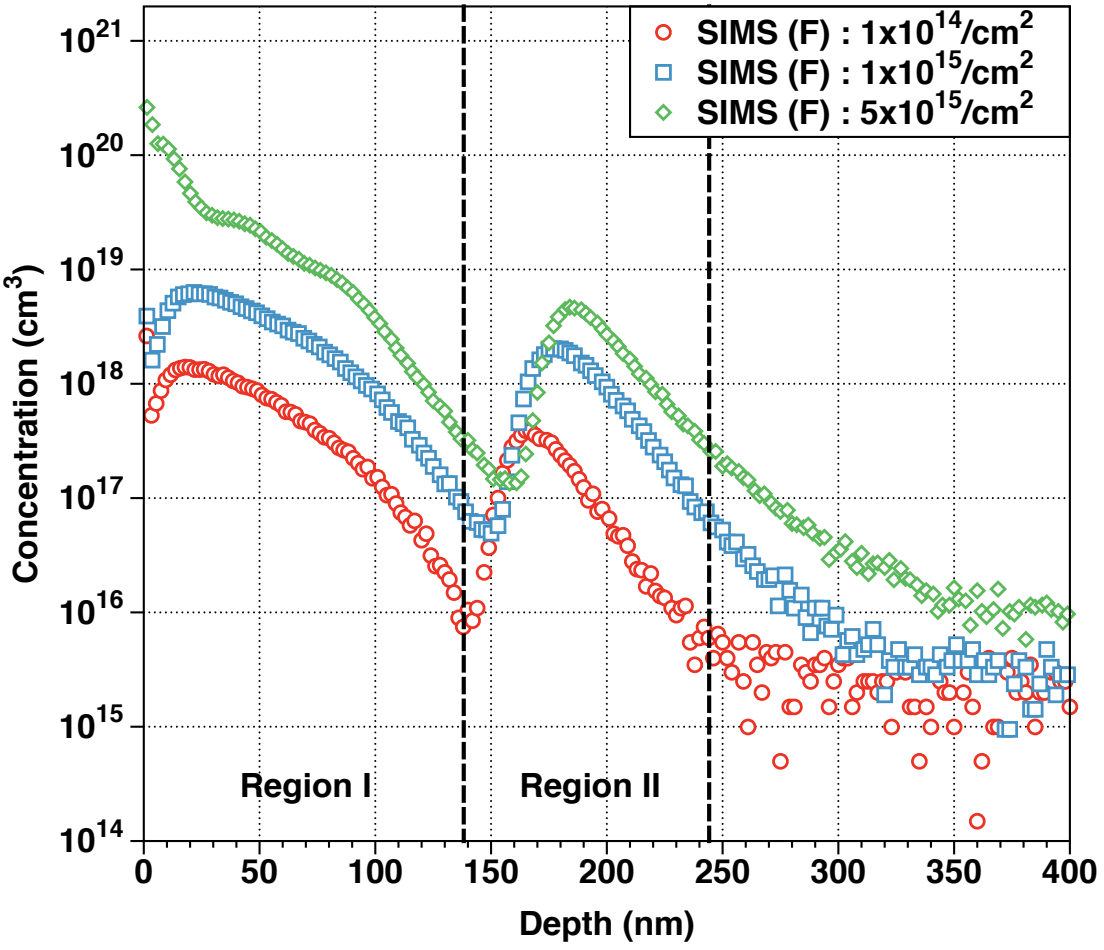

Figure. 4.3 SIMS profile of fluorine in the samples in Table 4.1. Notice that there is a huge out-diffusion of fluorine making difficult to have the right amount for passivation.

Effectiveness of F in enhancing the dopant activation is shown in Figure 4.4, by displaying the fraction of dopant that is activated compared to the total chemical concentration of the dopant present in the sample. For the control sample where the dopant has been activated without F, we obtain similar degree of activation reported from other literature [40]. As for the samples with F, we observe an increase of activation level up to ~50%. However, the level of activation decreases lower than the control sample at high F dose, which can be attributed to large V_{Ge} creation due to F ion implant. In this case, the implanted F concentration might not be sufficient to passivate all the vacancies. Therefore, we conclude that total accumulated V_{Ge} created from both P and F implants is a major consideration factor in achieving high activation rate by F passivation. In this logic, we can expect that relative effect of dopant activation enhancement using F compared to the samples with no F will be small for lower P implant dose. This is evident in Figure 4.5, where we compare dopant activation with varying P dose with fixed F dose of $1x10^{14}/cm^2$. If we compare this to earlier works by Chui et al. [40] which shows that P activation decreases with increased dose, sample with F shows great activation enhancement in the high dose regime ($\sim 1x10^{15}/cm^2$), whereas the activation level is slightly higher for low dose regime ($\sim 1x10^{14}/cm^2$).

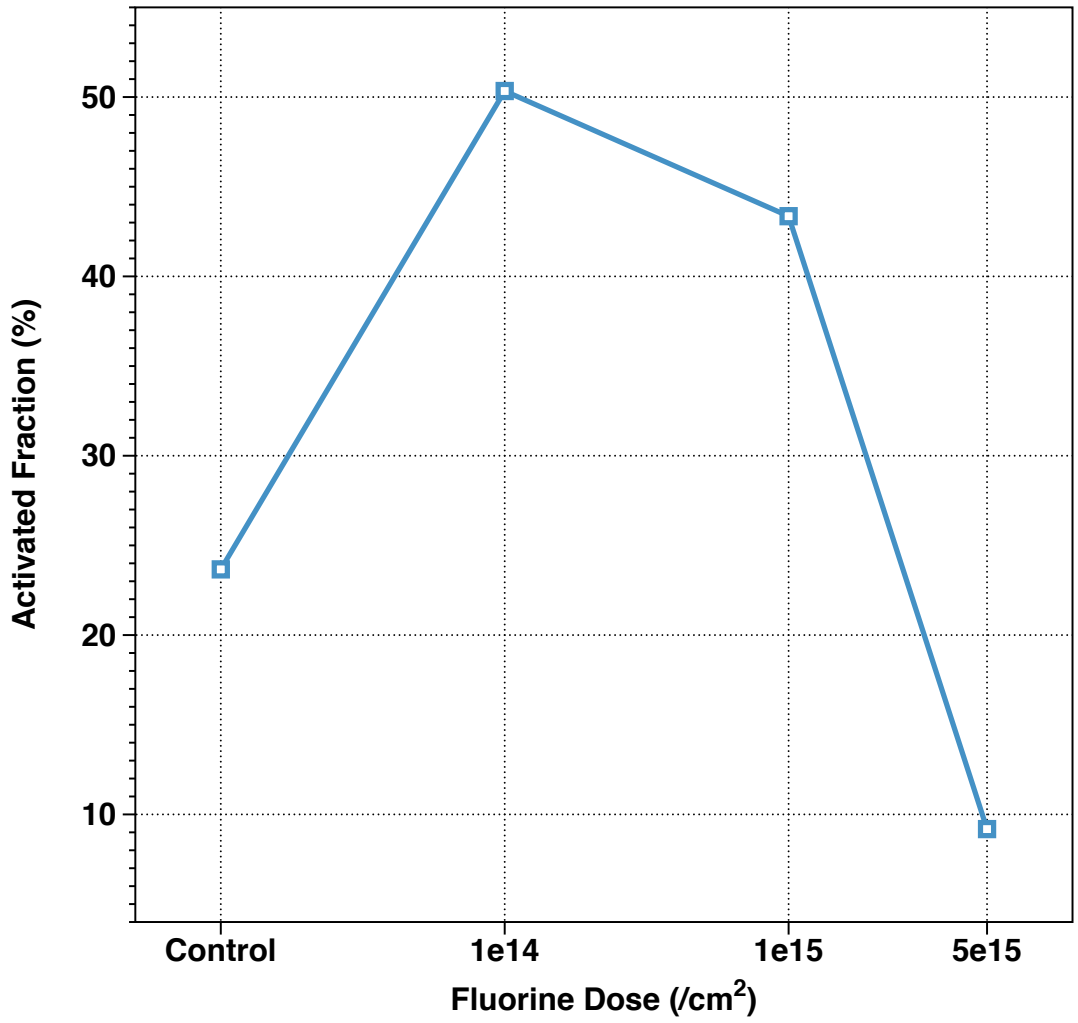

Figure 4.4 Activated fraction of phosphorus dopant extracted by comparing the total amount of dopant present in SIMS and electrically activated amount by SRP.

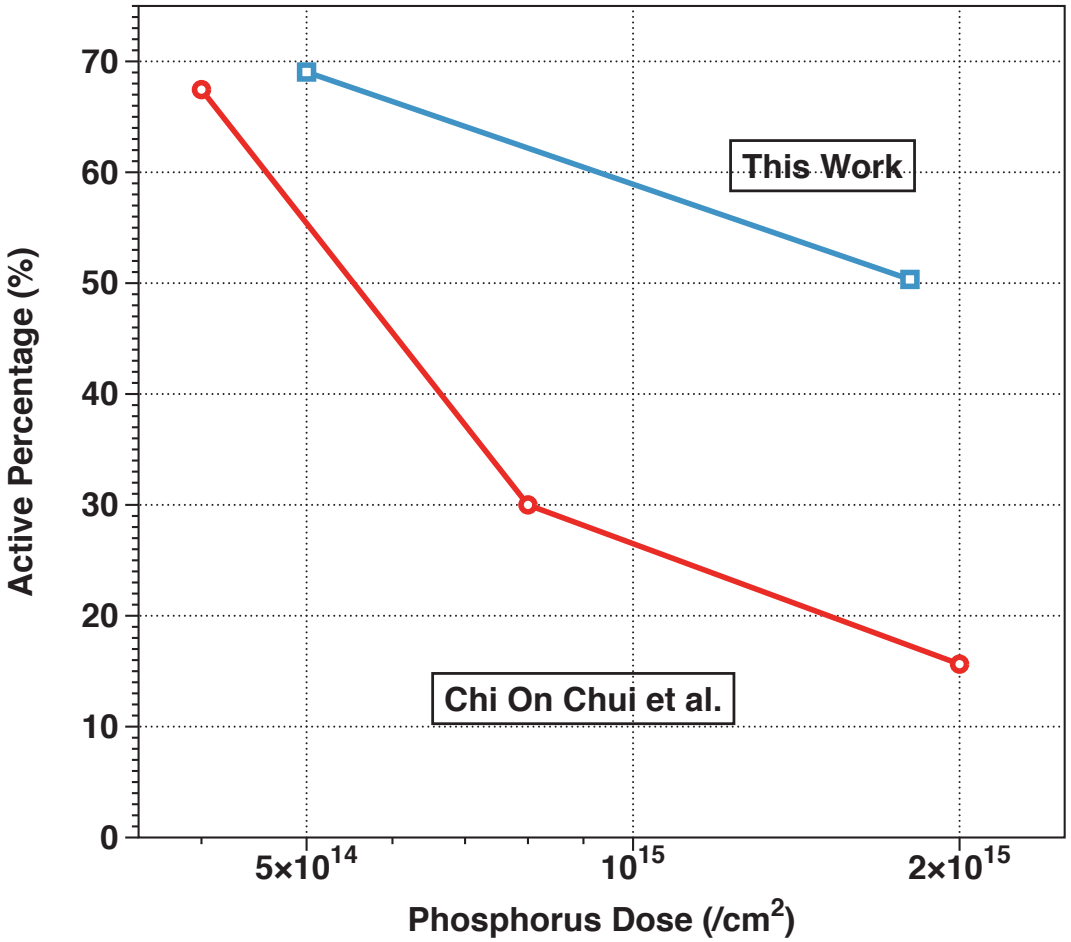

Figure 4.5 Activation level when the fluorine dose is fixed to $1x10^{14}/cm^2$ and the phosphorus dose is varied. We clearly see that fluorinated sample shows better activation than the reported value [7] for all dosage levels.

4.3.3 Experimental Analysis of Fluorine Passivation with Two – Step Annealing

In the previous section, incorporation of F was done right after the P implant step. This means that Ge was fortified with damage when F was ion-implanted, which could

enhance the out-diffusion process leading to poor activation percentage. As we've discussed in the previous section, Figure 4.5 suggests that even though small improvement in terms of dopant activation can be achieved with low-damage (low-dose) samples, the overall activation can be increased to further extent. By reducing the amount of damage before the fluorine ion-implantation, it can be expected that higher dopant activation can be achieved. One way of doing this is to anneal the sample right after the P implant, (1^{st} implant) which would reduce the vacancy defects in the sample considerably, as discussed in Chapter 3. For verification, the following sample groups shown in Table 4.2 are prepared and processed. Both 1^{st} and 2^{nd} annealing steps were done in an N_2 ambient for 10secs, and for comparison each group had a control sample; sample that went through both anneals but received only the first implant.

Sample (#)	1^{st} Implant	1^{st} Anneal (°C)	2^{nd} Implant	2^{nd} Anneal (°C)
A	P	500	F	500
B	P	500	F	600
C	P	600	F	500
D	P	600	F	600

Table 4.2 Ion Implant conditions for phosphorus and fluorine co-implant process. Phosphorus implant conditions are fixed and only fluorine dose is varied for the purpose of investigating its effect on vacancies.

Again, the activation fraction of P compared to the implanted dose is calculated and is shown in Figure 4.6. Overall for non-fluorinated control samples, dopant activation rate was limited to ~55% for sample that had a 600 °C annealing step. For non-fluorinated sample where the maximum thermal budget was 500 °C, dopant activation was similar to that of previously reported value [40]. As we have discussed in chapter 3, it seems for control samples with 600 °C annealing step, the vacancy defects were minimized thus achieving higher activation value than that of 500 °C anneal. However, because of un-annealed defects present in the surface, the activation rate is still limited to 55%. For sample group with F, best results are achieved for group B (~87.5%) and D (~81.25%), where the final annealing was done at 600 °C. The slightly lower activation of group D compared to group B can be explained through higher annealing time at 600 °C (20second in total) which would result in higher out-diffusion. Because the concentration of vacancy defect within the crystal was lowered by a thermal treatment before F ion implantation, total accumulated damage was less, making F more effective in passivating out the rest of the vacancies. However, if the final annealing was done at a lower temperature of 500 °C (group D), the level of activation showed only slight improvement (62.5%) over the control sample (55.6%). While the final thermal anneal at 500 °C is sufficient to initiate F to passivate the existing vacancies for group D, it seems it is not enough to passivate the vacancy defects created by F ion-implant to a significant level. Based upon this results, F passivation in conjunction with high annealing temperature of 600 °C gives best results in terms of dopant activation.

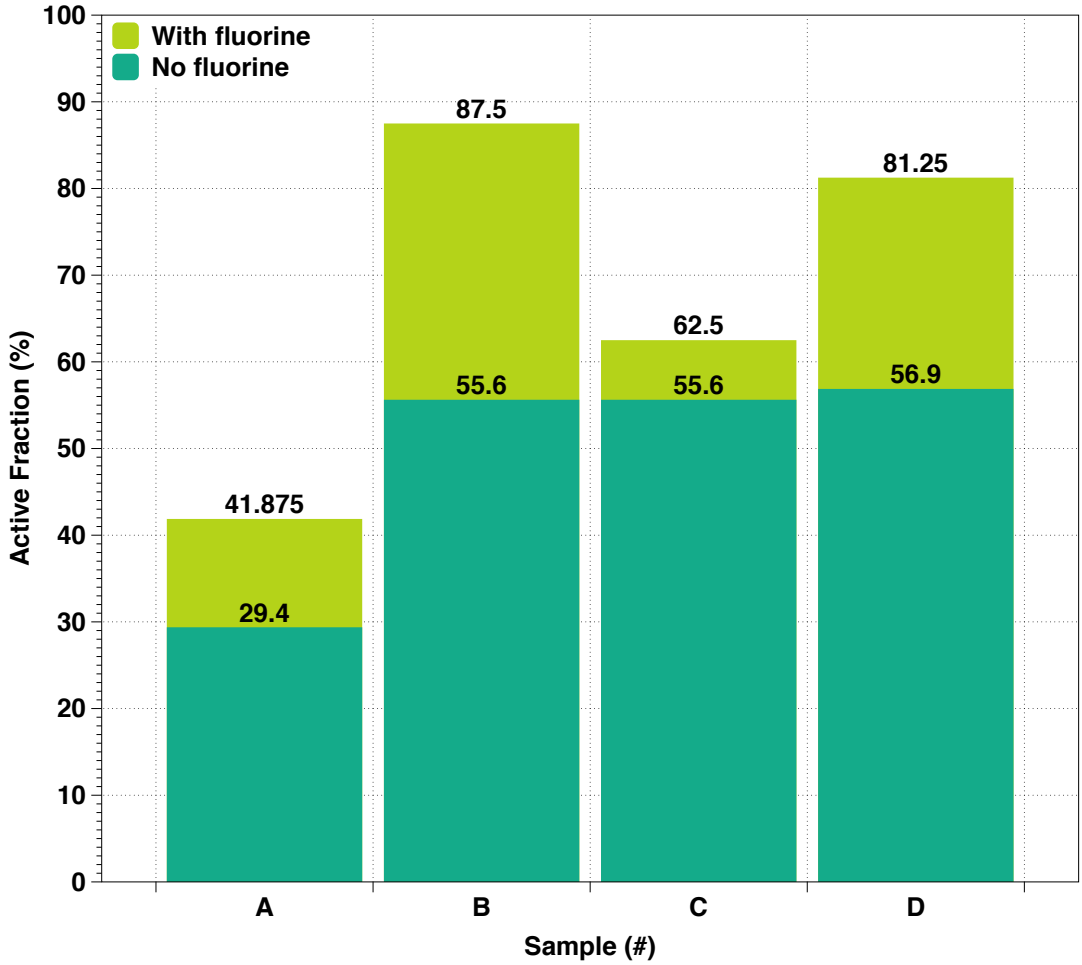

Figure 4.6 Activated fraction of phosphorus dopant extracted by comparing the total amount of dopant present in SIMS and electrically activated amount by SRP.

4.4 Suppression of Phosphorous Diffusion in Germanium by Fluorine

Even though SRP showed indication of diffusion retardation of P by vacancy site reduction using F, this cannot be conclusive without studying the junction depth in terms of chemical concentration. This is because different degree of dopant activation due to non-uniform V_{Ge} distribution by depth could give wrong impression of the actual junction depth. In addition, 10 seconds at 500°C anneal is not sufficient to see clear effects of diffusion. In theory, F passivation of V_{Ge} sites within the Ge lattice would prevent the P dopant from using it as a fast diffusion route resulting in a shallower junction. In Figure 4.7, SIMS analysis was used to identify the chemical doping profile of P for samples in Table 4.1, which have been additionally annealed for 1 hour at 500°C. For low and medium dosed F samples, the trend is as expected; less diffusion than samples with just P. Slightly deeper junction in medium dosed F sample compared to low dosed F sample can be explained by higher degree of F implant damage with similar degree of V_{Ge} passivation by F. Most intriguing result is the high dosed F sample, showing overall lower chemical concentration yet shallower junction than the P only doped Ge. The hypothesis of this is that because of extensive damage in the Ge crystal with high dose ($5x10^{15}/cm^2$) F implant, higher loss of P due to damaged enhanced out-diffusion might occur. This point is further solidified by the fact that there is a threshold of damage to the Ge crystal where damage becomes irrecoverable and large clustering of V_{Ge} occurs at the surface [43]. This would also explain the large deactivation of dopants for high F dosed samples in the SRP result.

But, because of the large amount of F implanted in the Ge lattice, it is still effective in suppressing the P diffusion at least in the deeper junction region where the V_{Ge} concentration is less than the surface, leading to shallower junction than the P only doped Ge sample. However, it seems that F is not able to passivate out the massive V_{Ge} in the surface region. Along with dopant activation enhancement, this gives proof that V_{Ge} reduction by F is affecting the P to diffuse less rapidly through the Ge lattice.

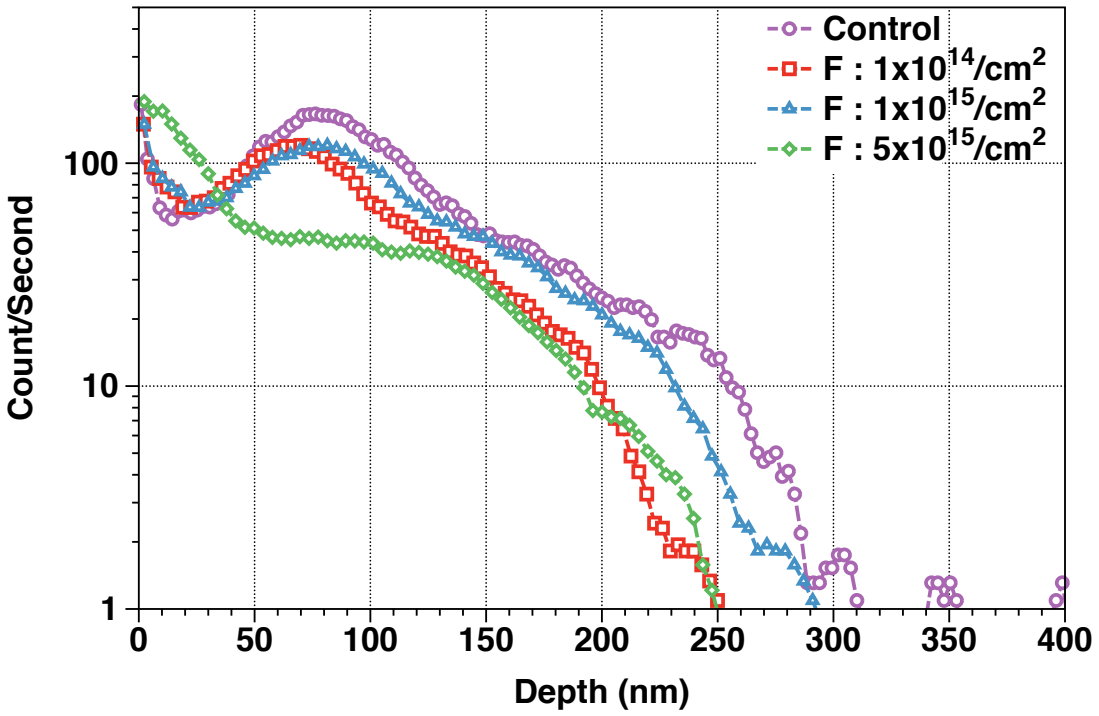

Figure 4.7 SIMS profile for samples in Table 4.1. Samples with fluorine give shallower junctions than the control sample indicating reduction of vacancies in Ge.

So far, this study was based on the assumption that V_{Ge} site reduction by F passivation is strongly correlated with dopant enhancement and diffusion retardation

of P. If so, crystalline quality inferred by Ramen spectroscopy would also have to concur with this assumption. By measuring the intensity and the full width half maximum (FWHM) value of the Raman spectra, crystalline quality can be indirectly inferred [45]. Because increased V_{Ge} sites (which is essentially a defect state in Ge) would also mean poor crystalline quality, lower intensity and higher FWHM value for P implanted sample can be expected. Figure 4.8(a) shows this trend clearly. Compared to virgin epi-Ge sample with no implant, P implanted sample exhibits lower Ge-Ge bond peak intensity and broader FWHM value located at 299 cm^{-1}, which is indication of poor Ge crystal quality. As a note, the discrepancy between the reported Ge-Ge peak value of 300 cm^{-1} [45] comes from 0.2% strain due to thermal expansion mismatch between Ge and Si during its epitaxial growth [46]. However, when $1x10^{14}$ $/cm^2$ ~ $1x10^{15}$ $/cm^2$ F is introduced in the system, the peak intensity and the FWHM is almost restored to the virgin epi-Ge value, indicating improvement in crystalline quality. The medium dosed sample ($1x10^{15}$ $/cm^2$ F) shows slightly lower peak intensity than the low dose ($1x10^{14}$ $/cm^2$) meaning that medium dosed F sample will have slightly higher V_{Ge} states. This is consistent with the SRP and SIMS results where medium dosed F samples have slightly lower degree of activation and deeper junction depth. Another interesting thing to note is the Raman spectrum for the highly dosed F ($5x10^{15}$ $/cm^2$) sample. For SRP and SIMS results, it was speculated that the lower activation and high out-diffusion was from extensive high-dose F implant induced damage. Raman spectra result supports this speculation for the lower peak intensity and broader FWHM value than the other fluorinated samples. Especially, the FWHM

value that is extracted and plotted in Figure 4.8(b) is the highest for F dose of $5x10^{15}$ /cm^2 indicating extensive Ge lattice damage. The shift in peak from 299 cm^{-1} to 298.5 cm^{-1} also suggests that high concentration of V_{Ge} is giving tensile strain to the lattice. Similar FWHM increase and peak shifting by heavy ion implant have also been observed by D. R. Myers et al [47]. Overall, the significance of this Raman analysis is that it verifies that level of defect (V_{Ge} state) in Ge is affected by F passivation, giving confirmation that it is indeed change in V_{Ge} defect levels that influences the level of P dopant activation and diffusion enhancement in Ge.

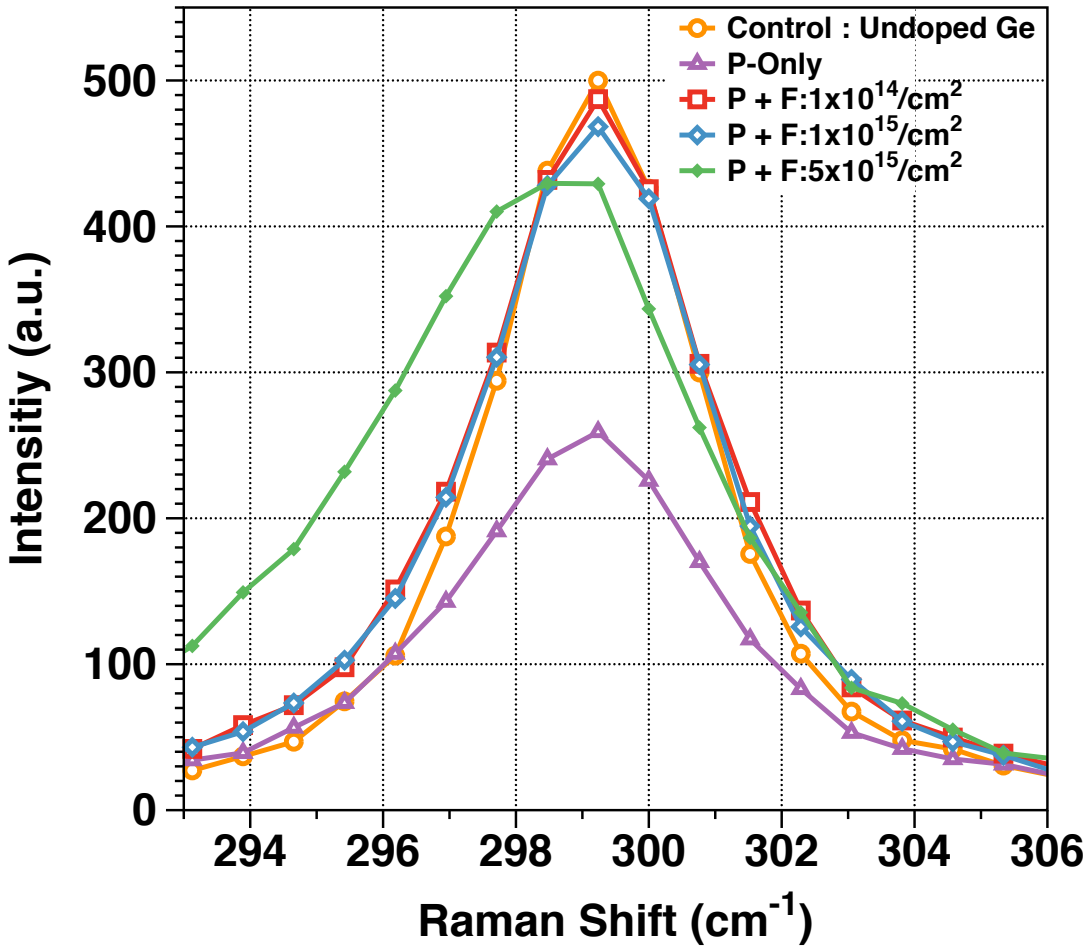

Figure 4.8 (a) Raman spectra of samples in Table. 4.1. With optimized amount, the fluorine treated sample can restore the Raman profile close to the undoped Ge with no ion implantation.

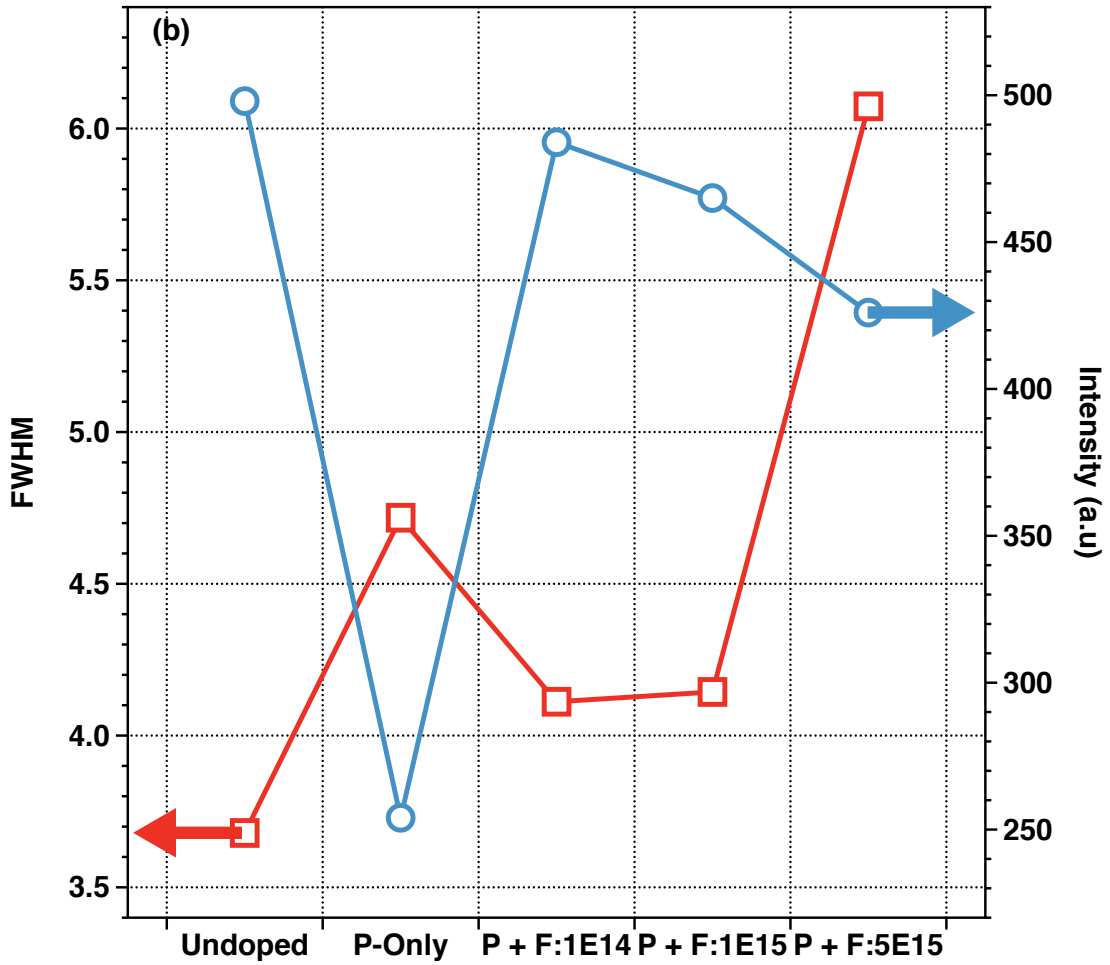

Figure 4.8 (b) Extracted value of intensity and FWHM from Figure 4.8 (a). Here, fluorine treated sample can restore the FWHM value close the control sample (undoped Ge) compared to P-only doped sample.

4.5 Conclusion

In this chapter, we have investigated the effect of F on P-doped Ge in terms of P dopant enhancement and diffusion retardation. Judging by the SRP measurements,

there is an indication that F passivates the V_{Ge} in Ge and enhances the overall activated fraction of the dopant. It is found that F is more effective in vacancy rich sample rather than Ge sample with less vacancy defects. However, even for low damaged samples, F is able to enhance their P activation rate. With optimized annealing schemes like two-step annealing, activation of P in Ge can be enhance to ~87%, which is a significant improvement.

In addition, SIMS analysis indicates retardation of diffusion by decreased dopant-vacancy pair. To be more conclusive, restoration of Ge-Ge bond peak in Raman spectra is also demonstrated by F. In short, F can be used to achieve low resistance junction and ultra shallow junction for future Ge based CMOS fabrication.

Chapter 5

Fluorine Passivation of Germanium Based Devices

5.1 Introduction

In the previous chapters, we have verified the role of vacancy defects in Ge and its passivation by F. In addition, it was confirmed that this passivation scheme could be used to enhance the P activation in Ge, while suppressing the dopant's diffusion. In this chapter, F passivation is applied to various Ge based devices for enhanced performance.

First, F passivation is applied to a Ge n+/p junction. If F is successful in passivating the defects in the n+ layer (thereby enhancing the overall activation), it will result in an increased on-current due to lowered series resistance. In addition, by reducing the vacancy and end of range (EOR) defects near the n+/p junction interface, reduction of off-current by carrier generation is expected. Based on this result, the exact same method will be applied to a S/D of a Ge n-MOSFET, in order to lower the total resistance path (R_{SD}) between the source and drain. In addition, F passivated n+/p junction is revisited in terms of carrier lifetime performance. By using temperature dependent current-voltage measurement, recombination lifetime and generation lifetime of the n+/p junction is analyzed for samples with and without F passivation. Due to lowered defect levels within the junction, both recombination and generation lifetime is expected to increase.

Next, F passivation will be applied to the interface between Ge and Al_2O_3 gate oxide in a Ge p- and n-MOSFET to reduce the interface defects density. If F passivation is effective, it will result in increased carrier mobility in the channel region. The F passivation is done by CF_4 plasma exposure, where F atom will diffuse through the gate oxide to the interface [17]. Id-Vg and split CV measurement is done to characterize the effective mobility.

For the third part, F passivation is applied to Ge/metal contacts in an attempt to reduce the contact resistance. Fermi level pinning phenomenon in Ge surface forces work function of the metal to be ‘pinned’ near the Ge valence band, regardless of its kind [1]. This allows nearly all metals to form an ohmic contact with p-doped Ge,

which is favorable when making a Ge p-MOSFET. However, this forces metals to form a Schottky barrier with n-doped Ge, which increases the contact resistance. This is considered a major obstacle in scaling Ge n-MOSFET, if it should be adapted by the industry. Fortunately, the thickness of the depletion region in a Schottky barrier decreases with n-Ge doping [48], allowing more tunneling currents to pass through. Enhanced P activation due to F passivation could result in lower contact resistance in an n-Ge/metal contact.

5.2 Fluorine Passivation of Ge n+/p Junction

A p/n junction is one of the simplest devices where F passivation can improve its performance. In general, it is known that the total current (I_{total}) in a p/n diode is the sum of diffusion and drift current. However, if we were to express this in terms of recombination and generation, the total diode current is the sum of space-charge region (scr) recombination/generation and quasi-neutral region (qnr) recombination/generation current [49], leading to the following equation

$$I_{total} = I_{o,scr}(e^{q(V-Ir_s)/nkT} - 1) + I_{o,qnr}(e^{q(V-Ir_s)/nkT} - 1) \quad (1)$$

Where r_s is the series resistance, V is the voltage, n is is the deality factor, k is Boltzmann's constant, q is the charge, T is the temperature, and $I_{o,scr}$ and $I_{o,qnr}$ are the saturation current for scr and qnr, respectively. As with most p/n diodes, doping for

each junction is usually achieved by ion implantation. During this process, defects such as vacancies are created at the junction interface, which could lead to higher generation current (off-current) at scr and qnr, for these vacancies act as carrier generation sites. Especially for n+/p diode, active dopant level is lowered by the dopant deactivation effect, as discussed in the previous chapter. By incorporating F into the n+ layer and at the n+/p junction interface, series resistance of the n+ region is expected to decrease from enhanced dopant activation. This would show up as increase in on-current in a J-V measurement. Second, when F is placed within the n-doped Ge crystal by ion implantation, portion of the F dose will be positioned at the n+/p junction interface. Because F atom will bond with the end-of-range (EOR) defects [50], it will decrease the absolute number of carrier recombination/generation sites at scr, thereby reducing the off-current in the reverse bias regime.

5.2.1 Fabrication of F Passivated Ge n+/p Diode

The final cross section of the n+/p diode and a simple process flow diagram is illustrated in Figure 5.1 (a). For its fabrication, a ~2.0μm undoped Ge was heteroepitaxially grown [25] on p-type Si. To reduce the surface damage by ion implantation, ~20nm thick low temperature silicon oxide (LTO) was deposited on epi-Ge. Then, samples were implanted with high P concentration with $5x10^{15}/cm^2$ dose at 35keV energy. This implant condition is expected to create an, n+/p junction interface at 70nm depth from the surface. The high implant dose was to account for heavy out-diffusion near the surface. The p doping in Ge comes from vacancy defects during

heteroepitaxial growth. After the n+ dopant implant, the samples were split into two groups: i) sample with F ion implant right after the P ion-implant and ii) sample with no F ion-implant. The F implant was done with $1x10^{14}$ /cm^2 dose at 15keV energy. Then, all samples went through a 500 °C anneal in N_2 ambient for 10 seconds in a rapid thermal anneal (RTA) system. Then a circular mesa structure was defined for both groups by lithography and the surrounding surfaces are etched about 500nm in depths by CF_4 plasma dry etch. For sidewall and surface passivation, 20nm of Al_2O_3 was deposited at 250 °C by atomic layer deposition (ALD). Finally, metal contacts for both n+ and p layer were defined by lithography and the exposed Al_2O_3 layer was etched away by 2% HF. After opening, 100nm of Al was deposited immediately by an e-beam metal evaporation system and the samples go through a lift-off process. By creating such mesa structure where metal contact are at top and bottom of the mesa, surface leakage current components around the diode is expected to be eliminated, allowing only the vertical current component to flow through the n+/p junction. For electrical measurement, a parameter analyzer was utilized to measure the current density–voltage (J-V) characteristics. In addition, sheet resistance of the n+ layer was measured by 4 point probing method [51]. Presence of F and P was confirmed through SIMS analysis with a separate Ge sample that was dosed with similar condition (from chapter 4), but at deeper depth (F: $1x10^{14}$ /cm^2 dose at 55keV and P: 1.8x1015 /cm^2 at 90keV). This was to see the presence of F more clearly at the junction formed by P.

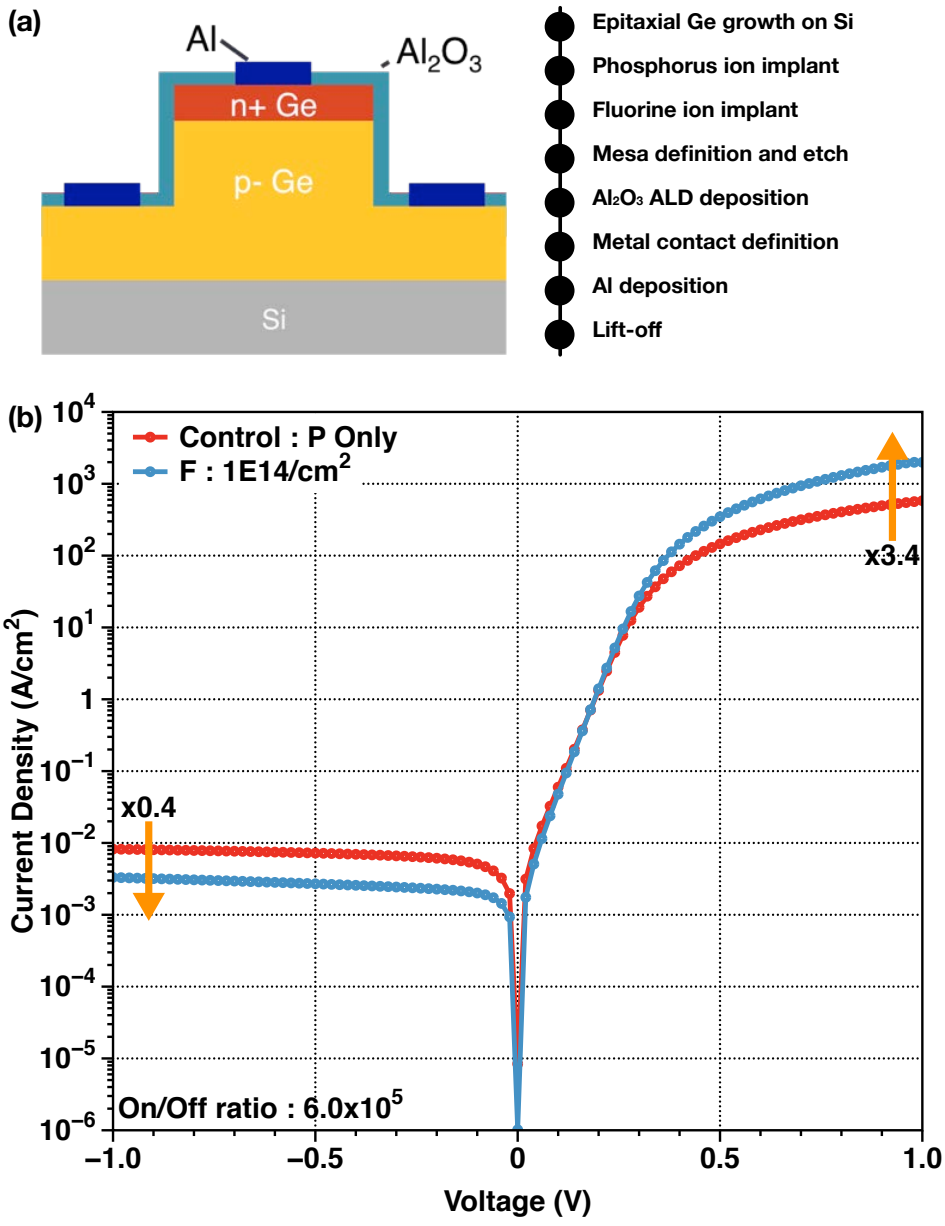

Figure 5.1 (a) Schematic of fabrication n+/p diode and its fabrication process. Here, a mesa structure is adopted to minimize the lateral leakage current. (b) Current density – Voltage (J-V) characteristics of F passivation n+/p diode. By enhanced dopant

activation on the n+ side, overall on-current has increased, while off current decreased due to lower generation current by vacancy defect sites.

5.2.2 Electrical Characterization of Ge n+/p Diode

After Ge n+/p diode fabrication, J-V characteristic was measured and the data is shown in Figure 5.1 (b). Here, it can be clearly observed that for series resistance dominant regime of the forward current, F passivated diode has 3.4 times higher on-current with respect to the control sample without F. Sheet resistance measurement for the fluorinated n+ layer was 380 ohm/sq compared to 820 ohm/sq in the control (non fluorinated) sample, confirming series resistance reduction. In addition, series resistance could have been reduced to further extent, because the implanted F could have lowered the contact resistance between the n+ Ge and metal contact. Lowering of the contact resistance by F passivation will be discussed in further detail in the later section of this chapter. Besides the on-current increase, F passivated diode showed lower off current than the control sample by a factor of 0.4, while maintaining a similar off-current slope to the control sample. SIMS analysis shown in Figure 5.2, confirms F concentration peak near the n+/p junction region, which is known to have EOR defects after ion implant and anneal [52]. It is believed that F has bonded with the EOR defects and vacancy defects in the region, thereby reducing the defect concentration within the n+/p junction interface (which includes scr and qnr). This would result in lower carrier generation/recombination center, thereby causing lower off-current when the diode is reverse biased. Overall, F passivated n+/p diode showed better performance in term of on- and off- current level, having an excellent on/off

ratio of about $6x10^5$. Such result is encouraging for reduction of source to drain resistance (R_{SD}) in a Ge nMOSFET, which will be discussed in a later section.

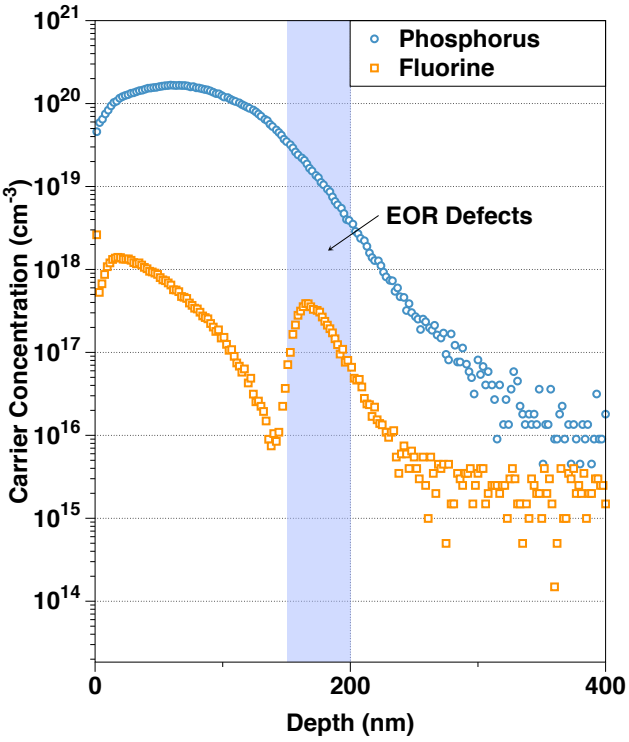

Figure 5.2 SIMS profile of F and P in after diode fabrication. F peak is observed near 180~200nm deep from the surface. This region is abundant with end of range (EOR) defects, which is usually present after heavy ion implantation of P. F atom clears interacts with these defects, thereby creating an electrically inert compound.

5.2.3 Carrier Lifetime Characterization

As described earlier, the forward diode current is the sum of carrier recombination in the space charge region and quasi-neutral region. With bias increase,

recombination current from increase scr tend to be slower than qnr recombination current increase, although the initial qnr current value is lower than scr current at low bias values (for the case of Si). This means that depending on the bias condition, one component might be more dominant than the other. As illustrated in Figure 5.3, the degree of particular current dominance can be inferred by looking into the ideality factor of the current slope. For scr recombination, the ideality factor converges to 2, while qnr recombination takes on the value of 1. Ideally, the slope of the forward current in a diode assumes the scr recombination is negligible, taking on the value of 1. Close look at the J-V curve in Figure 5.1 (b), we find that there are slight difference in the current slope in the 0V ~ 0.2V regime between the control (non fluorinated) and the fluorinated sample. This suggests that there is less of scr recombination for fluorinated samples. To investigate further, the temperature was lowered to -30°C and J-V plot is measured again, as shown in Figure 5.4. As the temperature is lowered, current contribution from qnr recombination decreases faster than scr recombination does, making the current difference between scr and qnr current to be more apparent in the low forward-bias region. Clearly in region II, it is shown that diode treated with F shows lower current level and steeper slope than the control sample. For clarification, ideality factor is extracted and plotted as a function of temperature, which is shown in Figure 5.5 (a). Compared to the control with no F implant, fluorinated samples show ideality factor close to that of ideal Ge diode. This indicates that sample treated with F has fewer recombination centers within scr than the control sample. This also means that overall defect density within the scr region has decreased. Based on ideality factor

values at various temperatures, it is possible to extract the carrier recombination lifetime within the junction as a function of temperature [53], and the result is shown in Figure 5.5 (b). At room temperature, the carrier recombination lifetime has increased from ~500ns to ~900ns. From temperature dependent J-V measurements, it is also possible to extract the activation energy of the traps within the junction. Figure 5.6 (a), shows the resulting Arrhenius plot for fluorinated sample and the control. Although the activation energy seems to be similar for both curves (0.44eV for F treated sample and 0.42eV for the control sample), suggesting that the dominant trap levels for both samples are almost the same, F treated sample seems to have lower absolute density of traps, leading to lower scr current. With previously obtained carrier recombination lifetime and the activation energy, the generation lifetimes can be calculated [54], and is shown in Figure 5.6 (b) as a function of temperature. With F treatment, it is observed the generation lifetime greatly increases from 20μs to 60μs at room temperature. For optoelectronic applications such as Ge based detectors and light emitting diode (LED), lowering of scr recombination by defect density reduction would prove beneficial, for it increases both recombination and generation lifetime in the junction.

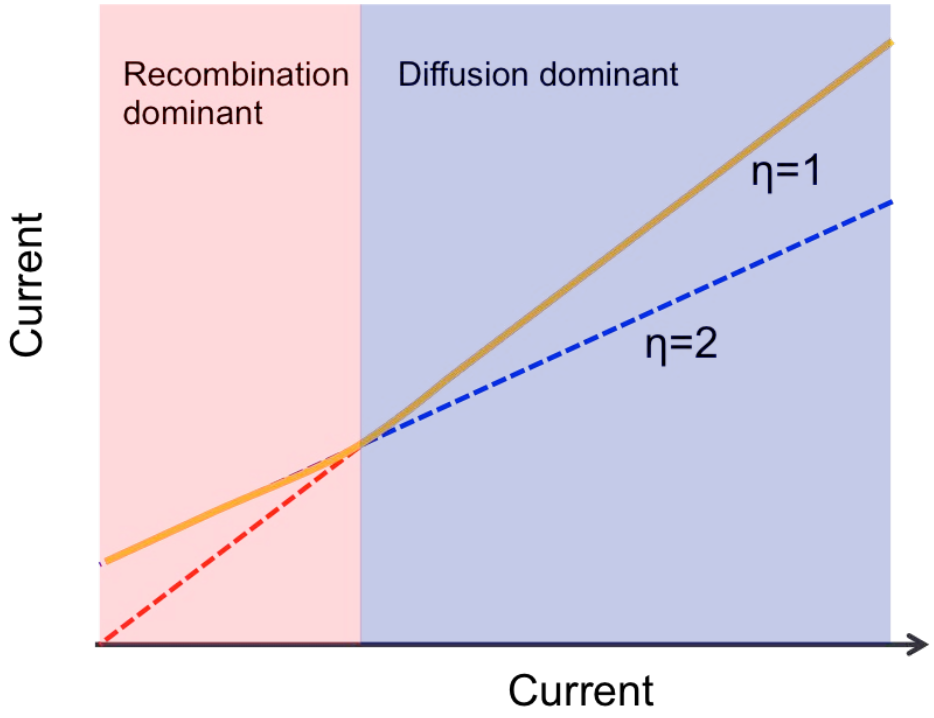

Figure 5.3 Theoretic domains in forward biased p/n diode. At low bias, recombination current dominates the forward current, which is dependent on the junction carrier lifetime.

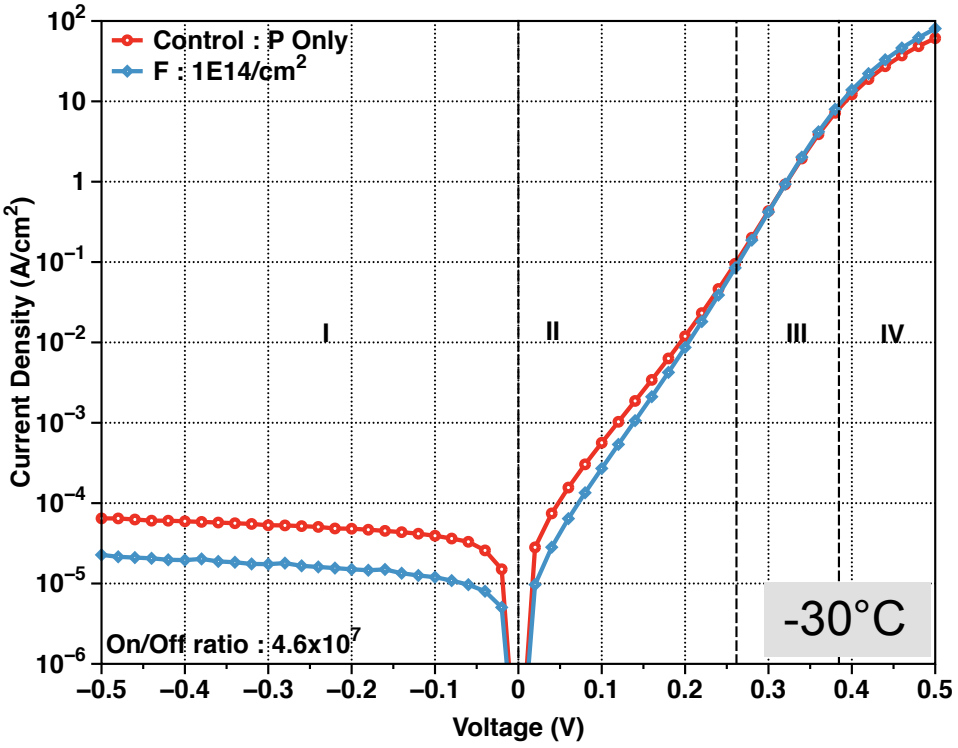

Figure 5.4 J-V plot of Ge n+/p diode at -30°C. At this temperature, the diffusion dominant region (III) and the recombination dominant region (II) becomes more distinct.

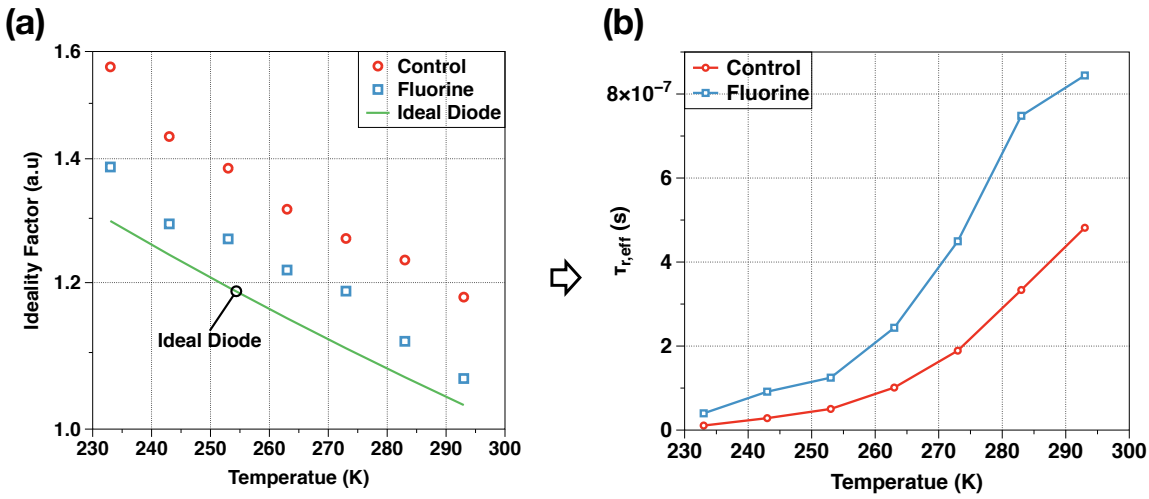

Figure 5.5 (a) Ideality factor comparison of n+/p diode treated with and without F. Based on the ideality factor at the recombination current dominant regime, (b) carrier lifetime is extracted and is plotted.

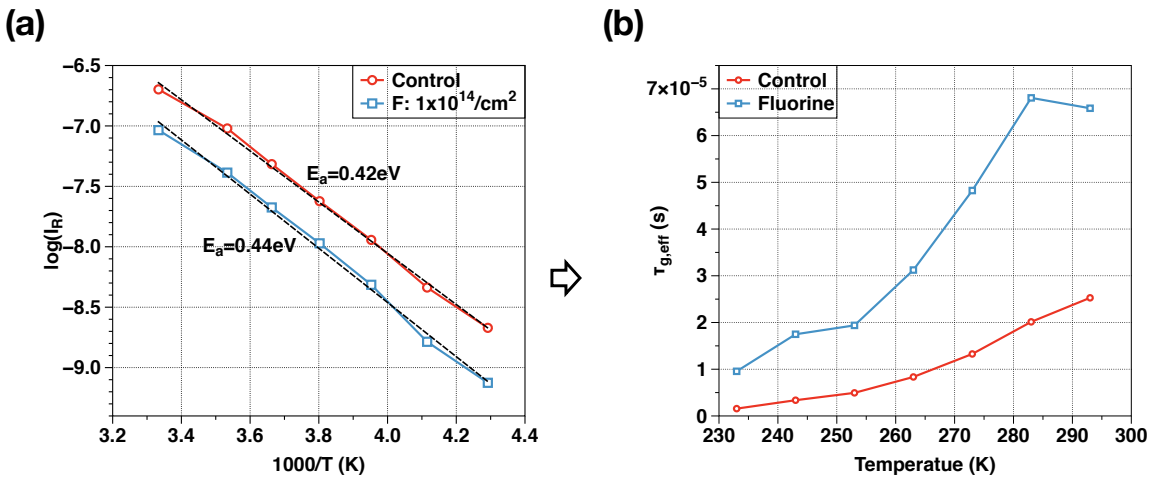

Figure 5.6 (a) Activation energies of control and fluorinated samples by temperature dependent J-V measurement. (b) Extracted generation lifetimes as a function of temperature.

5.3 Fluorine Passivation of Ge MOSFETs

5.3.1 Fabrication of Ge nMOSFET with F Passivation S/D

Figure 5.7 shows the final cross section and the process flow for Ge nMOSFET with F passivated S/D. Similar to n+/p diode fabrication in section 5.2.1, ~2.0μm undoped Ge was grown on p-type Si by heteroepitaxy [25]. For gate oxide deposition, HF-HCl cyclic clean [55] is performed on the substrate to make the surface sub-oxide free. Then, about 1nm of Al_2O_3 oxide was deposited in an ALD chamber at 250 °C, followed by O_3 annealing at 400 °C [56]. This is to create a thin GeO_2 layer that gives very good passivation for the channel-gate oxide interface. Afterwards, about 9nm of additional Al_2O_3 oxide was deposited without breaking the vacuum. Gate metal consisting of 20nm thick titanium nitride (TiN) and 50nm thick tungsten (W) was deposited by a sputtering system. Gate region is then defined by lithography the surrounding area is etched away by SF_6 plasma. Fortunately, this SF_6 plasma etch gives excellent selectivity between the TiN layer and the Al_2O_3 gate oxide, leaving Al_2O_3 virtually unharmed during the etch process. Before removing the photo-resist (PR) after the gate etch, the S/D area was implanted with P with $1.0x10^{15}/cm^2$ dose at 90keV. The remaining PR on the gate should protect the gate metal from ion implant damage. Then the sample was implanted again with $1x10^{13}/cm^2$ of F at 55keV. In conjunction, sample without F implant is also made as a control sample. After PR removal by O_2 ashing, the samples were annealed at 500 °C for 10 seconds in a N_2 ambient for n-dopant activation. Contact areas were then defined by lithography and the exposed Al_2O_3 layer was opened by 2% HF solution. Finally, 100nm thick Al was

deposited by e-beam evaporation and the outside metal area is removed by lift-off process. Id-Vg characteristics of the MOSFETs were measured by parameter analyzer.

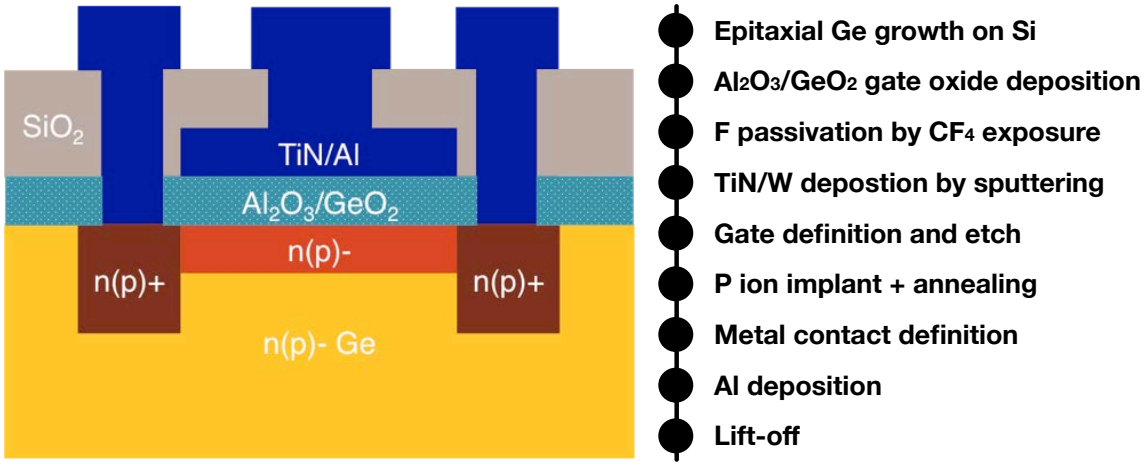

Figure 5.7 (a) Schematic diagram and the process flow of fabricated Ge n-MOSFET with F passivation in S/D.

5.3.2 Electrical Characterization of Ge nMOSFET with F Passivated S/D

In a MOSFET, the total resistance path between source and drain is comprised of channel and series resistance (sum of source, drain, and contact resistance). When the gate length for Si MOSFETs were still scaling down in the ~μm regime, channel resistance was the dominant component. Therefore, the series resistance didn't pose much of a problem and the Si MOSFET community faced relatively a small challenge in continuing the scaling paradigm. However, as the gate length was scaled down to

sub μm regime, the situation was reversed. As seen in Figure 1.4 from chapter 1, contribution from series resistance increased after the 100nm barrier, eventually becoming an equally contributing component as the channel resistance at 20nm node. Therefore, the Si MOSFET community began implementing methods to lower the series resistance. This included increasing the doping level in the source and drain while making the S/D-metal interface as ohmic as possible. The same situation will apply to Ge based MOSFET if it should be adapted by the industry. As we have already discussed in chapter 2, achieving high doping density over $1x10^{20}/cm^3$ for n-type doping seems to be a challenging task because of dopant deactivation phenomena. This is where passivation of S/D by F is effective. Figure 5.8 (a) shows the Id-Vg characteristics of Ge nMOSFET fabricated with F passivation adapted to S/D. The measured device had a gate length of 5μm, and the measurement parameter was Vg sweep from 0V to 1V at Vds = 0.1V. Here, it was found that there was approximately 15% increase in on-current on the fluorinated sample compared to the control sample. However, because we have fabricated a long channel MOSFET device with gate length of ~5um, the channel resistance still dominates and makes up most of the total resistance. Thus, it is expected that the ratio of on-current enhancement will increase as the gate length decreases. In Figure 5.8 (b), total resistance across the source and drain is measured for Ge n-MOSFET with gate length from 30μm to 3 μm and is plotted as a function of gate-length and resistance. It is observed that the degree of resistance reduction in the fluorinated sample compared to the control sample increases as the gate length decreases to 3μm. If we were to extrapolate this trend to

zero gate length, which is the total resistance in just the source and drain region, we can see that there is about 50% reduction in resistance in the fluorinated sample. This is the same trend that we got from the sheet resistance measurement in the n+ layer that is mentioned in section 5.2.2. So far, we have dealt in passivation only the bulk vacancy defects in Ge for device performance enhancement. In the next section, F passivation of channel region of the Ge p- and n-MOSFET will be investigated.

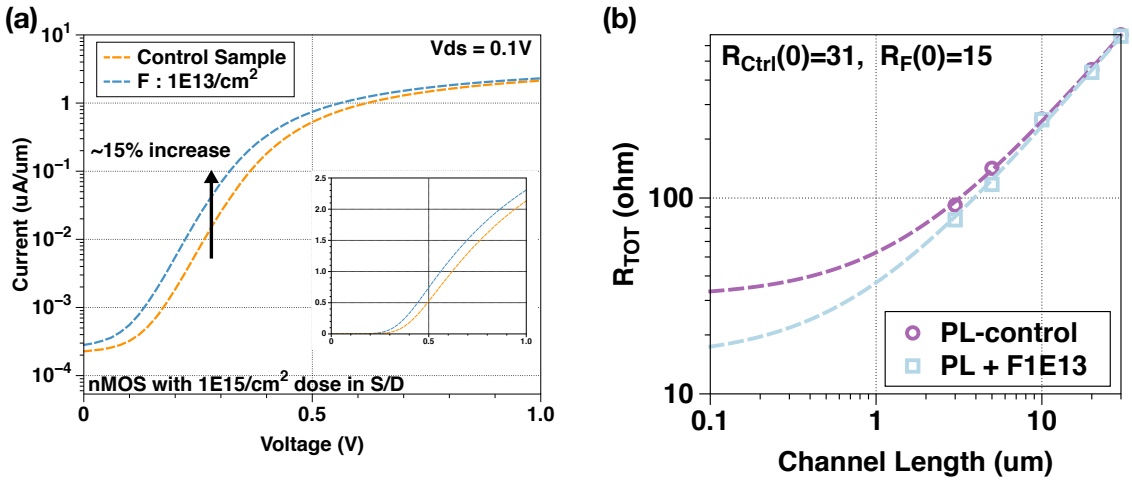

Figure 5.8 (a) Id-Vg characteristics of Gen MOSFET with fluorinated S/D. Here we obtain about 15% increase in on-current due to lowered S/D resistance. (b) Total resistance along the channel and S/D as function of gate length. As S/D resistance becomes more dominant with gate scaling, benefit of F passivation at S/D becomes more apparent.

5.3.3 Fabrication of F Passivated Ge p- n- MOSCAP

Figure 5.9 shows the fabrication process flow for F passivation of Ge p- and n-MOSCAPs. Fabrication begins with the same epitaxially grown 2.0 μm thick Ge on Si substrate mentioned in section 5.2.1. First, the wafers went through cyclic HF-HCl cyclic clean for surface clean up [55]. Next, 12nm thick layer of Al_2O_3 is deposited on top of Ge surface in an ALD system at 250 °C. For F passivation of Ge/Al_2O_3 interface, the sample is exposed to CF_4 plasma with a flow of 500sccm at 40W in a PECVD system. During this process, F atom will diffuse through the Al_2O_3 layer passivating the defect at the Ge/Al_2O_3 interface. Adjusting the sample's exposure time to the CF_4 plasma from no exposure to 40 minute exposure controls the degree of F passivation. Then the samples are deposited with 20nm thick TiN and 50nm thick W as a gate metal. MOSCAP pattern was then defined by lithography and the metal layers were etched by SF_6 based plasma. In addition, the backside of substrate was deposited with platinum (Pt) to provide good contact. Capacitance – Voltage (CV) measurement was then done for the samples using a LCR meter along with a parameter analyzer.

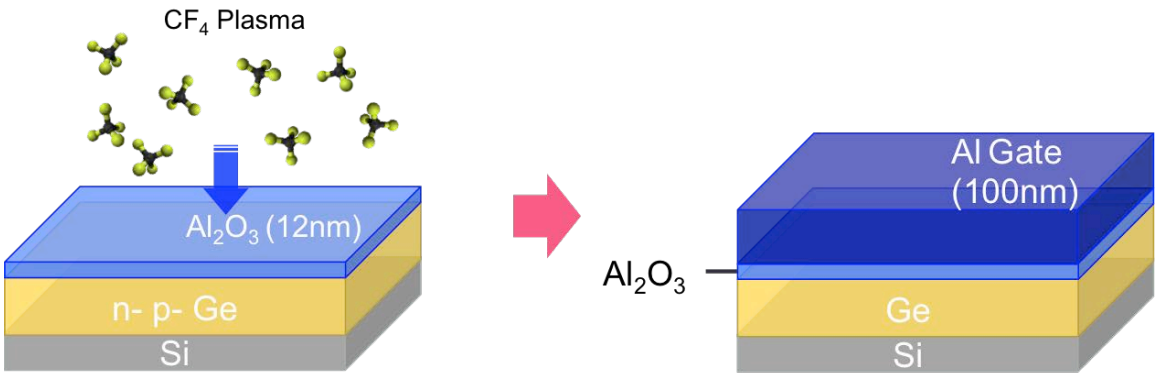

Figure 5.9 Process diagram for Ge p- and n- MOSCAPs.

5.3.4 Electrical Characterization of F Passivated Ge p- n- MOSCAP

The measured CV characteristics for Ge p- and n-MOSCAPs according to different CF_4 plasma exposure are shown Figure 5.10 (a) and (b), respectively. Here, main indication that it is the defects that are being passivated is the fact that CV bumps that are associated with the defects are decreasing as the fluorination time is increased. This effect can be clearly seen for p-MOSCAPs in Figure 5.10 (b), where the CV bump near 0.8V is a representative feature caused by interface defects in Ge p-MOSCAP. Although not completely eliminated, it can be observed that with increased fluorination time, these bumps begin to shrink. Similar effect is also observed for Ge n-MOSCAPs shown in Figure 5.10 (a), where the CV kink near 1.2V is eliminated with F passivation. In addition, for both MOSCAPs the slope between the accumulation and inversion seems to increase with F incorporation, also suggesting defect reduction. Interface defect density extracted by conductance method shows that for Ge p-MOSCAPs, the value improved from $5x10^{12}$ /cm^2-eV (0min exposure) to

$7x10^{11}$ /cm^2-eV (40min exposure). For Ge n-MOSCAPs, the interface defect density decreased from $9x10^{12}$ /cm^2-eV (0min exposure) to $3x10^{12}$ /cm^2-eV (40min exposure). It can be expected that with better Ge gate stack such as Ge/GeO_2/Al_2O_3 with O_3 annealing, F passivation will give additional boost in giving more ideal CV profile. However, this reduction of interface defects comes at the expense of increased negative fixed charge in the oxide, indicated by positive flat band voltage (V_{fb}) for Ge p- and n- MOSCAPs. It is thought that these fixed oxide charges are created during the CF_4 plasma treatment. Such results are expected to increase the effective mobility in a Ge p- and n-MOSFETs, which is investigated in the next section.

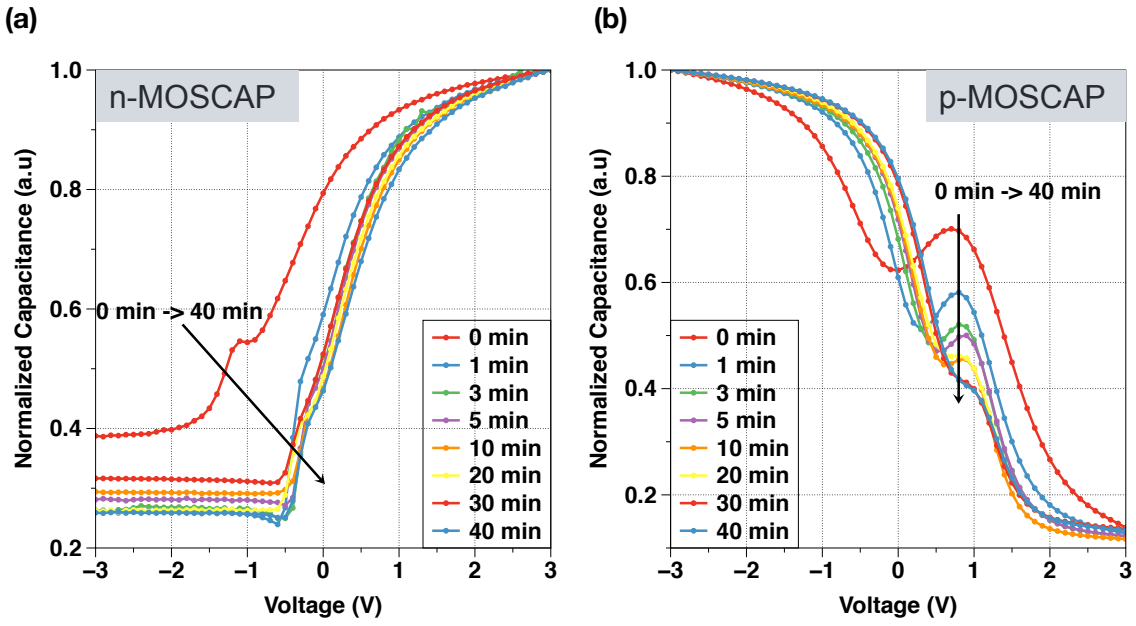

Figure 5.10 Current-Voltage response of fluorinated Ge (a) n- and (b) p- MOSCAPs.

5.3.5 Fabrication of Ge p- n- MOSFETs with F Passivated Channel Region

Based upon the MOSCAP results in section 5.3.4, Ge p- and n- MOSFETs were fabricated with F passivated channels. Figure 5.11 shows fabrication process flow the Ge p- and n- MOSFETs and its cross section diagram. Again, we start off with ~2.0μm thick undoped Ge, grown on p-type Si by heteroepitaxy [25]. Then 10nm Al_2O_3 oxide was deposited by using O_3 annealing method mentioned in section 5.2.3. Then the samples were exposed with CF_4 plasma for 0 minutes (control sample) to 20minutes to differ the degree of fluorination. Then 20nm thick TiN and 50nm thick W was deposited as gate metal by a sputtering system. This region is etched by SF_6 plasma after defining the gate region by lithography. Then, with the PR still intact after gate-etch, the S/D area was implanted with P dose of $1.8x10^{15}/cm^2$ at 90keV for Ge nMOSFET and with B dose of $5x10^{14}/cm^2$ at 35keV for Ge pMOSFET. PR was then removed by O_2 ashing, and samples were annealed at 500 °C for 10 seconds in a N_2 ambient for dopant activation. 100nm thick Al was deposited by e-beam evaporation after contact area definition by lithography and Al_2O_3 barrier removal by 2% HF. Id-Vg characteristics for these Ge p- and n- MOSFETs were measured by a parameter analyzer, and the their mobility was measured by split CV measurement.

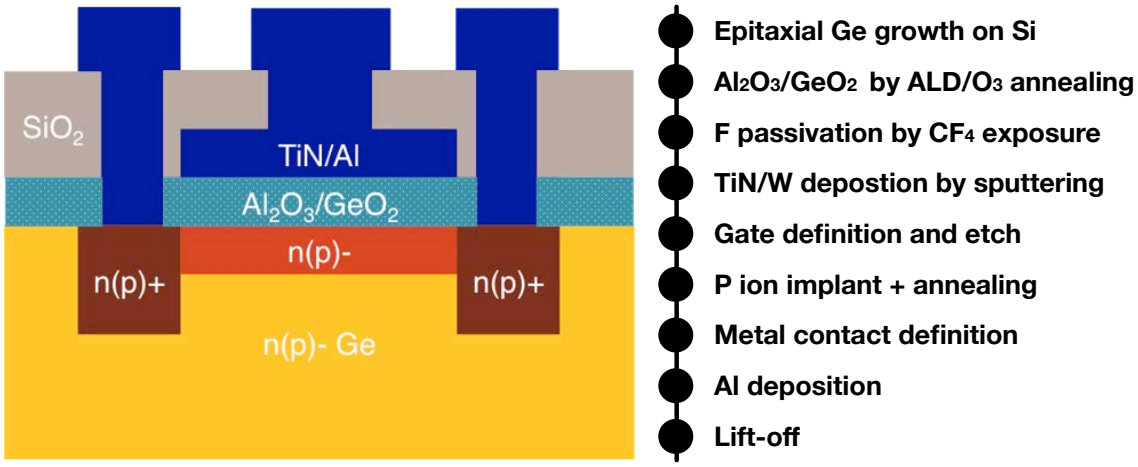

Figure 5.11 Schematic of fabricated Ge n-MOSFET with F passivation in the channel region.

5.3.6 Electrical Characterization of Ge p- n- MOSFETs with F Passivated Channel Region

By improving the gate oxide interface with Ge substrate in Ge MOSFET, one can obtain better performance in terms of carrier mobility, which gives better on-current in I_d-V_g measurement. Figure 5.12 respectively shows the I_d-V_g curves for Ge p- and n-MOSFETs. As previously discussed in section 5.3.4, the threshold voltage (V_t) shifts positively for F treated samples, due to increased bulk oxide charge during the CF_4 plasma treatment. But, both samples show an increase in on-current with improvement in sub-threshold (SS) voltage. This suggests that the interface scattering is less for F treated samples. For quantification, carrier mobility for both samples was extracted by split-CV method and is shown in Figure 5.13. Here, there was ~40% improvement in terms of peak hole mobility for Ge p-MOSFET and ~20% improvement in peak

electron mobility for Ge n-MOSFET. Although the mobility enhancement diminishes at higher charge density of N_{inv} = ~2x10^{12} /cm^2, there are still mobility improvemets where Ge MOSFETs can benefit from fluorine.

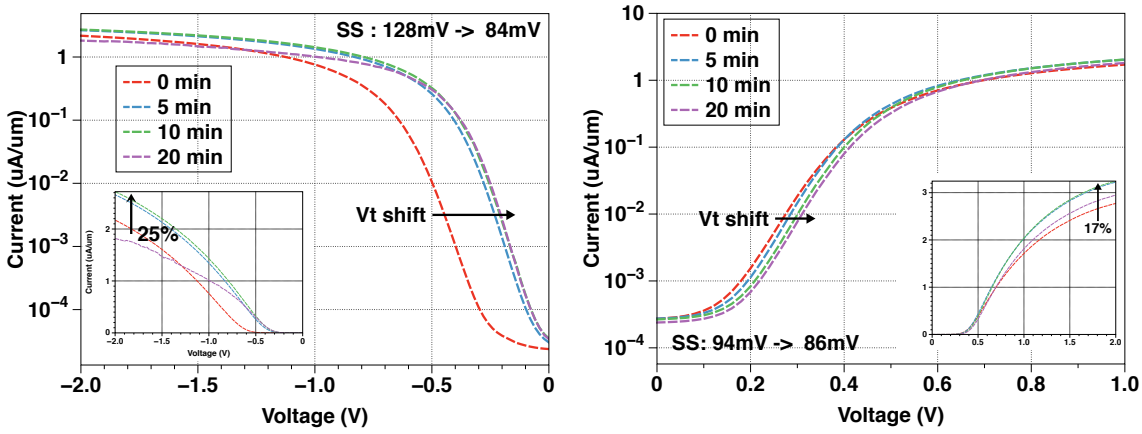

Figure 5.12 I_d-V_g measurement of Ge p- and n- MOSFET with F passivation in the channel interface. For both cases, increase of on current with shift threshold voltage (V_t) is observed.

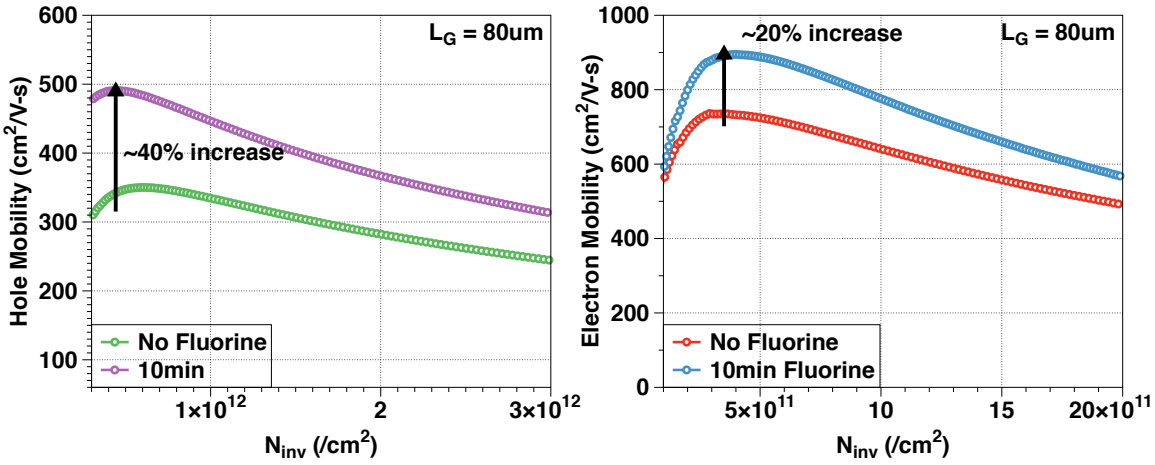

Figure 5.13 Hole and Electron mobility measurement from Ge p- and n- MOSFET. Mobility improvement is present for both Ge p- and n- MOSFETs.

5.4 Fluorine Passivation of Ge/Metal contacts

5.4.1 Fabrication of Fluorine Passivated Circular Transfer Length Method (cTLM) Structure

Figure 5.14 (a) and (b) illustrates the top view and cross section diagram for cTLM respectively. First, cTLM structures were defined on ~20nm of Al_2O_3 capping layer on 2.0 μm thick Ge that was heteroepitaxially grown on Si. Then P concentration with $1.8x10^{15}/cm^2$ dose at 90keV energy was implanted followed by F implant from $1x10^{14}$ $/cm^2$ to $5x10^{15}$ $/cm^2$ dose at 55keV. Control sample with no F implant was fabricated along with this sample. After PR removal by O_2 ashing, the samples underwent 500 °C thermal anneal in N_2 ambient for 10 seconds using a RTA system. Then metal contact areas was defined for the cTLM structure by lithography and the

exposed oxide area was etched away by 2% HF. Then 100nm Al was deposited by e-beam evaporation and lift-off process was carried out. Al was selected for the n-Ge contact, because of it's work function of 4.06 eV would ideally form an ohmic contact with n-Ge, if it not for Fermi level pinning. The resulting set of structures along with different dimensions is illustrated in Figure 5.14 (c). In addition to these samples, the exact same cTLM structures with surfaces that was etched about ~80nm in depth after P and F ion implant by Ge etchant (mixture of nitric and citric acid) was fabricated. Electrical characterization for the samples was done using a parameter analyzer.

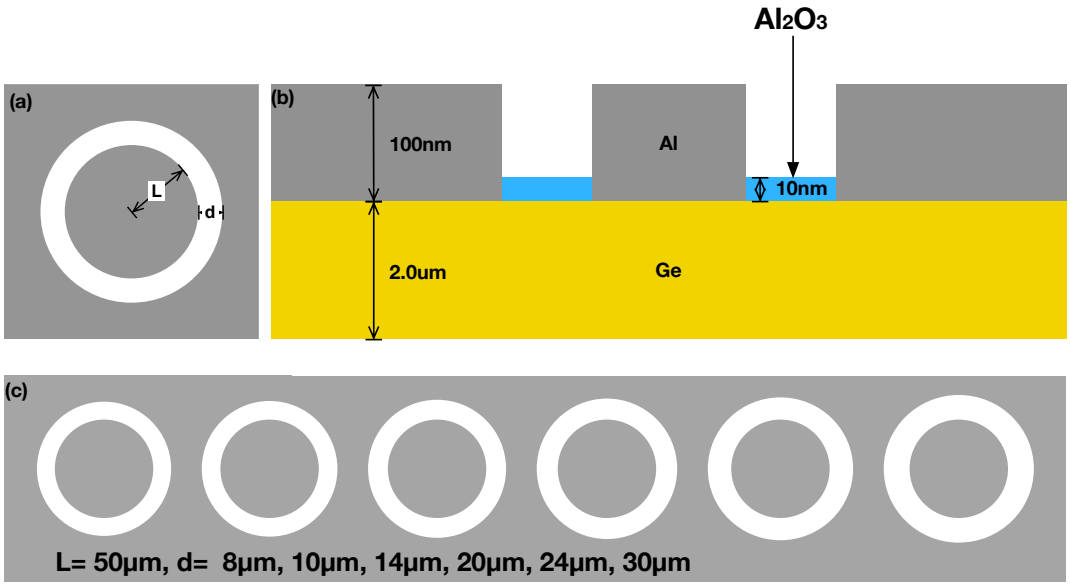

Figure 5.14 (a) Single cTLM structure with radius 'L' and ring thickness 'd'. (b) Cross section view of cTLM structures. (c) cTLM structures with different 'd' values. By mapping out the resistance values for ring, contact resistance can be extracted.

5.4.2 Electrical Characterization of Ge/Metal Contacts with F Passivation

Previous results in chapter 4 suggest that F is effective in enhancing the n-type dopant activation in Ge. Because higher doping would thin down the Schottky barrier region [48] between n-Ge/metal interface, it would in turn reduce the contact resistance by allowing more tunneling current to pass. Therefore, higher n-type dopant activation in a P-doped Ge by F passivation would naturally decrease the contact resistance. Electrical contact resistance was extracted by cTLM structure, which is basically a series of circular contact pads isolated by a circular ring differing in diameter. By extrapolating the resistance extracted by each ring diameter to the point where total resistance is zero (the x-intercept), one could calculate the contact resistance between the semiconductor and metal interface [49]. By this method, the contact resistance values were extracted for the samples with F passivation and sample with no F (control sample) and are plotted in Figure 5.15. Here we can observe for F doping with $1x10^{15}$ /cm^2, the contact resistance is about $9.0x10^{-5}$ ohm-cm^2, compared to that of control sample, which is $1.4x10^{-4}$ ohm-cm^2. This is not so much of an improvement and is well within each other's error bar range. In addition, with too much F doping of $5x10^{15}$ /cm^2, the contact resistance increases. This is because P dopant activation in Ge decreases significantly due to heavy F ion implant damage, lowering the active doping. However, there is another possible explanation why F passivation is not effective for contacts. Previously in chapter 4, we briefly mentioned that during a thermal anneal, vacancy defects tend to move towards the surface. These

vacancies could cluster by themselves, thereby forming a very stable state with low binding energy than F_nV_m complexes. Then these complexes would not be affected by F passivation and would not disassociate during a 500 °C anneal. SRP results in chapter 4 always have a dip in the surface, which may be from the vacancy clusters interacting with n-type dopants, making them electrically inert. This 'dip' was observed in other works showing SRP of n-type dopant in Ge[40], [57], but was not mentioned properly because it was viewed as a measurement artifact. If this was the case, the contact resistance should be improved if this defective surface layer was removed. For verification, contact resistance was again extracted by cTLM method on the samples where the surface was etched about 80nm in depth. A simple schematic of the process and the result of contact resistance extraction are shown in Figure 5.16 (a) and (b), respectively. Contact resistance reduction of about an order of magnitude is observed in all cases including the control sample without F implant. In addition, F implanted sample with dose of $1x10^{14}$ /cm^2 showed 50% lower contact resistance than the control sample. This trend is consistent with the dopant activation results in chapter 4, where the F implanted sample with dose of $1x10^{14}$ /cm^2 showed the highest activation. Because the tunneling current through the Schottky barrier in between the Ge-metal interface would increase with higher surface doping [48], this contact resistance reduction trend follows the active P doping enhanced by F with $1x10^{15}$ /cm^2 to $5x10^{15}$ /cm^2 dose. In such aspect, alternative process such as CMP can be utilized to remove the surface defective layers after all ion implantation in addition to smoothing

the surface for further device fabrication, but this is beyond the scope of this work and needs further investigation.

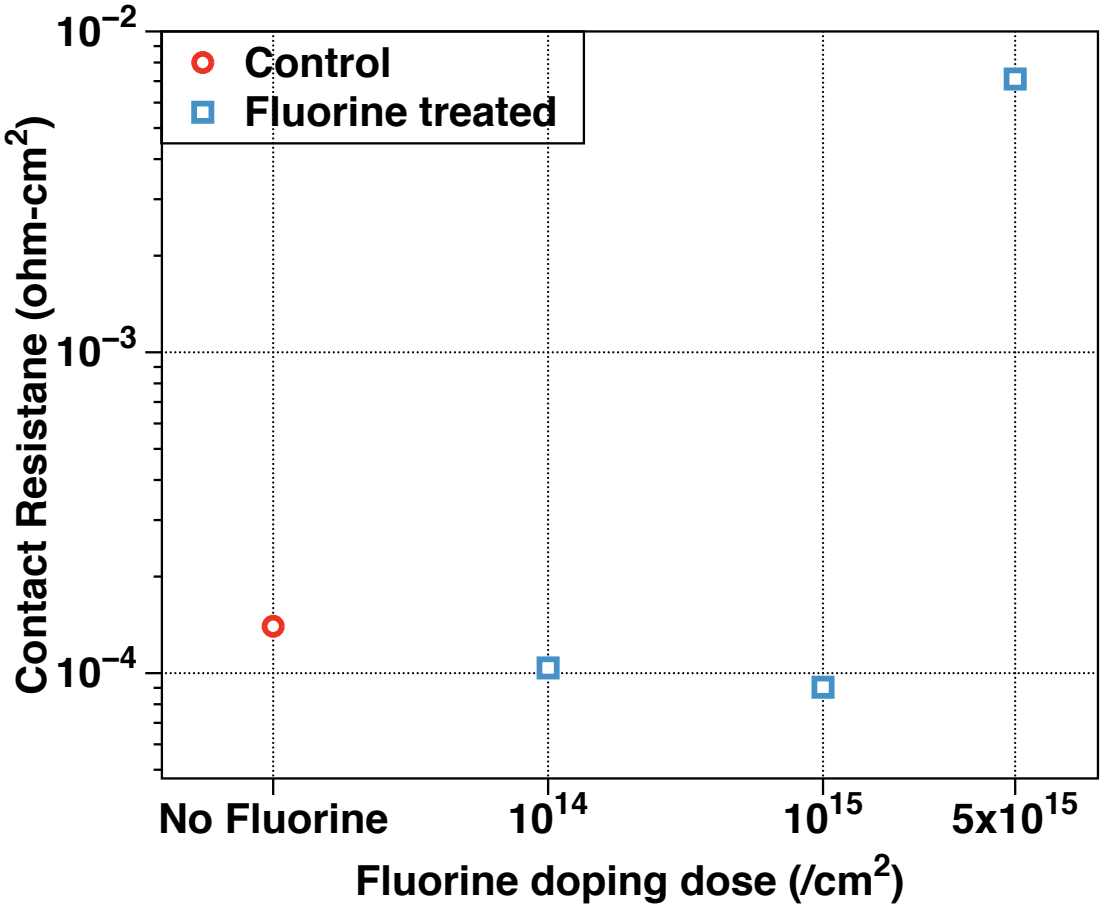

Figure 5.15 Contact resistance measurement for fluorinated samples. Despite the expectation, fluorine passivation only lowered the contact resistance by on ~20%.

(b)

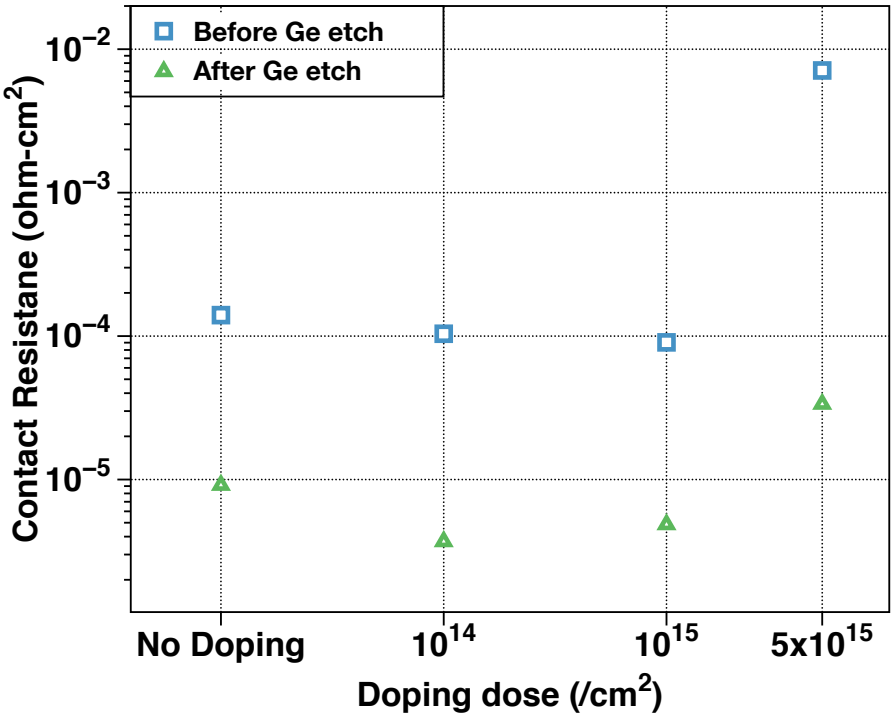

Figure 5.16 (a) Schematic diagram of removing the top damaged layer after ion implantation/annealing. Ge is etched until it reaches the depth where n-doping is at the peak. (b) Contact resistance measurement after Ge etching. For all samples, contact resistance was lowered about an order of magnitude.

5.5 Conclusion

In this chapter, applications of F passivation to various Ge devices have been investigated. The basic principle was to passivate the defects that are present below the surface and on the surface. For Ge n+/p diode, both on-current and off-current level improved, leading to high on/off ratio. This was mainly because F passivation helped to achieve higher dopant activation for the Ge n+ region and less generation current in the scr region. In the case of Ge MOSFETs where the S/D area was passivated with F, reduction of series resistance was observed that would be beneficial further scaling down of GeMOSFETs. In addition to F passivation in the Ge bulk area, it was found that F passivation of Ge/gate-oxide interface leads to improved CV response in Ge MOSCAP, resulting in increase in the effective mobility in Ge MOSFETs. For optical Ge devices, F passivation in the n+/p junction leads to carrier lifetime increase, for both recombination and generation lifetime because of defect density reduction in the junction. Finally, application of F passivation to n-Ge/metal contact resistance was attempted. It was found that with enhanced P activation in Ge by F passivation along with surface damage removal by wet etching, n-Ge/metal contact resistance was reduced.

Chapter 6

Conclusions

Point defects play a significant role in application of Ge to device fabrication. In this dissertation, electrical roles of point defects have been investigated, and efforts of passivating those defects with F have been attempted for various Ge devices.

In chapter 2, basic terminology of defects and their electrical roles were defined. In Ge, vacancy defects act as acceptor sites and also diffusion enhancing sites for n-type dopants. Especially for n-type Ge devices, vacancy defects (i) deactivate implanted n-type dopant, and (ii) make it difficult to achieve a shallow junction because of vacancy enhanced diffusion. Surface defects on Ge pose other challenges. They degrade the channel mobility of Ge MOSFETs and pin the Fermi level when contacted with metal, making it difficult to achieve an ohmic contact for n-Ge/metal interface.

In chapter 3, the role of vacancy defects in Ge was experimentally verified. When vacancy defects are intentionally created by ion implantation, they act as acceptor like sites, which was verified by SRP. Next, F was proposed as a possible passivating element for the defect sites. By incorporating F into vacancy rich Ge by ion implantation, followed by thermal annealing, it was shown that most of these defects can be eliminated.

In chapter 4, F passivation was applied to P (n-type) doped Ge to verify if it can negate the effects of vacancy defects. By using SRP and SIMS, it was experimentally proven that F passivation can help P in Ge to achieve higher electrically active dopant concentration of ~$1x10^{20}$ /cm^3 with less diffusion than estimated P diffusivity in bulk Ge.

In chapter 5, passivation effects of F in various Ge devices were investigated. For Ge n+/p diode, F passivation enhances the on-off ratio by reducing the series resistance in forward bias and leakage current in reverse bias. This method was then applied to a Ge p- and n-MOSFETs with F passivation in S/D area. As expected, overall source to drain resistance decreased due to series resistance reduction in S/D. Then F passivated n+/p diode was revisited to investigate its carrier lifetimes. Since F passivation reduces the defects in the n+/p junction, both recombination and generation lifetime are increased. Such results will be useful for Ge based optical devices. Next, F passivation by CF_4 plasma exposure to Ge/Al_2O_3 was investigated through MOSCAP measurements. For both Ge p- and n-MOSCAPs, F passivation reduced the D_{it} values closer to the ideal for Ge MOSFETs. Such method was applied

to Ge p- and n-MOSFETs and it was found that hole and electron channel mobility were improved by F passivation. In the last experiment, F passivation by ion implant for n-Ge/metal contact was investigated. F incorporation to Ge was able to lower the contact resistance further than the sample without F through higher n-dopant activation. However, better contact resistance was achieved by simply etching the first few 10nm of the surface for both F implanted and non-F implanted samples. It was speculated that the surface of Ge doesn't fully recover from the effect of implantation induced defects even after thermal anneal and F passivation.

Although not covered here, it would be worth investigating the effect of F passivation for noise reduction in Ge devices. Defects in Si can act as a noise source, and it would be a similar scenario for Ge devices. By passivating out these defect sites with F, one should be able to reduce the noise level to a certain extant.

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