GERMANIUM-TIN (GESN) TECHNOLOGY

A DISSERTATION

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING

AND THE COMMITTEE ON GRADUATE STUDIES

OF STANFORD UNIVERSITY

IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

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August 2013

This dissertation is online at: http://purl.stanford.edu/xx161jj1880

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Abstract

Semiconducting GeSn alloy is a versatile material system that is attracting significant research interest due to its several unique and beneficial properties, such as the ability to show a direct band gap and the compatibility with conventional Si technology. GeSn alloy system is also predicted to exhibit high electron and hole mobilities, making it an ideal material platform for co-integration of Si compatible photonics and high speed CMOS devices.

This thesis discusses a very broad range of topics pertinent to GeSn, beginning with a detailed theoretical study of electronic properties of GeSn using both first principles and empirical methods. Challenges in obtaining high quality epitaxial GeSn thin films are addressed. Innovations in GeSn material processing and device fabrication are presented. Applications of the GeSn technology thus developed to high performance logic devices, Si-compatible photonics and 3-dimensional integrated circuits are discussed.

Acknowledgements

I am grateful to my thesis advisor, Prof. Krishna Saraswat, for giving me the opportunity to work on this topic and his invaluable guidance over the last several years. The creative freedom given to me by Prof. Saraswat was the essential ingredient in turning this project into a successful venture. I am also thankful to my co-advisor Prof. James Harris and Prof. Yoshio Nishi for their constant support and encouragement over the years.

The work presented in this thesis was made possible because of numerous fruitful collaborations. I have enjoyed the good fortune to interact with and learn from researchers who are experts in their fields. These interactions have played a crucial role in making my doctoral research work an enriching and enjoyable experience. I would like to thank Dr. Blanka Magyari-Kope for sharing her expertise on first principles simulations; Prof. Piero Pianetta and Dr. Apurva Mehta for their help with measurements at the Stanford Linear Accelerator Center (SLAC). It has been my pleasure to work in close collaboration with Robert Chen, whose passion and energy for this project never dwindled despite several setbacks along the way. His wealth of experience in materials growth and characterization was a valuable resource.

I wish to thank colleagues at IMEC and KU Leuven: Benjamin Vincent, Dennis Lin, Andrea Firrincieli, Federica Gencarelli and Matty Caymax for hosting me as a visiting scholar at IMEC in the summer of 2011. I am grateful to Dennis Lin for

teaching me the finer details of MOS device characterization and analysis. I would also like to extend my gratitude to Benjamin for his pivotal role in establishing this collaboration and his help in GeSn material growth. I would like to thank colleagues at Applied Materials: Yi-Chiau Huang, Yihwan Kim and Errol Sanchez for sharing their expertise on GeSn material growth and providing me with very high quality material for experimental work. Towards the end of my PhD, I had the good fortune to meet and collaborate with folks at Synopsys: Victor Moroz, Lee Smith and Qiang Lu. I wish to thank them for their help in strained FinFET simulations using Synopsys tools.

A large fraction of the experimental work presented in this thesis was performed at Stanford Nanofabrication Facility (SNF) and Stanford Nanocharacterization Laboratory (SNL). Credit goes to the SNF and SNL staff for their diligence in maintaining the tools. In particular, I am deeply grateful to Dr. Jim McVittie for his tireless efforts in keeping the tools up and running, and his help in setting up the ALD system. I am also thankful to the Saraswat group members for the helpful discussions and constructive feedback over the years.

Lastly, I am very thankful to my parents and my loving sister for their unwavering support and patience. There is no doubt in my mind that I would not have been able to successfully reach this major milestone in my life without their guidance and heart-felt blessings. I humbly dedicate this work to them.

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Chapter 1

Introduction

Germanium (Ge) is a promising material candidate for the next generation of semiconductor devices. In conjunction with other group IV materials - silicon (Si) and silicon-germanium alloy (SiGe), Ge has shown to deliver high-speed transistors [**1**,**2**,**3**] as well as photonic devices such as photo-detectors[**4**,**5**] and modulators [**6**]. As it has been the case with Si CMOS[1] technology, band gap and strain engineering play a critical role in optimizing the performance of Ge-based devices. For example, over 2X improvement in hole mobility can be obtained by applying compressive stress to Ge [**7**,**8**]. Similarly, tensile strain is necessary for boosting electron mobility in Ge [**9**].

The substitution of tin (Sn) into germanium (Ge) lattice to form the semiconducting $Ge_{1-x}Sn_x$ alloy is another possible route for engineering the electronic properties of Ge. The small energy separation of 140 meV between the indirect (L) and direct (Γ) conduction band valleys in Ge can be overcome by alloying with Sn as shown schematically in **Figure 1.1**, paving the path for achieving efficient light emission. The possibility of obtaining high electron and hole mobilities in the $Ge_{1-x}Sn_x$ alloy [**10**] justifies the research interest in developing $Ge_{1-x}Sn_x$ for high speed

[1] Metal-oxide-semiconductor field effect transistor (MOSFET) technology including both p-channel (pMOSFET) and n-channel (nMOSFET) devices

transistor applications. Consequently, $Ge_{1-x}Sn_x$ alloys provide a ubiquitous material platform for enabling convergence of high-speed logic and optoelectronic devices for future integrated circuits. The technological importance of $Ge_{1-x}Sn_x$ devices is further amplified by the fact that they can be integrated monolithically on a low-cost Si platform. From a device design perspective, GeSn[2] alloys expand the design space beyond Si, Ge and SiGe for greater flexibility in band gap and strain engineering.

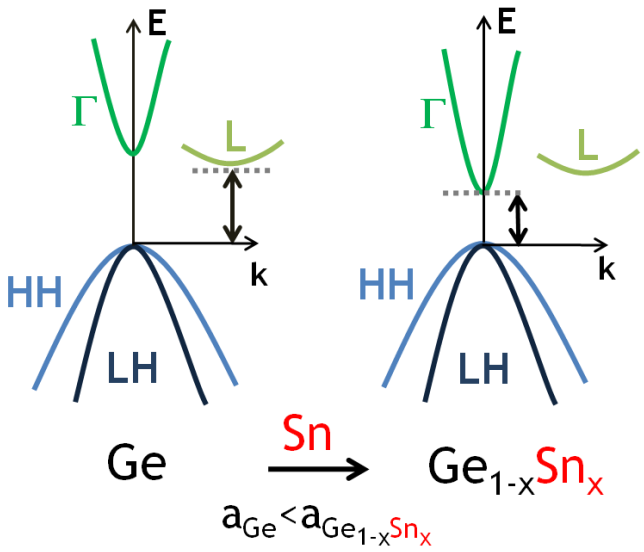


Figure 1.1 Schematic showing the effect of Sn alloying on the band structure of Ge. Addition of Sn to Ge reduces the direct energy gap more than the indirect energy gap, resulting in a direct band gap material.

Despite the immense potential of this material system, GeSn research is still in its nascent stage and the current GeSn technology severely lags behind other group IV materials such as Ge and SiGe. **Figure 1.2** gives useful insight into the evolution of research in this field over the past two decades. The sluggish pace of research in GeSn

[2] GeSn and $Ge_{1-x}Sn_x$ are used interchangeably unless otherwise noted

leading up to late last decade is mainly due to the formidable technological challenges involved in synthesis of high quality, defect-free GeSn and subsequent device fabrication – a topic of detailed discussion in the chapters to follow. Much of the initial work focused on developing techniques for GeSn material growth, while a handful of reports undertook the task of modeling the electronic band structure of GeSn. Nevertheless, recent advances in achieving device-quality material has helped set the stage for concerted research focused at understanding the properties of this material system and spurred efforts aimed towards employing GeSn for a range of semiconductor device applications.

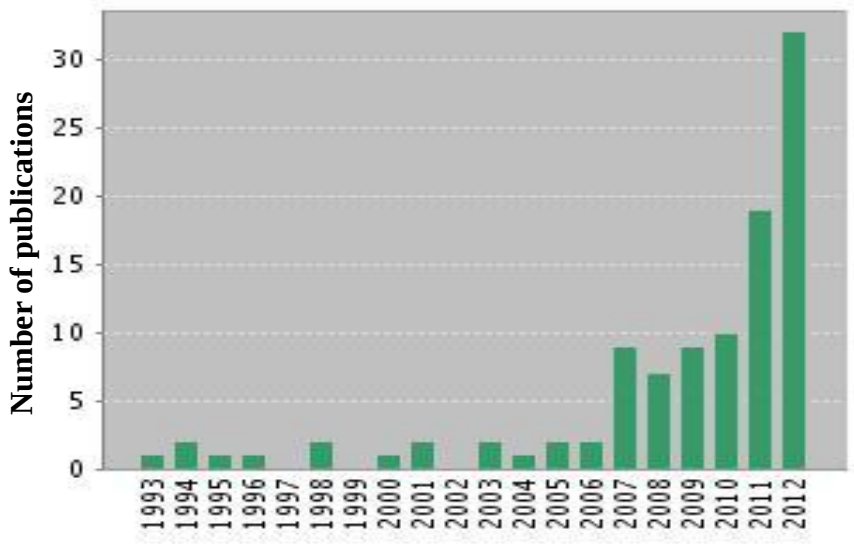


Figure 1.2 Number of published items (excluding patents) in each year related to Sn-based group IV alloys: GeSn and SiGeSn. Source: Web of knowledge © Thomson Reuters, as on Jan 31, 2013.

The goal of this dissertation, therefore, is to develop the GeSn technology in order to leverage the unique properties of this material system for realizing

semiconductor logic and optoelectronic devices, with special attention given to its applications in enabling high performance CMOS logic. The lack of significant prior art in the field of GeSn-based electronic devices allows this work to address a broad range of topics pertinent to the development of GeSn technology. These different topics are organized in this thesis as follows:

Chapter 2 presents a comprehensive understanding of the electronic band structure of $Ge_{1-x}Sn_x$ alloys. Accurate models for predicting the electronic properties are presented, followed by a detailed theoretical analysis of the transport properties of GeSn.

Chapter 3 provides a brief survey of the different methods that have been adopted for growth of GeSn. Key challenges in material synthesis and processing are discussed.

Chapter 4 investigates the use of GeSn as a channel material for CMOS applications. Details of fabrication, characterization and optimization of the performance of p and n channel MOSFETs are presented.

Chapter 5 shows how Si, Ge, Sn and their alloys can be used to engineer a FinFET based CMOS solution targeted at device dimensions for the 7 nm technology node and beyond.

Chapter 6 presents a novel etch chemistry that achieves extremely high selective etching of Ge over $Ge_{1-x}Sn_x$. The mechanism responsible for the observed etch selectivity is investigated in detail. The selective etch process is employed in

order to overcome the major challenges associated with achieving direct band gap in $Ge_{1-x}Sn_x$ alloys.

Chapter 7 summarizes this work and suggests directions for further research in the field of Sn-based group IV semiconductors.

Chapter 2

GeSn Band Structure Calculations

This chapter will present a detailed theoretical study of the electronic band structure of GeSn alloys. Using the results of band structure calculations, ballistic MOSFET simulations are carried out to gauge the performance benefits of GeSn as a channel material for nMOSFETs.

2.1 Background

Sn, the element that lies below Ge in the periodic table, exists in two allotropic forms: grey or α-Sn which has a diamond cubic lattice similar to Si, Ge and white or β-Sn which has a body centered tetragonal lattice. Here, the band structure of α-Sn is examined in more detail. The Groves-Paul model [**11**] predicts α-Sn to be a semi-metal with overlap between the conduction and valence band, resulting in a negative band gap. In a typical semiconductor, the conduction band is composed of atomic orbitals showing a predominant s character (azimuthal quantum number = 0). The valence band is derived from the $p_{1/2}$ and $p_{3/2}$ states of the free atom. For a semiconductor such as Si or Ge that show a positive band gap at the Γ point (k = 0) in the brillouin zone, the s-type conduction band lies higher in energy as compared with the p-type valence band as shown in **Figure 2.1a**. The 'band gap' defined as the energy difference

between the conduction and valence band is therefore positive. As the semiconductor lattice is expanded (by alloying Ge with Sn for example), the band gap reduces and reaches the situation shown in **Figure 2.1b,** where the conduction and valence bands become degenerate. With further expansion of the lattice (pure α-Sn, **Figure 2.1c**), the conduction band (s-state) falls lower in energy than the valence band (p-states), creating a negative band gap material. In case of α-Sn, this energy separation is -0.41 eV. The light hole band is bent upwards (positive effective mass) and degenerate with the heavy hole band. The conduction band s-state, on the other hand, shows a negative effective mass. This inverted band structure property is not unique to α-Sn, but also observed for few other heavy, large lattice constant II-VI materials such as HgTe and HgS [**12**].

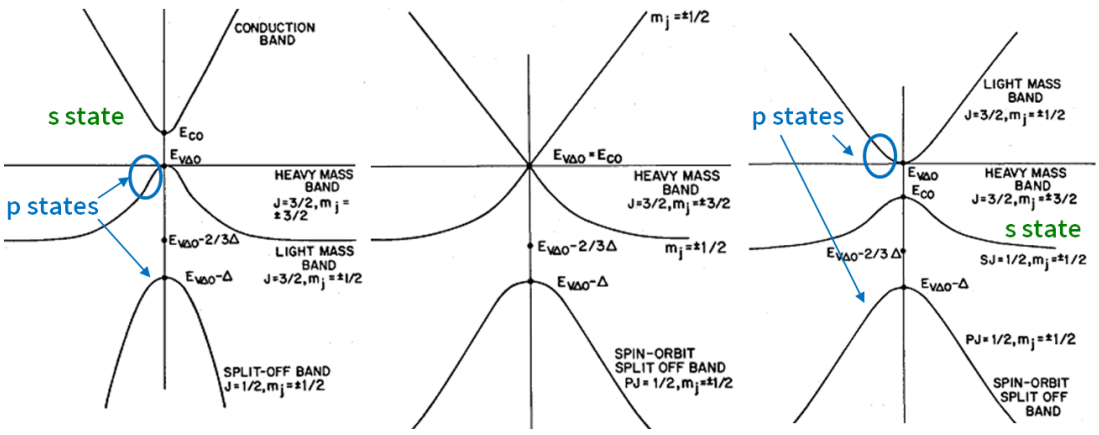


Figure 2.1 Schematic of energy bands at k = 0 for (a) positive band gap semiconductor (germanium), (b) zero band gap material, and (c) negative band gap material (α-Sn) [**12**].

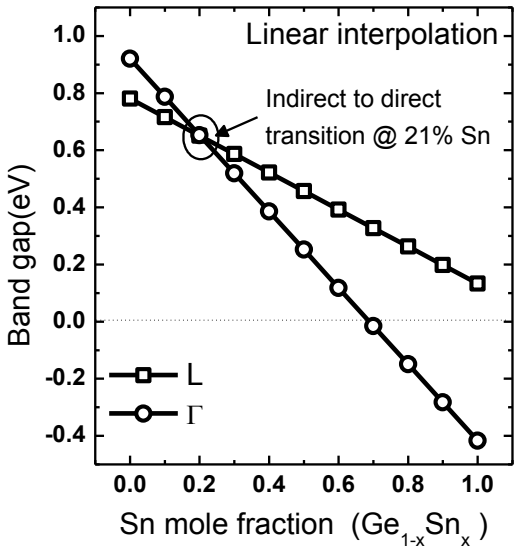


Figure 2.2 Dependence of direct (Γ) and indirect (L) band gap in $Ge_{1-x}Sn_x$ on Sn mole fraction as calculated using a linear interpolation between the band gaps of Ge and α-Sn.

As it is the case with most semiconductor alloys, the band gaps in $Ge_{1-x}Sn_x$ may be estimated using a simple linear interpolation between the band gaps of Ge and α-Sn. The variation in the direct and indirect energy gaps in GeSn as a function of alloy composition is shown in **Figure 2.2** and the alloy is predicted to show direct band gap for more than 21% Sn. More elaborate simulation models for calculating the GeSn band structure have been proposed in the literature, yielding quite a large variation in the predicted Sn composition at which the material transitions from indirect to direct band gap. For example, tight-binding calculations using the virtual crystal approximation (VCA) of [**13**] predicts GeSn to become direct gap material for alloy Sn composition > 20%. Band structure calculation using the 'supercell mixed-atom method' [**14**] requires 17% Sn in order to induce the indirect-to-direct band gap

transition in GeSn. The band anti-crossing model proposed in [**15**] requires 14% Sn for this transition. On the other hand, first principles electronic band structure calculations based on density functional theory (DFT) of Yin et al. [**16**] predict a much lower alloy Sn% of 6.3% for the indirect to direct band gap crossover in GeSn alloys. Also, the recent experimental investigations of [**17**] and [**18**] based on photoluminescence study of strain-free GeSn layers suggest the onset of direct gap at approximately 7-8% Sn. Clearly, huge discrepancy exists in literature over the some of the most important properties of GeSn, warranting the development of more accurate simulation models for GeSn.

2.2 Density functional theory

Density functional theory (DFT) is an important class of first principles (*ab-initio*) modeling methods for studying the electronic and structural properties of various solid state and molecular materials. DFT owes its origins to two seminal papers by Hohenberg-Kohn[**19**], Kohn-Sham[**20**] that establish the fundamentals of this method through the following two theorems:

1. The Hamiltonian operator and the ground-state properties of a many-electron system are uniquely determined by an electron density $n(\vec{r})$ that depends on only 3 spatial coordinates.
2. The functional that delivers the ground-state energy of the system, delivers the lowest energy if and only if the input electron density is the true ground state density.

Consequently, the electron density forms the central quantity in DFT.

Within the framework of DFT, the intractable many-body problem of interacting electrons in a static external potential is reduced to a tractable problem of non-interacting electrons moving in an effective potential. The effective potential includes the external potential and the effects of the Coulomb interactions between the electrons, e.g., the exchange and correlation interactions. Physical quantities of interest such as the electron wavefunctions, total energies etc. are then expressed as functional of the electron density. A major challenge in DFT is that the exact functionals for exchange and correlation are not known except for the free electron gas. The exchange-correlation functional is typically estimated using the local density approximation (LDA) in which the exchange-correlation energy depends solely on the value of the electron density at a point in space. Another commonly adopted method is the generalized gradient approximation in which the exchange-correlation energy depends on both the local electron density (GGA) of the electrons as well as the gradient of the electron density $\vec{\nabla} n(\vec{r})$.

It has been found that local (LDA) and semi-local (GGA) approximations for the exchange-correlation functional tend to severely underestimate energy gaps in Ge and Sn[**21**]. These standard approximations for exchange-correlation delocalize the electron density over the entire crystal such that each electron experiences an average of the Coulombic potential. For highly correlated materials, the large Coulombic repulsion between localized electrons might not be well represented by a functional such as the LDA or GGA. As a result, LDA/GGA fails to capture the orbital dependence of the Coulomb interactions. A way to avoid this problem is to add a

localized term to the density functional. This approach is known as LDA/GGA+*U* [**22**].

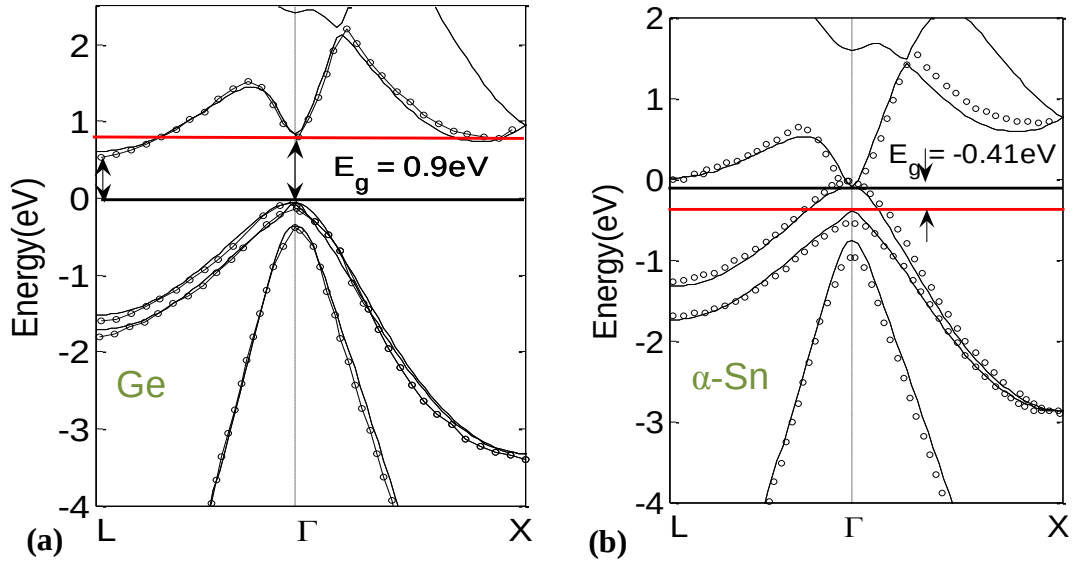


Figure 2.3 Electronic band structure of **(a)** Ge and **(b)** α-Sn calculated using GGA+U. Lines: GGA+U, symbols: Non-local empirical pseudopotential calculations fitted to experimental data[**23**]. The red-line denotes the conduction band extremum.

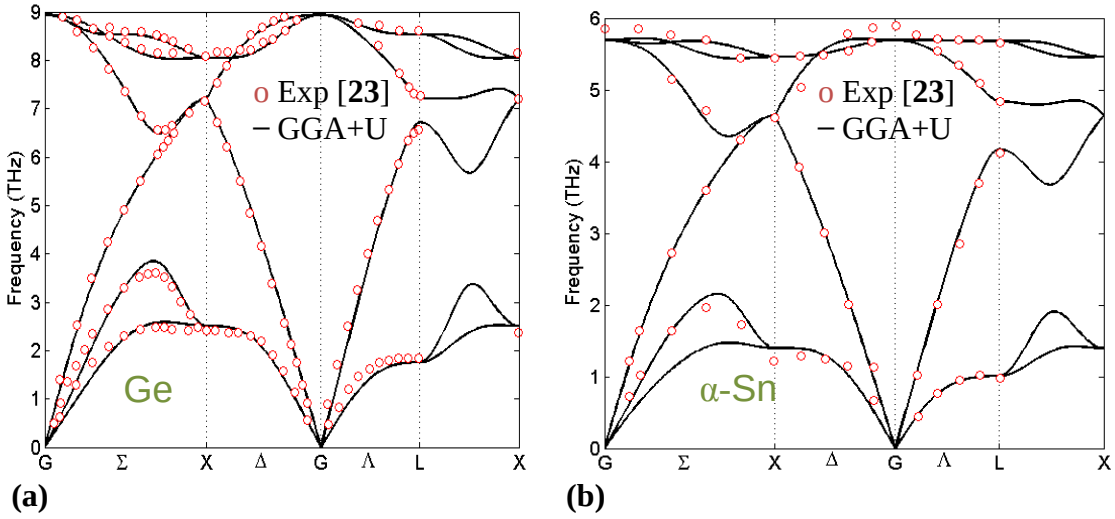


Figure 2.4 Phonon band structure of **(a)** Ge and **(b)** α-Sn calculated using GGA+U. Experimental data taken from[**23**].

Here, the electronic structure of Ge, Sn and GeSn are calculated using DFT as implemented in the Vienna Ab Initio Simulation Package (VASP) [**24**,**25**]. For the exchange-correlation functional, GGA with corrections for on-site Coulomb interactions (GGA+*U*) is used to estimate structural and electronic properties of Ge, Sn and GeSn. *U* is treated as an empirical parameter and adjusted iteratively in order to reproduce both the electronic as well as the phonon band structure of elemental Ge and α-Sn in agreement with experiments. The *U* corrections are applied only to the p-orbitals (azimuthal quantum number $l = 1$). **Figure 2.3** shows the comparison of the electronic band structure of Ge and α-Sn calculated using DFT-GGA+*U* with the band structure calculated using the non-local empirical pseudopotential method. The empirical pseudopotential band structure is fitted to the experimentally available data for the energy gaps in Ge and α-Sn. Similarly, **Figure 2.4** shows phonon band structure of Ge and α-Sn calculated using DFT-GGA+*U* and compares them with the experimental results catalogued in [**23**]. The values of *U* used in these calculations are -3.13 eV and -3 eV for Ge and α-Sn, respectively. The results from DFT calculations using GGA+*U* for Ge and α-Sn are in excellent agreement with the experimental data, suggesting that the calculation methodology adopted here is well-suited for estimating the properties of both Ge and α-Sn.

Next, the DFT-GGA+*U* method is extended for calculating the properties of substitutional GeSn alloy. The atomic structure of the alloy can be constructed by forming supercells of the 8-atom unit cell of the simple diamond cubic lattice. Therefore, a (2x1x1) and (2x2x1) supercells contains 16 and 32 atoms, respectively.

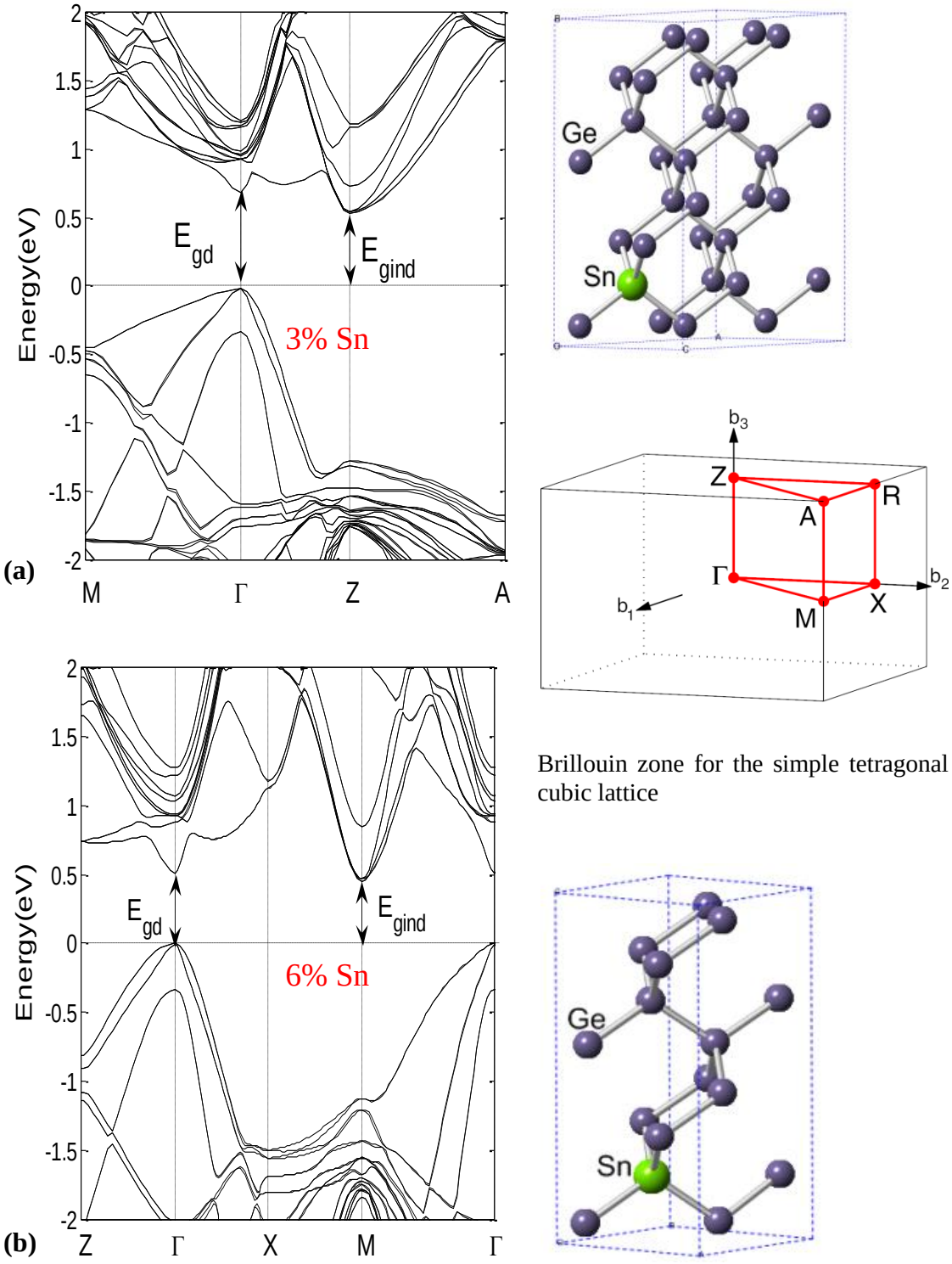


Figure 2.5 (a) Band structure of GeSn showing the direct and the indirect band gaps. **(a)** 3% Sn **(b)** 6% Sn.

A 32-atom supercell composed of 31 Ge atoms and 1 Sn atom yields a substitutional GeSn alloy with ~3% Sn. Similarly, in a 16-atom supercell, replacing 1 Ge atom with Sn gives an alloy with ~6% Sn. Since all atomic positions in the 8-atom diamond cubic unit cell are identical, the precise location of the Sn atom in the supercell is irrelevant. The supercells thus constructed represent the primitive cell of the ordered alloy for the given Sn%. After constructing the primitive cell for the alloy, the atoms positions are allowed to relax with a total energy convergence tolerance of 10^{-6} eV/ atom and the ground-state is obtained when the inter-atomic force is less than 0.001 eV/Å. The calculated electronic band structures of the relaxed GeSn alloy with 3% and 6% Sn are shown in **Figure 2.5**. Note that during these calculations, the *U* parameter for Ge and Sn is kept fixed to the values determined previously.

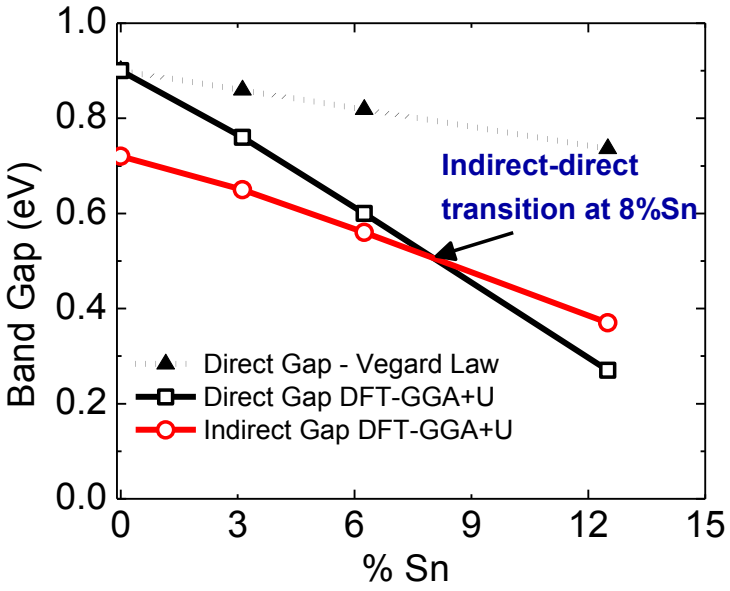


Figure 2.6 Direct and indirect band gap in GeSn as a function of the alloy composition. Indirect to direct band gap transition is expected at ~8% Sn.

The direct and the indirect band gaps can be extracted from these calculations and plotted as a function of alloy Sn%. This is done in **Figure 2.6** and the indirect to direct energy gap crossover is found to occur at ~8% Sn. Note that the values of direct band gap calculated here shows quite a considerable deviation from the values determined using the linear interpolation between band gaps of Ge and α-Sn (see **Figure 2.2**). As mentioned previously, experimental investigations of [**17**] and [**18**] suggest the onset of direct gap at approximately 7-8% Sn. Thus the results from DFT calculations are in good agreement with the experimental data.

The DFT-GGA+*U* methodology developed here for GeSn provides a powerful and robust framework for a more detailed theoretical study of this material system. However, the large computational overhead involved in these calculations limits its applicability to device level simulation that typically involves thousands of atoms. Empirical methods can be powerful approaches to model the alloy properties if the desired accuracy can be achieved.

2.3 Empirical pseudopotentials

The empirical pseudopotential method (EPM) has been employed with remarkable success to calculate electronic structure properties of other group IV elements and alloys namely Si, Ge and SiGe [**9**]. The EPM is chosen here due to the relatively small number of empirical parameters required to obtain a given material's band structure. Following the seminal work of Chelikowsky and Cohen [**26**], the single electron pseudo Hamiltonian including spin orbit coupling is written as:

$$H(G,G') = -\frac{\hbar^2}{2m}\nabla^2 + V_{loc}(|G-G'|) + V_{nloc}(G,G') + V_{so}(G,G') \tag{2.1}$$

V_{loc}, V_{nloc} and V_{so} represent the local, non-local and spin orbit contributions to the pseudopotential respectively. A basis set {G} consisting of 137 plane waves is used to expand the pseudopotential in the reciprocal space. V_{loc} depends only on the magnitude of the reciprocal lattice vector $q=|G-G'|$ and V_{nloc} captures the angular momentum dependence of the pseudopotential. For pure unstrained elements, the knowledge of local pseudopotential form factors at only certain discrete magnitude values of reciprocal lattice vector q suffices to reproduce the band structure. However for band structure calculation of GeSn alloy, strained Ge, Sn and GeSn, local pseudopotential at an arbitrary reciprocal vector q is required and obtained by performing cubic spline interpolation between local pseudopotential form factors V_{loc} at $q^2=\{0, 3, 8, 11\}^* (2\pi/a_0)^2$. As in [**27**], V_{loc} at $q^2=0$ is extrapolated to $-2E_F/3$ where E_F is the free electron Fermi-energy. Also, in order to ensure fast cut-off of the potential at large q^2 the approach outlined in [**28**] is adopted:

$$V_{loc}(q) = V_{cubic}(q)\left(\tfrac{1}{4}\tanh\left(\frac{a_5 - q^2}{a_6}\right) + \tfrac{1}{4}\right), \qquad V_{cubic}(q) = a_1 q^3 + a_2 q^2 + a_3 q + a_4 \tag{2.2}$$

The overlap integrals $B_{nl}(K)$ needed for evaluation of the matrix elements for spin orbit interaction are estimated using the analytical expression [**27**]:

$$B_{nl}(K) = \frac{5-(K/\zeta)^2}{5\left(1+(K/\zeta)^2\right)^4} \tag{2.3}$$

Table 2.1 lists the values of pseudopotential parameters used for Ge and Sn. Remaining pseudopotential parameters have been slightly modified from those in [**9**] and [**26**] so as to reproduce as closely as possible the band structure of Ge and Sn of [**26**]. The calculated band structure of elemental Ge and α-Sn are shown in **Figure 2.7**.

Table 2.1 Pseudopotential parameters used for Ge and Sn. Nonlocal parameters taken from [**26**]. [a][**27**], [b][**26**]

		Unit	***Ge***	***Sn***
Lattice constant		Å	5.646	6.490
Interpolation coefficients	a_1	atomic units	-0.1684	-0.1186
	a_2		0.4956	0.3159
	a_3		-0.0077	0.0809
	a_4		-0.5650	-0.4276
	a_5		5.0	4.0
	a_6		0.3	0.3
Spin orbit parameters	ζ	$Å^{-1}$	10.09[a]	7.81
	μ	Ry	0.000965[a]	0.00225[b]
$2C_{12}/C_{11}$	D_{001}		0.751	0.849

It must be noted that using the spin orbit parameters listed in **Table 2.1** and approximation of equation(2.3), the large spin orbit coupling of 0.8 eV observed in the case of α-Sn is reproduced accurately by the non-local EPM.

For GeSn alloy, the lattice constant has been assumed to be described by

$$a_{Ge_{1-x}Sn_x} = (1-x)a_{Ge} + xa_{Sn} - \theta_{GeSn}(1-x)x \tag{2.4}$$

θ_{GeSn} is the lattice bowing parameter and assumed to be equal to -0.166Å [**29**].

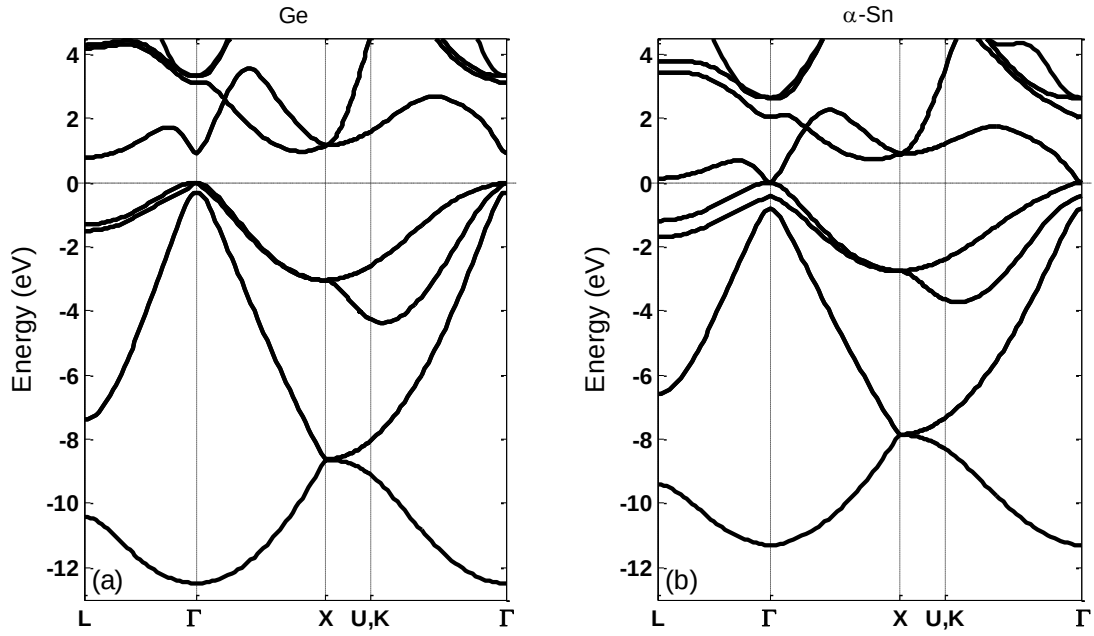


Figure 2.7 Band structure of Ge and α-Sn calculated using the nonlocal empirical pseudopotential method (NL-EPM)

2.3.1 GeSn band structure

For calculation of GeSn alloy band structure, the virtual crystal approximation (VCA) is invoked. The VCA representation of a random alloy assumes the alloy to be composed of 'virtual' atoms producing a periodic crystal potential modeled as composition weighted average of constituent element potentials. Band structure for GeSn alloy with varying Sn content is calculated using the NL-EPM method outlined

above and the alloy pseudopotential as determined by the VCA. The calculated band gaps at high symmetry points in fcc brillouin zone are shown in **Figure 2.8** and fitted to a second order equation in alloy Sn composition *x:*

$$E_g^{Ge_{1-x}Sn_x} = (1-x)E_g^{Ge} + xE_g^{Sn} - b_g(1-x)x \tag{2.5}$$

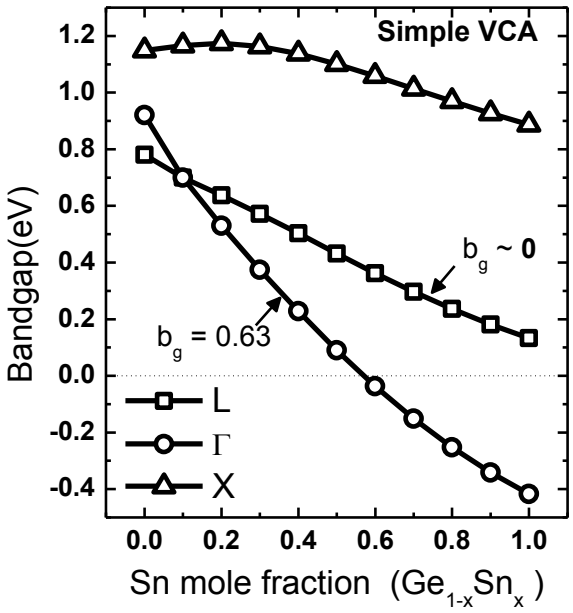


Figure 2.8 Band gap at high symmetry points in the brillouin zone for GeSn alloys calculated using the conventional VCA.

b_g is called the band gap bowing parameter and measures the deviation of the alloy band gap from a linear interpolation between the band gaps of constituent elements. Several experimental studies [**17**,**18**,**30**] have found GeSn alloys to exhibit a large bowing parameter (b_g ~ 2.1eV at 300K [**17**]) for the direct band gap. However, as shown in **Figure 2.8**, the conventional VCA representation of GeSn alloy severely underestimates the direct band gap bowing in GeSn (b_g = 0.63 eV). This suggests that VCA is insufficient in accurately describing GeSn alloys.

Investigations into the applicability of the VCA to model semiconductor alloys has been the subject of several theoretical reports [**31**,**32**,**33**,**34**,**35**]. The disagreement between the alloy band gap bowing predicted by VCA and that observed experimentally is typically attributed to the failure of potential averaged VCA formalism to adequately capture the effect of random potential fluctuations on alloy crystal potential. Also, the effect of potential fluctuations arising due to alloy disorder are expected to be pronounced for a highly lattice mismatched system such as Ge (a_0 = 5.64Å) and Sn (a_0 = 6.49 Å). Hence, in order to correctly account for the effect of large mismatch between Ge and Sn, a correction term is added to VCA alloy potentials representing the combined effect of structural and compositional disorder in the alloy, similar to the approach described in [**35**]. In order to limit the number of additional parameters introduced in the simulation model, the disorder corrections are applied only to the local component of alloy pseudopotential:

$$V_{loc}^{Ge_{1-x}Sn_x}(q) = (1-x)\frac{\Omega_{Ge}}{\Omega_{Ge_{1-x}Sn_x}}V_{loc}^{Ge}(q) + x\frac{\Omega_{Sn}}{\Omega_{Ge_{1-x}Sn_x}}V_{loc}^{Sn}(q) - (1-x)xP_{loc}\frac{\left(\Omega_{Ge}V_{loc}^{Ge}(q) - \Omega_{Sn}V_{loc}^{Sn}(q)\right)}{\Omega_{Ge_{1-x}Sn_x}} \quad (2.6)$$

Ω is the primitive cell volume, x is the mole fraction of Sn in the alloy and P_{loc} is a fitting parameter. First two terms in the above equation correspond to the potential averaged VCA and the effective alloy disorder potential is represented by the last term. **Figure 2.9** shows the dependence of direct energy gap on the numerical value of P_{loc}. P_{loc} equal to zero reverts to the case of conventional VCA whereas a negative value of P_{loc} increases the direct gap bowing b_g.

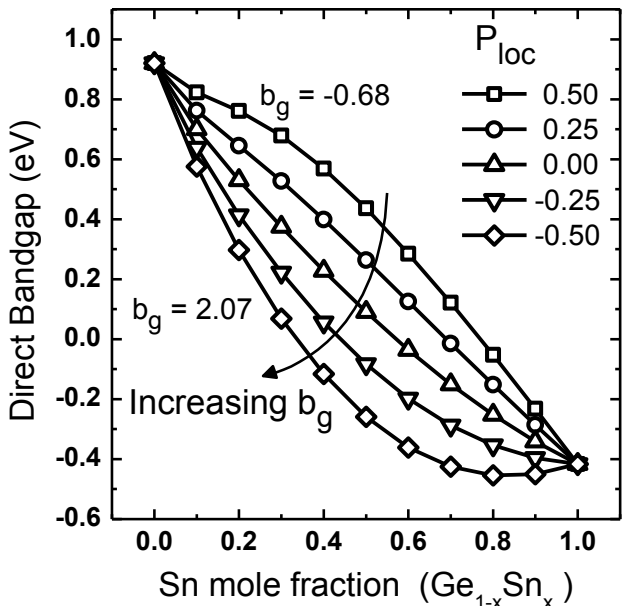


Figure 2.9 Dependence of the direct band gap bowing on the value of P_{loc} used in equation (2.6).

In **Figure 2.10a**, P_{loc} is adjusted to fit to the direct gap b_g of 2.1 eV as determined experimentally in [**17**]. The resulting indirect gap bowing has been found to be equal to 0.91 eV and the indirect to direct band gap transition has been found to occur at alloy Sn% of 6.5%. Also, negligible change in Δ energy gap has been observed for Sn composition < 20%, resulting in an increase in L-Δ energy gap. A comparison of the calculated direct gap with the experimental data [**17**,**18**] measured at 300 K is shown in **Figure 2.10b**. The NL-EPM calculations are performed assuming lattice temperature of 0 K and do not take into account the effect of temperature on band structure. Hence there is an energy offset between calculated band gap and the band gap measured at 300 K.

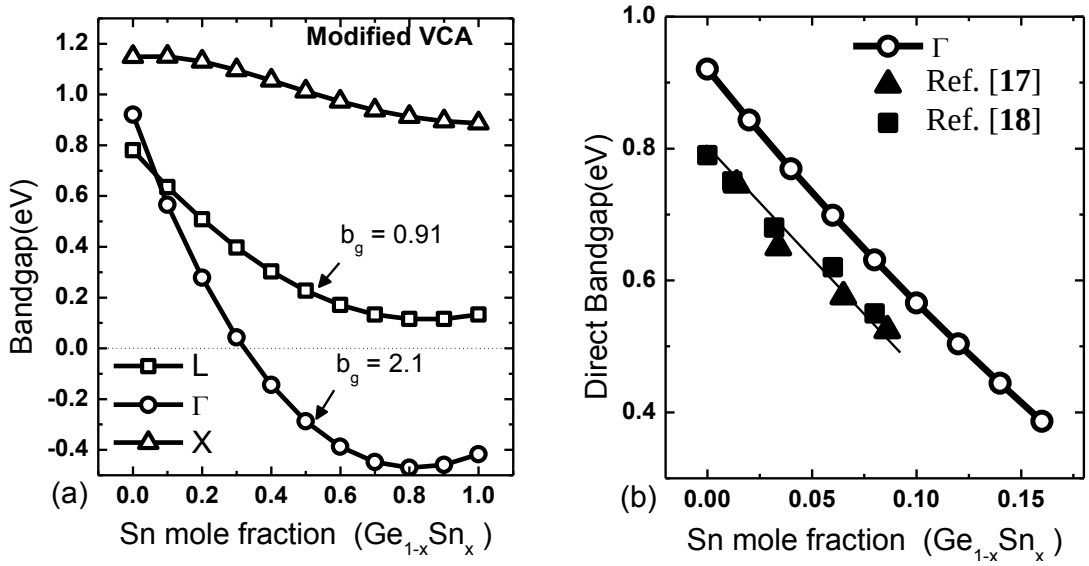


Figure 2.10 (a) Band gap at high symmetry points in the brillouin zone for GeSn alloys using VCA corrected for alloy compositional and structural disorder (modified VCA). **(b)** Comparison of the calculated direct gap with experimental data measured at 300 K as in [**17**,**18**].

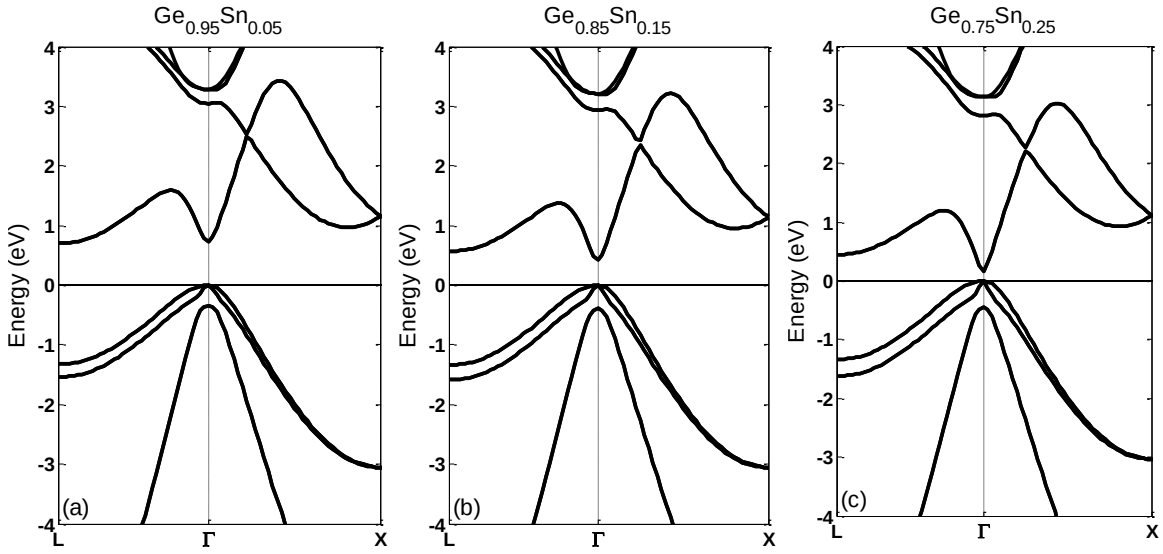


Figure 2.11 Calculated band structure for GeSn with (a) 5% Sn, (b) 15% Sn and (c) 25% Sn.

The calculated band structure for GeSn with Sn% as 5%, 15% and 25% are shown in **Figure 2.11**. The spin orbit coupling ΔV_{so} in $Ge_{1-x}Sn_x$ shows negligible bowing and follows closely the linear relation in alloy Sn composition *x:*

$$\Delta V_{so}^{Ge_{1-x}Sn_x} = (1-x)\Delta V_{so}^{Ge} + x\Delta V_{so}^{Sn}, \tag{2.7}$$

where ΔV_{so}^{Ge} = 0.29eV and ΔV_{so}^{Sn} = 0.8eV. A closer inspection of changes in the band structure upon increased Sn incorporation reveals that as the direct band gap shrinks, the electron and hole valleys at Γ point become increasingly 'sharp'. In other words, the curvature effective mass for electron and holes proportional to $\left[\partial^2 E/\partial k^2\right]^{-1}$ decreases with decreasing direct band gap.

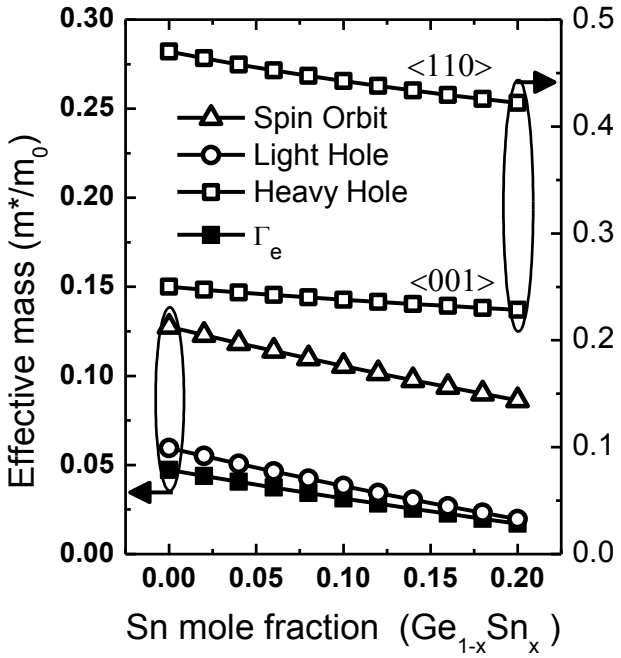


Figure 2.12 Calculated electron and hole effective masses at Γ point as a function of Sn composition in GeSn.

In fact, from **k.p** perturbation theory one can arrive at the conclusion that the effective mass of light hole and Γ electrons is proportional to the direct energy gap. A similar trend is observed in our simulation results. As the Sn content in GeSn increases, effective masses at Γ point decreases for both electrons and holes as shown in **Figure 2.12**. Interestingly, electron effective masses in GeSn at the satellite L and Δ conduction valley minima are found to be practically unchanged from those in Ge.

2.3.2 Strained GeSn alloys

The small energy separation of 140 meV between indirect (L) and direct (Γ) conduction band valleys in Ge can also be overcome by inducing tensile strain [**9**,**36**], motivating numerous research efforts aimed towards engineering Ge in order to achieve direct band gap. Consequently, several solutions have been proposed to introduce tensile strain in Ge thin films – such as micromechanical strain [**37**,**38**,**39**] and epitaxial growth of Ge on larger lattice constant buffer layers [**40**]. The effect of application of tensile strain on the band structure of Ge is qualitatively similar to that of alloying Ge with Sn. This raises an interesting possibility of employing tensile strained GeSn alloys for achieving a direct band gap material.

As will be discussed in detail in the next chapter, the low solid solubility (<1%) of Sn in Ge renders growth of high quality, defect free GeSn containing even a few atom % Sn a difficult task. However, recent advances in non-equilibrium growth techniques have made it possible to achieve GeSn with alloy substitutional Sn% exceeding 8%. Nevertheless, increasing Sn% in the alloy raises concerns regarding the thermal stability of the material and the maximum allowable thermal budget

during device fabrication. On the other hand, the approach of relying on strain alone to induce direct gap in Ge necessitates use of specialized, non-conventional techniques such as suspended thin film Ge membranes to achieve the large amount of tensile strain (~1.5%) needed for indirect to direct band gap transition. Recent attempts employing these techniques have at best been able to achieve 1.1% biaxial tensile strain [**37**,**38**] – falling short of the requirement for onset of direct band gap. A combination of strain and Sn alloying i.e., strained GeSn alloys may be able to relax the requirements on both the amount of Sn as well as the tensile strain needed for inducing indirect to direct band gap crossover, thereby offering a more practical route towards achieving a direct band gap material.

The effects of biaxial strain on GeSn alloy band structure are investigated using the NL-EPM method described in previous sections. In the analysis presented here, a uniform stress applied in the [001] direction that produces a diagonal strain tensor with $e_{xx} = e_{yy} = e_{\parallel}$ and $e_{zz} = e_{\perp}$ is considered. The in-plane $e_{\parallel}$ and out of plane $e_{\perp}$ strain components are related by $e_{\perp} = -D_{001} e_{\parallel}$, where $e_{\parallel} = \left(a_{\parallel} - a_0\right) / a_0$. The values of D_{001} used for Ge and Sn are listed in **Table 2.1**. D_{001} for the alloy is taken as a linear interpolation between the values for Ge and Sn. **Figure 2.13a** plots the lowest energy gap in GeSn under biaxial strain. The corresponding energy separation between L and Γ valley conduction band minima is illustrated in **Figure 2.13b**. For pure Ge, a tensile strain of 1.5% is necessary to induce a direct gap. Under large compressive strain, the four fold degenerate Si like Δ_{100} valleys are pushed lower in energy than the L valleys.

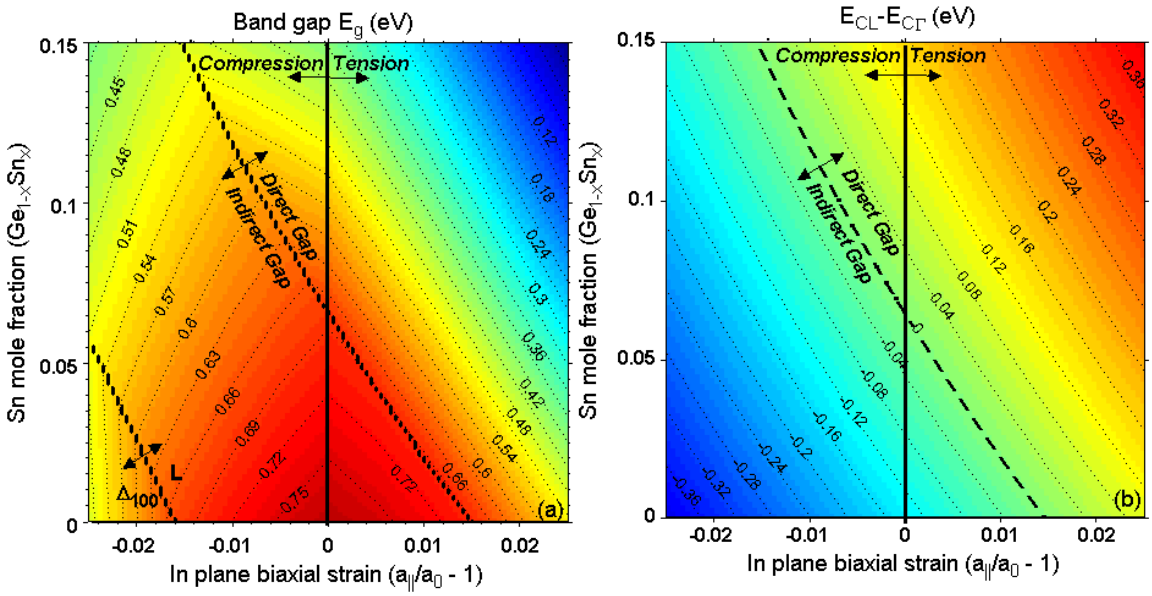


Figure 2.13 (a) Contour plot of lowest energy gap in GeSn. Band gap values in eV are given on the contour plot **(b)** E_{CL}-$E_{C\Gamma}$: Energy separation between the L and Γ conduction band minima as a function of in plane biaxial strain and alloy Sn composition for [001] stress. E_{CL}-$E_{C\Gamma}$ values in eV are given on the contour plots.

As seen in the previous section, strain-free GeSn shows transition to direct band gap material at 6.5% Sn. From **Figure 2.13a,** the combination of strain and Sn alloy % at which Γ and L valleys are degenerate can be expressed in closed form as:

$$f(x,e_{\|}) = 15.38x + 1.02xe_{\|} + 0.67e_{\|} - 1 = 0 \qquad (2.8)$$

, where $e_{\|}$ is the in plane component of the strain and x is alloy Sn%. Values of x and $e_{\|}$ for which $f(x,e_{\|}) > 0$ represents cases under which the material exhibits direct band gap. As evident from **Figure 2.13**, the amount of biaxial strain required to achieve direct band gap reduces as the alloy Sn% increases and vice versa.

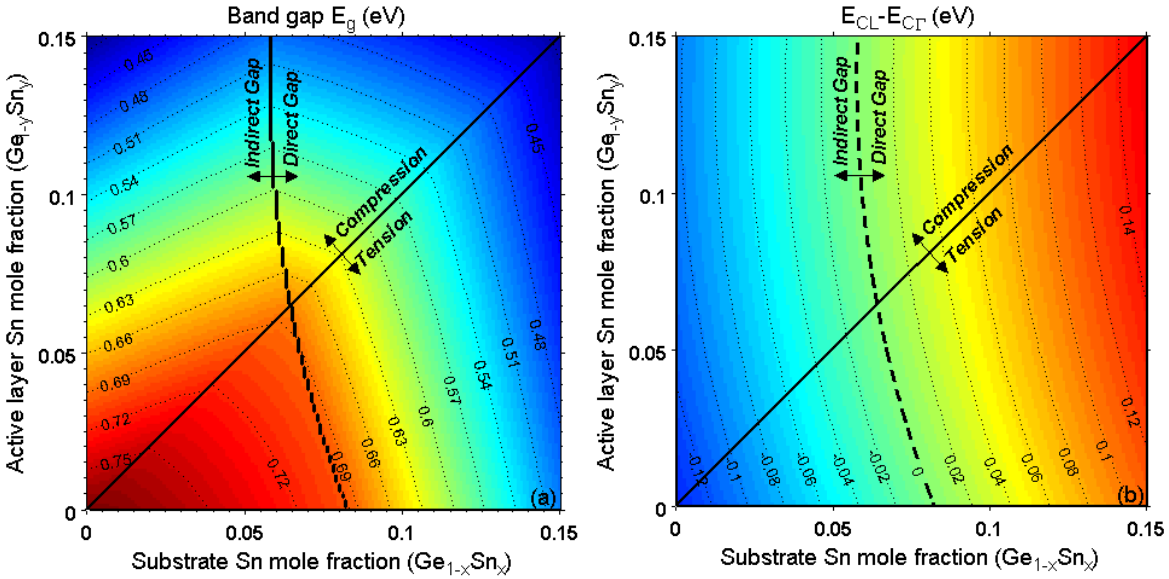


Figure 2.14 (a) Lowest energy gap and **(b)** E_{CL}-$E_{C\Gamma}$: Energy separation between the L and Γ conduction band minima in $Ge_{1-y}Sn_y$ grown pseudomorphically on (001) unstrained $Ge_{1-x}Sn_x$. Band gap and E_{CL}-$E_{C\Gamma}$ values in eV are given on the contour plots.

A commonly adopted method to induce strain in thin films is through epitaxial growth on lattice mismatched buffer layers. $Ge_{1-y}Sn_y$ grown pseudomorphically on strain relaxed $Ge_{1-x}Sn_x$ buffer layers is considered for further analysis. The active layer of $Ge_{1-y}Sn_y$ is under tensile strain if $y<x$ and under compression for $y>x$. The lowest energy gap in the active (top) $Ge_{1-y}Sn_y$ layer for such a configuration is shown in **Figure 2.14a** with corresponding L-Γ energy separation presented in **Figure 2.14b**. The set (x, y) of substrate Sn content x and active layer Sn content y at which the active layer $Ge_{1-y}Sn_y$ transitions to direct band gap can be obtained as solutions to the equation:

$$g(x,y)=12x+4.75y-18.5y^2-1=0,(x,y)\in[0,0.15] \quad (2.9)$$

It is interesting to note that no indirect to direct transition is observed for $Ge_{1-y}Sn_y$ grown pseudomorphically on Ge (x = 0 in equation(2.9)). The reduction in L-Γ energy separation obtained by Sn alloying is offset almost completely by the compressive strain arising due to growth of $Ge_{1-y}Sn_y$ on Ge substrate. Nevertheless, it is evident from **Figure 2.13** and **Figure 2.14** that a combination of strain and Sn alloying is a versatile method for tuning the band structure properties of Ge.

2.4 Ballistic electron transport simulations

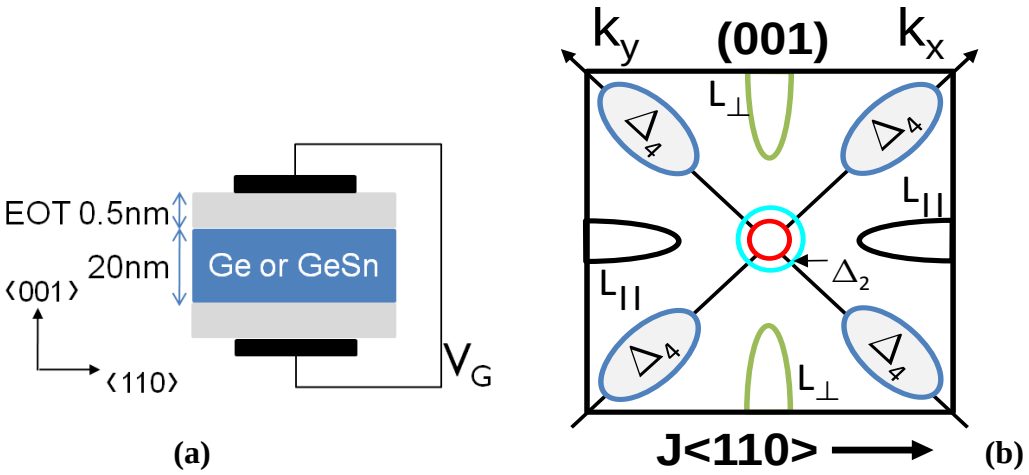


Figure 2.15 (a) Double-gate MOSFET used for ballistic transport simulations **(b)** Projection of equivalent conduction band valleys on the k_x-k_y plane for (001) oriented substrate.

The results from EPM band structure calculations are used in the ballistic MOSFET model [**41**] to estimate the inversion charge density, sub-band structure and source injection velocity (V_{inj}) in a double gate nMOSFET structure with 20 nm body thickness and 0.5 nm EOT with Ge or GeSn as channel material. The substrate is

assumed to be (001) oriented and the channel direction considered is along the <110> direction. Within the framework of the ballistic MOSFET model, the transport of electrons from the source to drain is assumed to occur without any scattering in the channel region. **Figure 2.15** shows the projection of equivalent conduction band valleys in Ge, GeSn on the k_x-k_y plane. $L_{||}$ indicates L valleys with major axis along the channel direction and have larger transport effective mass than the $L_{\perp}$ valleys. In-plane Δ valleys (Δ_4) and out-of-plane Δ valleys (Δ_2) have degeneracy of 4 and 2 respectively.

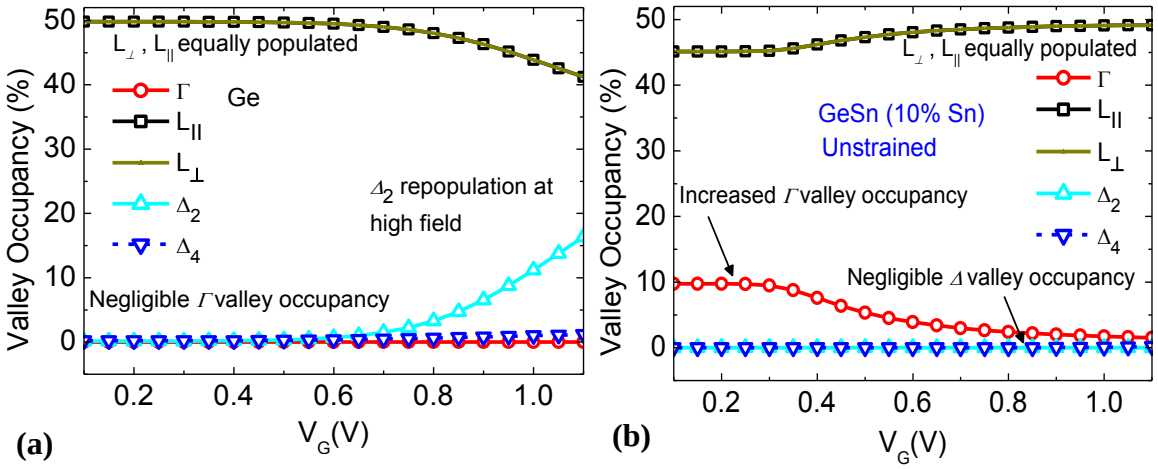


Figure 2.16 Relative valley occupancy for (a) Ge and (b) Unstrained GeSn (10% Sn) channel double gate nMOSFETs.

Figure 2.16 shows the calculated relative valley occupancies as a function of applied gate bias for Ge and unstrained GeSn (10%Sn) as channel material. Since, $L_{||}$ and $L_{\perp}$ valleys have same effective mass (m_z) in the confinement direction, they are equally populated. In case of Ge, the energy separation of 140meV between Γ and L valleys prevents any significant population of Γ valley. At high gate bias, large sub-

band splitting in L valleys causes carrier spill over to Δ_2 valley with larger confinement effective mass (m_z) and high transport effective mass ($m_{||}$). From NL-EPM calculations shown in **Figure 2.10**, unstrained GeSn with 10% Sn is direct bandgap with Γ valley ~40meV below L valley. As a result, increased population of low $m_{||}$ Γ valley is observed in GeSn with 10% Sn. Alloying with Sn lowers both Γ and L valleys without significantly affecting the Δ valley thereby eliminating the carrier spill over to Δ valley observed in Ge.

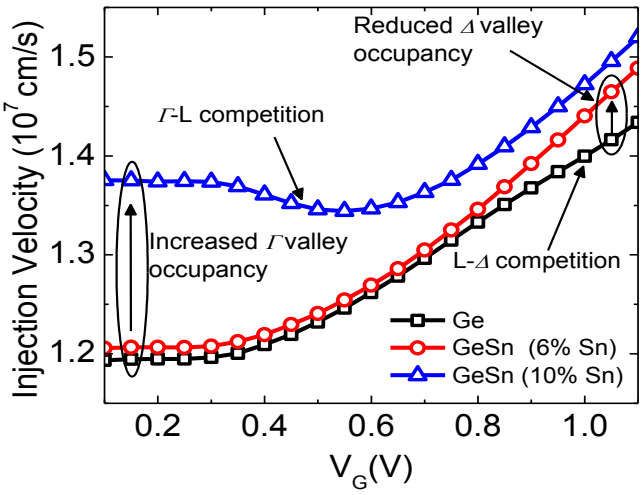


Figure 2.17 Comparison of source injection velocity (V_{inj}) double gate nMOSFETs with Ge, unstrained GeSn (6%Sn, 10%Sn) channel.

Population of valleys with low effective mass in the transport direction results in increase in the source injection velocity V_{inj} and the ballistic drive current of the device. As shown in **Figure 2.17**, for direct gap GeSn (Sn > 7%) increased population of Γ valley boosts V_{inj}. For both direct gap (10% Sn) and indirect gap (6% Sn) GeSn, increase in L-Δ energy gap inhibits Δ valley occupancy at large gate voltages and prevents the V_{inj} degradation seen in Ge. Thus, improvement over Ge nMOSFETs in

terms of electron V_{inj} (or equivalently, ballistic drive current) can be expected for GeSn channel nMOSFETs throughout the operating gate voltage range.

2.4.1 Compressive strain in GeSn

As will be discussed in the next chapter, state-of-the-art in GeSn growth relies on the use of a strain-relaxed Ge buffer to enable defect-free epitaxial growth and to achieve Sn incorporation beyond the solid solubility limit of 1%. Due to the larger lattice constant of GeSn than Ge, GeSn is fully biaxially compressed (pseudomorphic) with respect to Ge when grown epitaxially on Ge. Since Ge and GeSn have similar valence band structure, compressive strain in GeSn is expected to boost the hole mobility and pMOSFET drive current through a mechanism similar to that in Ge [**9**]. Here, the effect of compressive strain on nMOSFET performance is examined in more detail.

NL-EPM calculations presented in section 2.3.2 show that that biaxial compression in GeSn increases the direct energy gap and reduces the L-Δ_4 energy gap. **Figure 2.18** shows the energies of different conduction band minima in GeSn grown pseudomorphic to Ge. Unlike in case of unstrained GeSn no indirect to direct gap transition is observed for GeSn pseudomorphic to Ge. Therefore, for compressively strained GeSn negligible Γ valley occupancy is observed and electrons preferentially fill high effective mass Δ_4 valleys causing a reduction in V_{inj}. Hence, compression in GeSn layer resulting from growth on Ge offsets any improvements in nMOSFET performance expected from GeSn (**Figure 2.19**)

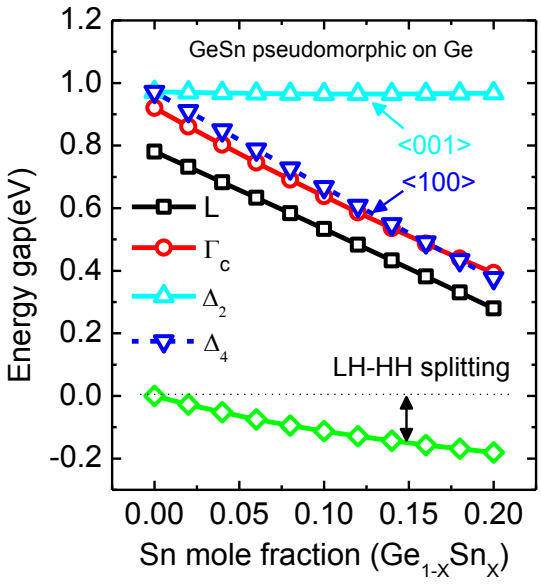


Figure 2.18 Band gap at critical points for GeSn grown on Ge. GeSn layer is under biaxial compression when grown epitaxially on Ge (001).

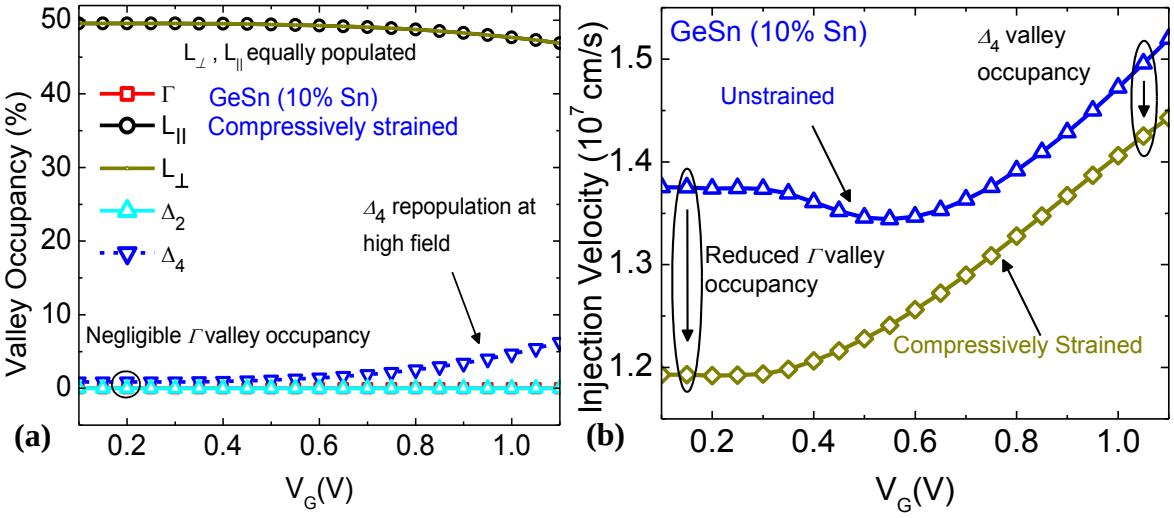


Figure 2.19 (a) Relative valley occupancy for GeSn compressively strained with respect to Ge. **(b)** Comparison on V_{inj} for strained and unstrained GeSn (10%Sn) channel double gate MOSFETs

2.5 Summary

The electronic properties of the GeSn alloy were examined through first principles and empirical methods. An empirical pseudopotential based method was developed for calculating the electronic band structure of GeSn alloys. Application of corrections to the virtual crystal potential in order to account for the large lattice mismatch between Ge and Sn was shown to reproduce band gaps in agreement with experiments. The effect of biaxial strain on the band structure properties of GeSn alloys was analyzed in detail.

Furthermore, ballistic transport model was used to provide valuable insights into material requirements for high performance CMOS using GeSn channel as the channel material. Significant benefits in nMOSFET performance can be achieved by employing GeSn as channel. However, compressive strain in GeSn grown on Ge has been shown to offset any gain in nMOSFET performance obtained by alloying Ge with Sn. Enhancement in GeSn nMOSFETs can be obtained by growth of GeSn on relaxed SiGeSn buffer layers in order to achieve strain-free GeSn or introduce tensile strain in GeSn channel.

Chapter 3

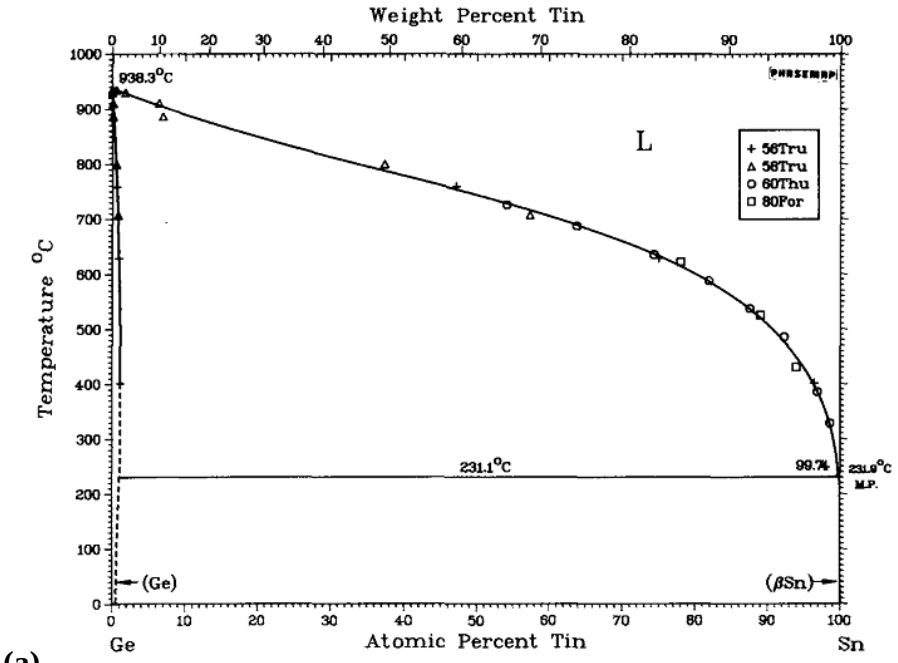
GeSn Material Challenges

This chapter discusses some of the most critical challenges involved in GeSn material growth and processing. A literature review of some of the key approaches adopted for GeSn material growth is presented. Thermal budget constraints in processing GeSn will also be discussed.

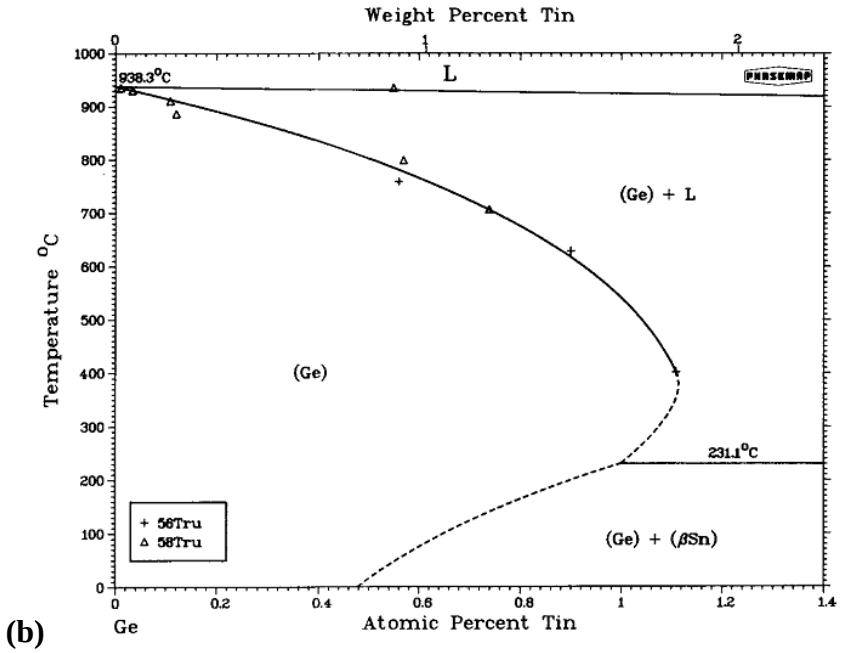
3.1 Solid solubility of Sn in Ge

Some of the earliest investigations into the synthesis of GeSn alloy were performed by Trumbore [**42**,**43**] using conventional crystal pulling techniques and crystal growth from a melt of Ge containing 1 to 5 at. % Sn. Equilibrium distribution coefficients of Sn in Ge at various temperatures and compositions were determined and the coordinates of the liquidus and solidus phase boundaries as a function of temperature T and Sn composition x were estimated. **Figure 3.1** shows the phase diagram of the GeSn alloy system. The diagram contains a eutectic point at a temperature of 231 ºC – close to the melting point of Sn. The maximum equilibrium solid solubility of Sn in Ge is about 1.1 at. % at 400 ºC, and the solubility at the eutectic temperature is possibly less than 1 at. % Sn. In the Sn-doped Ge samples

synthesis using the crystal pulling method, minority carrier lifetimes as high as ~ 100-200 μs were observed, confirming the electrical neutrality of Sn in Ge.



(a)



(b)

Figure 3.1 (From [**44**]) **(a)** The Ge-Sn phase diagram **(b)** Enlarged view of the 0 to 1.4% at Sn% portion of the GeSn phase diagram.

Sn undergoes an allotropic phase transformation at 13.2 ºC. The metallic phase β-Sn, which exists in the body centered tetragonal crystal lattice, is stable at temperature above this value. The semiconducting phase (diamond cubic) α-Sn is stable below this point. From the phase diagram, the problems associated with growth of GeSn are apparent. Equilibrium growth of GeSn results in a two phase solid mixture – diamond cubic Ge with < 1% Sn and β-Sn. Therefore, in order to achieve a supersaturated solid solution of Sn in Ge, material growth needs to be carried out at conditions far from equilibrium. It is essential to choose conditions that minimize precipitation of Sn – both at the surface and in the bulk. Sn surface segregation can be minimized by performing the growth at a temperature low enough to reduce the surface mobility of the Sn atom. Additionally, faster growth can also reduce the formation of Sn clusters on the surface. Phase separation in the bulk happens via nucleation and extension of precipitations, and can be triggered if the metastable alloy is subjected to a high enough thermal process during growth or post-growth processing. In the following sections, aspects of GeSn growth and processing are reviewed in more detail.

3.2 Approaches for GeSn material growth

3.2.1 Physical vapor deposition

As mentioned in the previous chapter, Ge and Sn differ quite significantly in terms of the lattice constant. Sn lattice constant (6.49 Å) is approximately 14% larger than that of Ge (5.658 Å). To grow single-crystal GeSn alloy requires lattice-matched substrates. Since GeSn has the largest lattice constant in the family of group IV bulk

semiconductors (Si and Ge), the only suitable substrates for GeSn growth are certain III-V materials. In 1981, Farrow and co-workers [**45**] reported the first successful attempt at stabilize thin films of α-Sn using closely lattice-matched substrates. Their approach relied the use of molecular beam epitaxy (MBE) to condense a beam of Sn atoms onto clean, (001) oriented InSb (lattice constant 6.479 Å) and CdTe (lattice constant 6.483 Å) substrates held at a temperature of 25 ºC. α-Sn films up to 0.5 μm thick were successfully synthesized and showed no signs of β-Sn precipitates. Interestingly, these films underwent a phase transformation to β-Sn when heated to ~ 75 ºC. After subsequent cooling towards room temperature, only a partial reformation of the original α-Sn was achieved.

This approach of low temperature heteroepitaxy of α-Sn using MBE has been investigated by several researchers and extended to growth of GeSn thin films. **Table 3.1** summarizes the critical growth parameters of some of the reported works focused on MBE growth of single-crystal GeSn alloy. Over the years, a large number of different substrates have been used as a template for GeSn epitaxy – such as Ge, GaAs, GaSb, InSb, CdTe and InGaAs. The growth of GeSn on Si substrates was been made possible through the use of an intermediate layer of strain-relaxed Ge buffer (Ge-on-Si virtual substrate). The amount of Sn incorporated in the GeSn layer is dependent on the substrate. For III-V substrates such as InP, GaSb and CdTe that lattice-match Sn closely, growth of GeSn with large Sn fraction is possible. On the other hand, growth on Si, Ge and GaAs typically allows for only a small level of Sn substitution in Ge. The common feature in all these reports is the use of low

temperature (< 220 ºC) during the GeSn growth step in order to achieve Sn incorporation beyond the solid solubility limit of 1% and to avoid precipitation of Sn into β-Sn. A drawback of the low temperature growth is the high density of point defects in the resulting material. A post-deposition anneal is typically required to annihilate these point defects and improve the material quality[**17**].

Table 3.1 Literature on growth of GeSn using MBE arranged chronologically. Key growth parameters such as alloy composition, growth temperature and substrate are indicated.

Reference	**Year**	**Sn %**	**Growth temperature**	**Substrate**
Shah et al. [**46**]	1987	0 – 20	90 – 150 ºC	Ge (001), GaAs (001)
Asom et al. [**47**]	1989	92 – 100	30 ºC	InSb (001)
Pukite et al. [**48**]	1989	0 – 30	100 – 200 ºC	Ge buffer
Reno and Stephenson [**49**]	1989	100	75 ºC	CdTe (110)
Piao et al. [**50**]	1990	26	200 ºC	InP
		54	190 ºC	GaSb
He and Atwater [**51**]	1995	0 – 34	120 – 200 ºC	Ge buffer
Gurdal et al. [**52**]	1997	0 – 26	100 ºC	Ge (001)
Takeuchi et al. [**53**]	2008	5.8	200 ºC	Ge buffer
Su et al. [**54**]	2011	2.5 – 7.8	100 – 220 ºC	Ge buffer
Kasper et al., [**55**]	2012	0 – 4	85 ºC	Ge buffer
Lin et al. [**56**]	2012	0 – 10.5	200 ºC	InGaAs

Apart from MBE, a few other physical deposition techniques have also been employed for growth of metastable GeSn. A conventional RF sputtering system was used to synthesize crystalline GeSn (up to 14% Sn) on Ge (001) substrates [**57**]. Ge and Sn were co-sputtered on to a Ge substrate heated to 150 – 170 ºC to yield GeSn thin films pseudomorphic to Ge. A more recent study [**58**] investigated the use of solid phase recrystallization of an amorphous GeSn layer to obtain single crystal GeSn containing Sn% as high as 6.1%. Ge and Sn were deposited at room temperature on a Si (111) substrate using thermal evaporation. During the deposition the Si substrate was exposed to a N_2 flux in order to reduce the adatom surface diffusion. The as-deposited films were amorphous, and subsequent rapid thermal anneal in N_2 ambient at 600 ºC for 1 min resulted in formation of single-crystal GeSn as confirmed by the XRD scan of **Figure 3.2**.

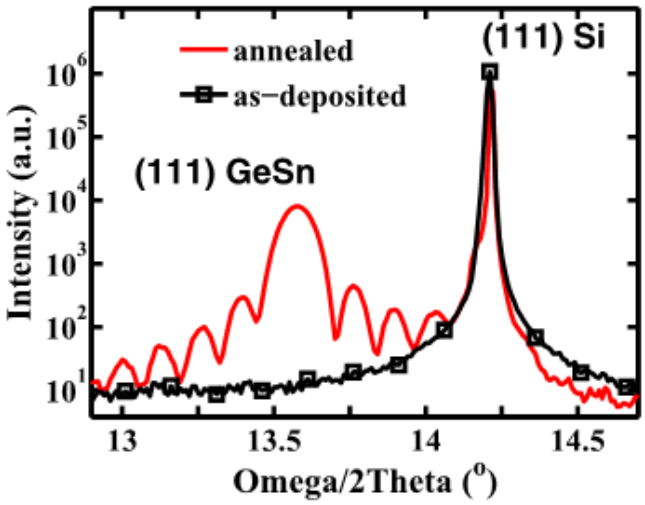


Figure 3.2 (From [**58**]) Comparison of XRD $\omega/2\theta$ scans of as-deposited (amorphous) and annealed (crystalline) GeSn on Si (111).

3.2.2 Chemical vapor deposition

Up until late the late 90's, MBE was the primary technique being developed and used for growth of GeSn. Chemical vapor deposition (CVD) of GeSn remained elusive due to the lack of suitable gaseous precursors for Sn. Unlike the Si and Ge hydrides that are typically used for Si, Ge and SiGe CVD, Sn hydrides are unstable at room temperature due to the significantly lower Sn – H bond energy. Taraci et al. [**59**] at Arizona State University proposed the use of deuterium to stabilize Sn hydrides in order to yield a viable Sn CVD precursor. In one of their earliest demonstration of GeSn growth using CVD [**60**], SnD_4 was used as the precursor for delivery of Sn, while digermane (Ge_2H_6) was used as the precursor for Ge. Depositions were carried out at temperatures in the range of 250 – 350 ºC using an ultra high vacuum CVD tool.

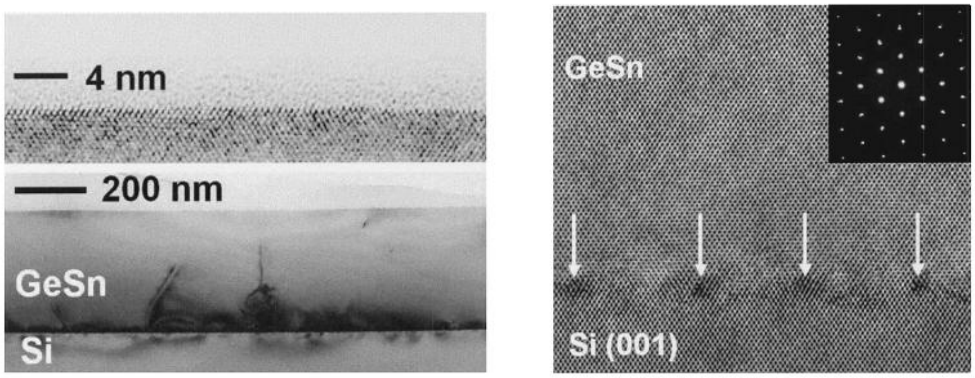


Figure 3.3 (From [**60**]) Cross-sectional TEM of GeSn (6% Sn) grown using UHV-CVD. Left panel shows the top surface of the GeSn layer and the uniformity of the GeSn layer. Right panel shows the GeSn/Si interface region. Arrows indicate the location of misfit dislocations.

More recently [**18**], the Ge_3H_8/SnD_4 combination was shown to yield 3-4 times higher growth rates than the Ge_2H_6/SnD_4 approach. Using Ge_3H_8, relatively thick

layers (> 450 nm) of GeSn containing up to 9% Sn were successfully synthesized at a growth rate of ~ 5 – 10 nm/min. A post deposition, *ex-situ* rapid thermal anneal was performed at a temperature of 650 ºC for 2 – 10s for GeSn with 3 – 4 % Sn, and at a temperature of 550 ºC for GeSn with 9% Sn. This anneal resulted in strain relaxation in the GeSn layer and reduction in the threading dislocation density. Note that GeSn was grown directly on Si and showed only a very slight residual strain. For GeSn with 9% Sn, anneal at temperatures above 575 ºC showed signs of material degradation due to Sn precipitation.

Although the UHV-CVD approach has been shown to result in good quality GeSn with high Sn%, several practical issues may limit its applicability. Firstly, the necessity of ultra high vacuum has never been confirmed experimentally. More importantly, the Sn precursor SnD_4 is highly toxic (NFPA704 health hazard rating 4) and has a very small shelf life as shown in **Figure 3.4**. SnD_4 has a tendency to rapidly dissociate into elemental Sn and deuterium gas at ambient temperatures.

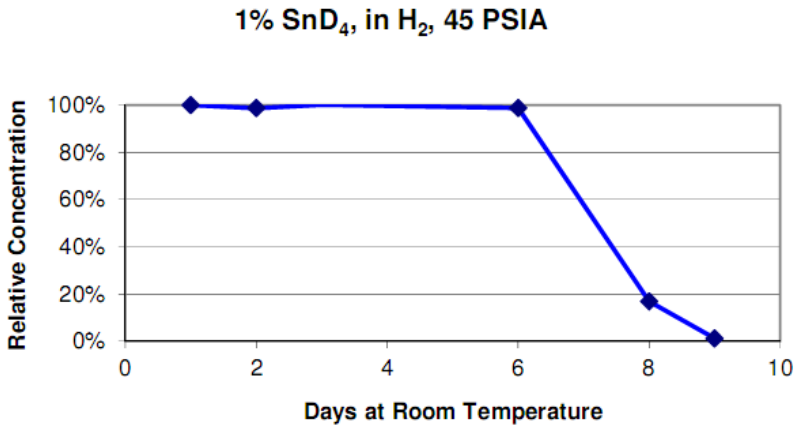


Figure 3.4 (From [**61**]) Stability of 1% SnD_4 in H_2 kept at 300 K in an untreated 1 liter aluminum cylinder.

Nonetheless, the attractiveness of the CVD technique for growth of high quality GeSn has prompted efforts towards developing SnD_4 as a commercially viable Sn precursor. In a recent study [**61**], different coatings on the interior of the SnD_4 storage cylinder were tested to improve the stability of SnD_4. Through the use of an antioxidant (Quercetin) as a coating for the cylinder wall, SnD_4 lifetime as high as 8 months was achieved (see [**61**] for more details).

Alternatively, Vincent et al.[**62**] demonstrated a different CVD growth recipe that overcomes the challenges faced in UHV-CVD using SnD_4. This CVD recipe relied on the use of commercially available tin-tetrachloride ($SnCl_4$) and digermane as precursors. $SnCl_4$ is a liquid at room temperature and it is introduced into the CVD chamber through a H_2 bubbler. Deposition was carried out at atmospheric pressure and at a temperature of 320 ºC. The main advantage of using $SnCl_4$ is the total absence of precursor instability issues. 1 μm thick strain relaxed Ge-on-Si buffer layer was used a template for GeSn epitaxy. A 40 nm thick layer of GeSn with 8% Sn was grown lattice-matched to this Ge buffer. The GeSn growth rate was approximately 30 nm/min. **Figure 3.5** shows the cross-sectional TEM image and the (224) reciprocal space map of GeSn (8% Sn) grown on Ge-on-Si. Since the GeSn layer is grown pseudomorphic to the Ge buffer, there are no misfit dislocations in the GeSn layer as seen in the case of GeSn growth on Si. Also, note that the GeSn layer is fully strained with respect to Ge. This growth technique achieves very high quality, defect-free GeSn with high Sn composition and has been chosen as the preferred platform for fabrication of GeSn-based CMOS devices in the next chapter.

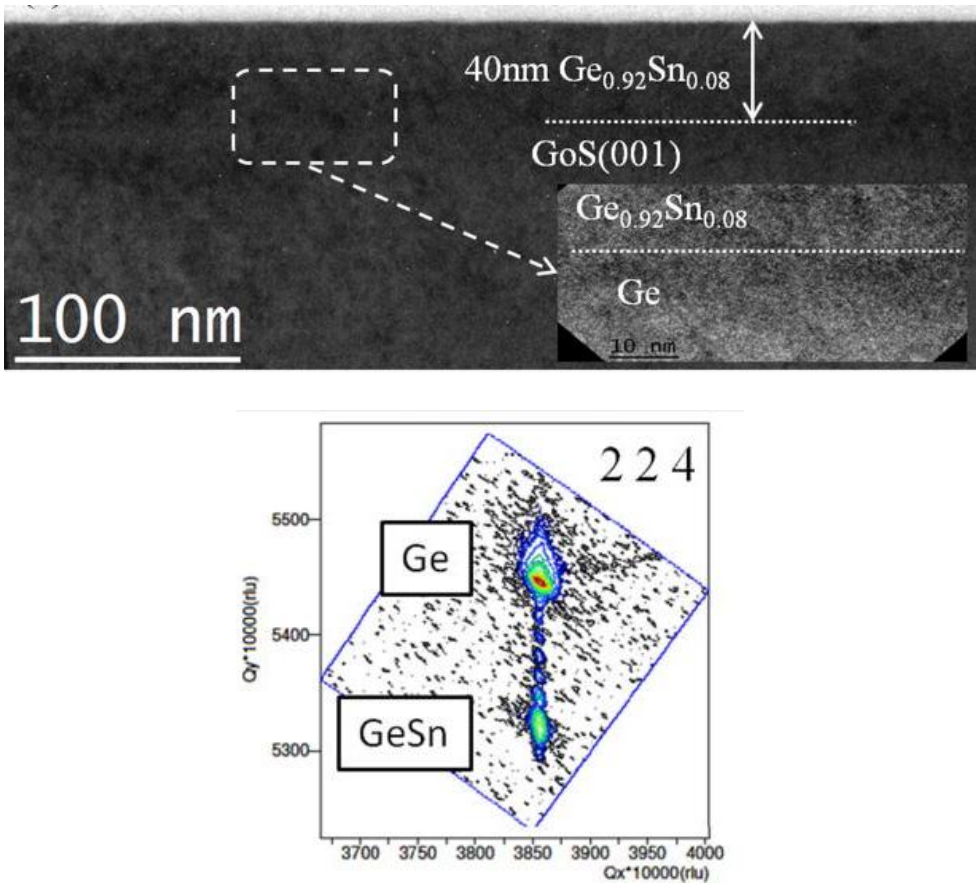


Figure 3.5 (From [**62**]) Cross Section TEM of a 40 nm fully strained defect free GeSn layer on 1 μm Ge/Si buffer substrate with 8% Sn grown with AP-CVD using combination of Ge_2H_6 and $SnCl_4$. (224) XRD-RSM of the 40 nm $Ge_{0.92}Sn_{0.08}$/Ge bi-layer showing that GeSn is fully strained on Ge.

3.3 Thermal budget constraint in GeSn processing

The supersaturated solution of Sn in Ge represents a metastable state which has the tendency to undergo phase separation to form the thermodynamically more stable solid solution of GeSn (<1% Sn) and β-Sn. This phase separation can be triggered if the metastable alloy is subjected to a thermal process that helps overcome the small activation energy barrier ΔE between the metastable and the ground-state (**Figure**

3.6). Naturally, this introduces a thermal budget constraint in processing GeSn alloys. Since only the semiconducting, metastable form of GeSn is of interest here, care must be taken in order to avoid to the precipitation of β-Sn. So far, this chapter has explored different growth methods that have been successfully employed for synthesis of metastable GeSn alloys. The remainder of this chapter discusses the effect of thermal treatment on the properties of GeSn.

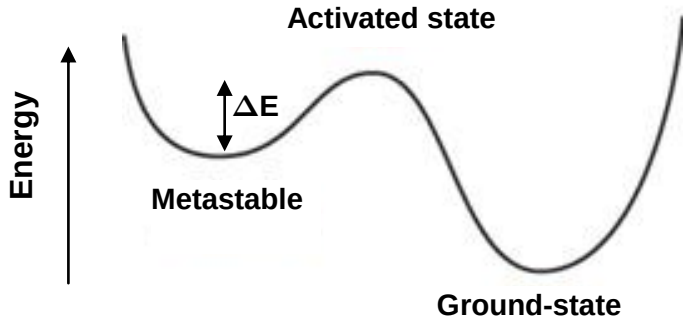


Figure 3.6 Schematic showing the relative stability of the metastable state with respect to the ground-state. The metastable state of the material can change into ground-state if the activation energy barrier ΔE can be overcome.

Takeuchi et al. [**53**] analyzed the effect of a post-deposition thermal anneal (PDA) on GeSn layers grown using low temperature MBE. GeSn layers containing 8% Sn were grown pseudomorphically on a Ge (001) substrate and subjected to PDA at 600 ºC for 10 min. **Figure 3.7** shows the cross-sectional TEM images of the samples before and after the PDA. The as-grown GeSn layers showed no obvious signs of defects or β-Sn. However, after the PDA, several spherical dots were observed close to the Ge/GeSn interface. Through the use of selected area diffraction

(SAD) technique, these spherical dots were identified to be β-Sn precipitates. Interestingly, very few misfit dislocations were observed and the GeSn layer showed very little strain relaxation. From the XRD measurements, the concentration substitutional Sn in the annealed GeSn layer was estimated to reduce to only 2.4%.

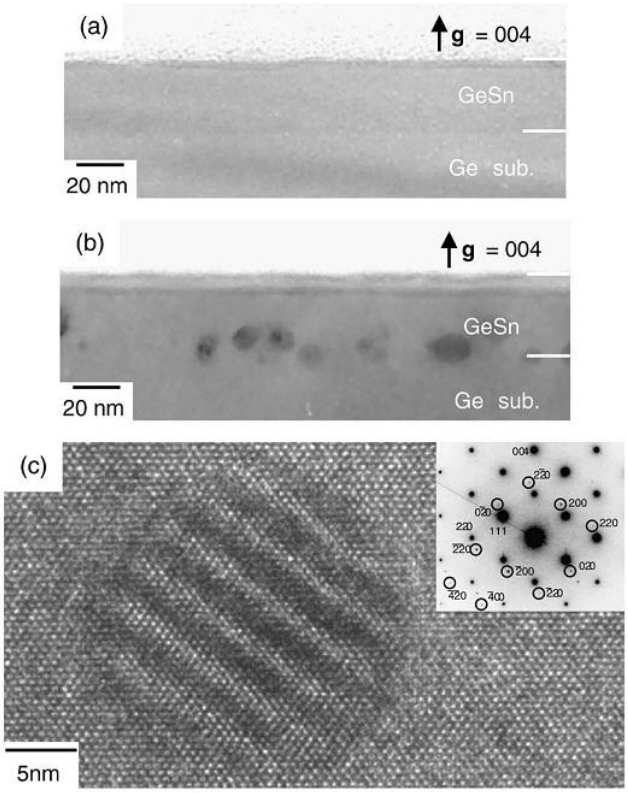


Figure 3.7 (From [**63**]) Cross-sectional TEM images for (a) as-grown and (b)PDA-treated GeSn (8% Sn) layers on Ge.(c) High-resolution TEM image of the spherical dot shown in (b).The inset shows the corresponding selected area diffraction pattern.

Similar experiments were also performed on GeSn grown using CVD with Ge_2H_6 and $SnCl_4$ as precursors [**64**]. GeSn layers investigated contained 10% Sn grown pseudomorphically on a strain-relaxed Ge buffer layer, and subjected to rapid thermal anneal (RTA) at temperatures in the range of 400 – 600 ºC. Surface analysis

techniques such as plan view SEM and Auger electron spectroscopy (AES) were used to determine the change in the GeSn surface morphology and chemistry upon thermal treatment. The surface quality remained similar to the as-grown samples for anneals at 400 ^{o}C for up to 500s and showed no signs of surface Sn. However, annealing treatments at 450 ^{o}C for 60s created surface nanodots with dome shapes on the sample surface. AES surface mapping of the sample annealed at 500 ºC confirms that the surface of the nanodots is Sn-rich.

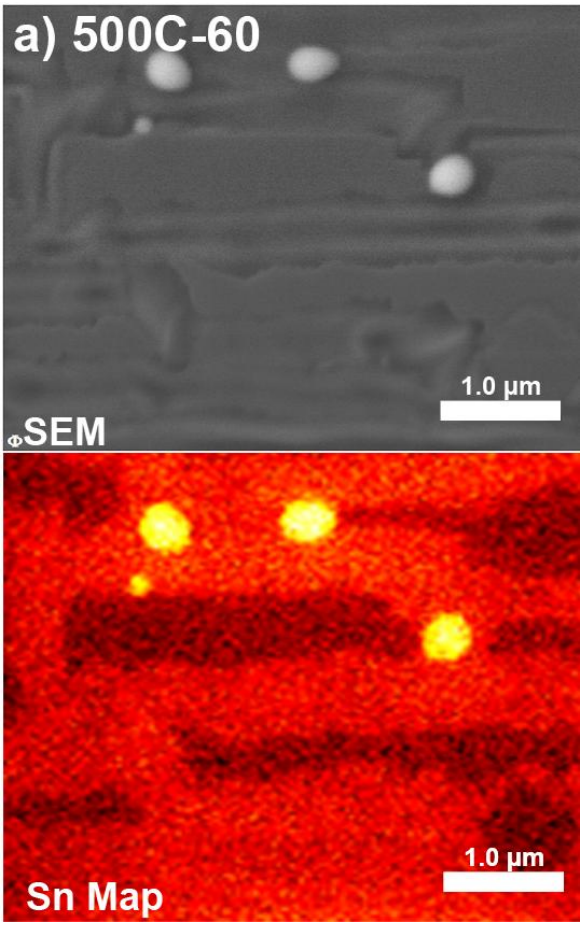


Figure 3.8 (From [**64**]) SEM and Auger surface mapping of Sn for GeSn annealed at 500 ºC for 60s showing the presence of surface Sn.

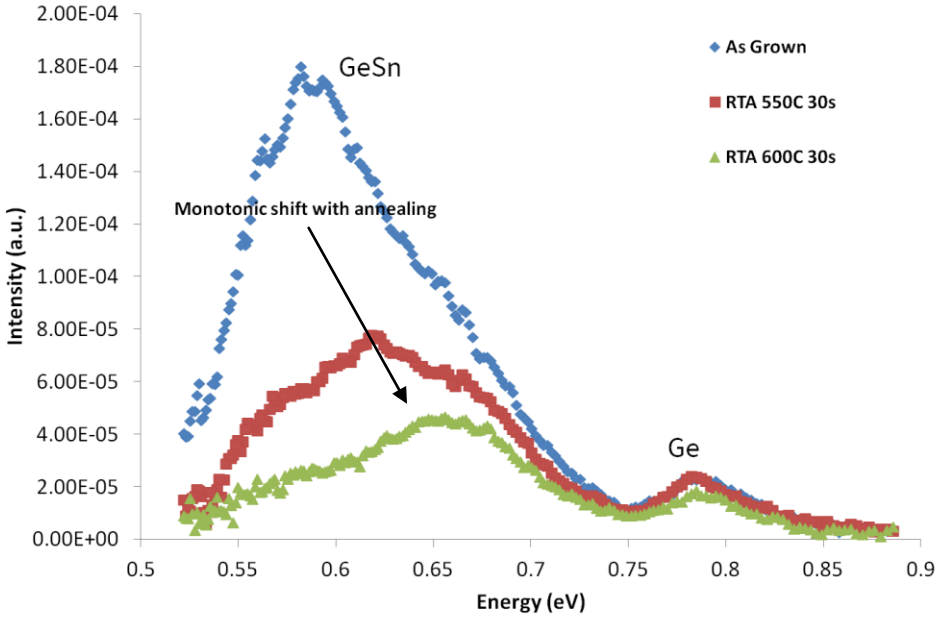


Figure 3.9 PL spectra for GeSn annealed at 550 ºC and 600 ºC for 30 s. The spectrum from the as-grown sample is also shown for comparison. A monotonic shift in the peak PL position with thermal budget is observed.

Other characterization techniques such as photoluminescence (PL) and XRD measurements can also be employed to detect the phase separation in metastable GeSn upon thermal treatment. **Figure 3.9** shows the PL spectra of samples that undergo different anneals. As the thermal budget of the anneal increases, the position of the peak PL due to GeSn shifts to higher energies, suggesting an increase in the band gap. Since the band gap of GeSn increases with a reduction in Sn content, this observation is consistent with the conclusion that excessive thermal budget processing causes a reduction in the amount of Sn present in the substitutional sites. Also, the decrease in the PL intensity in the anneal samples points towards a degradation in material quality due to precipitation of β-Sn.

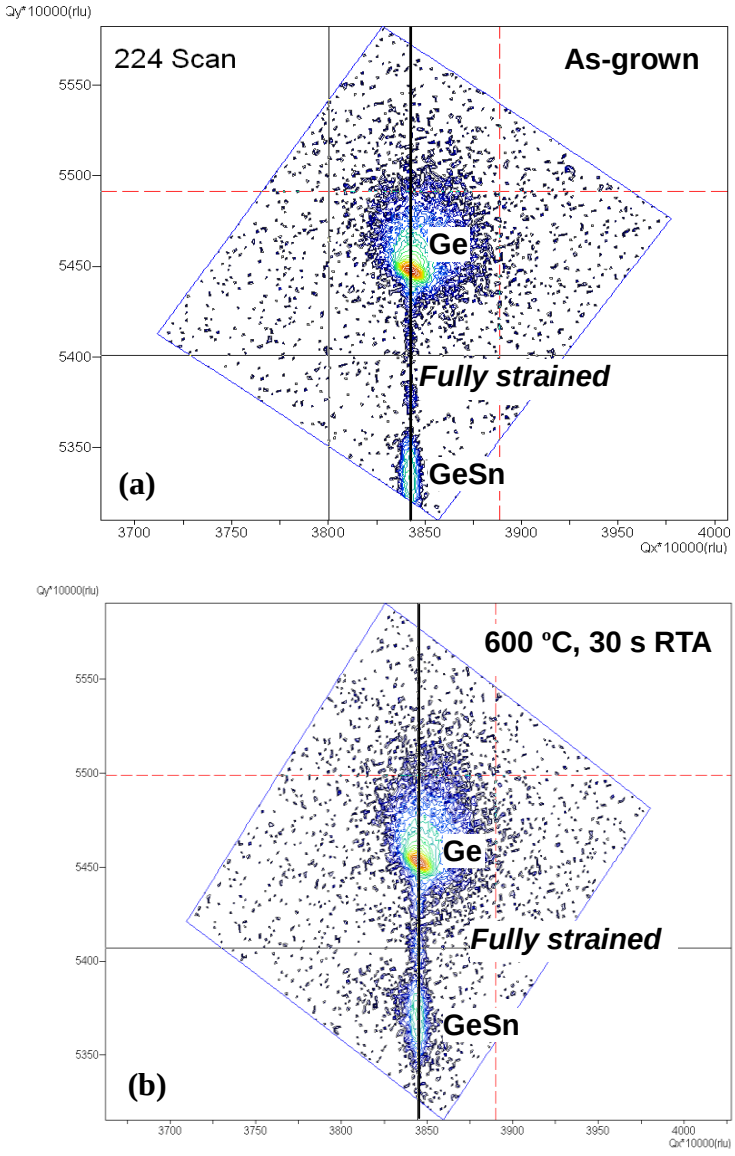


Figure 3.10 224 reciprocal space map of (a) as-grown GeSn and (b) GeSn annealed at 600 ºC for 30 s.

The reduction in the concentration of substitutional Sn is also confirmed through XRD measurements shown in **Figure 3.10**. In the (224) reciprocal space map shown here, the separation between the Ge and GeSn peaks is a direct measure of the amount of Sn occupying substitutional sites in the GeSn matrix. In **Figure 3.10**, the

shift of the GeSn peak closer to the Ge peak upon 600 ºC anneal is due to β-Sn precipitation. When present in substitutional sites, Sn increases the lattice constant of the GeSn layer. However, since the GeSn layer is pseudomorphic (fully-strained) to Ge, the in-plane lattice constant of the GeSn layer is same as that of the Ge buffer. The resulting tetragonal distortion of the GeSn lattice causes an increase in the out-of-plane lattice constant. If Sn moves out of the substitutional sites, the out-of-plane lattice constant of the GeSn layer reduces due to the combined effect of a) reduction in the unstrained lattice constant of GeSn and b) reduction in the degree of tetragonal distortion. Therefore, the GeSn XRD peak moves closer to the Ge peak. Note that even after anneal, GeSn layer stays fully-strained with respect to the Ge buffer.

3.4 Summary

This chapter reviewed the main challenges involved in growth and processing of GeSn. Different approaches for GeSn material growth that successfully achieve Sn substitutional Sn in excess of the solid solubility limit were discussed. These techniques include low temperature MBE, solid phase epitaxy and CVD. Excessive thermal treatment of GeSn was found to result in surface and bulk precipitation of β-Sn. The precise upper limit on the allowable thermal budget before the onset of Sn precipitation depends on the concentration of Sn in GeSn. GeSn containing as high as 10% Sn was found to withstand anneals at 400 ºC for up to 500 s. As the Sn% increases, this upper limit is expected to reduce. In the next chapter, the understanding of the GeSn material system established here is used to develop low thermal budget processes for fabrication of GeSn channel n and p MOSFETs.

Chapter 4

GeSn CMOS Technology

This chapter undertakes the task of developing essential elements of a GeSn-based CMOS technology. Topics of discussion include GeSn surface preparation, gate stack and source/drain formation for n-channel and p-channel MOSFETs. Special focus is given to the high-k/GeSn interface engineering for reducing the interface trap density and to avoid degradation in device performance.

4.1 GeSn channel pMOSFETs

The first generation of pMOSFET devices were fabricated on GeSn grown using MBE. However, CVD-grown GeSn was chosen as the preferred platform for the second generation of devices. This migration was largely motivated by the lack of adequate material supply from MBE and the need to develop the device technology compatible with large-area wafer processing. As opposed to MBE that relies on small (2” or 3” diameter wafers) Ge or GaAs substrate for GeSn epitaxy, CVD growth process is compatible with industry standard 8” or 12” Si wafers.

4.1.1 MBE-GeSn

The first step towards realizing MOSFET devices is to achieve good quality interface between the substrate and the high-κ dielectric. Atomic layer deposition

(ALD) is the most widely adopted method for forming thin layers of high-κ dielectrics such as Al_2O_3, HfO_2 etc. on the semiconducting substrate. Semiconductor surface treatment in order to remove the native oxide and other possible contaminants that may inhibit the ALD precursor nucleation or otherwise degrade the quality of the high-k/semiconductor interface is a critical step in the ALD process. Remainder of this section investigates the effect of different pre-ALD wet-chemical GeSn surface treatment methods on Al_2O_3/GeSn interface quality. Subsequently, the optimal surface preparation method is incorporated into a low thermal budget process flow for fabrication of GeSn pMOSFETs.

GeSn surface preparation

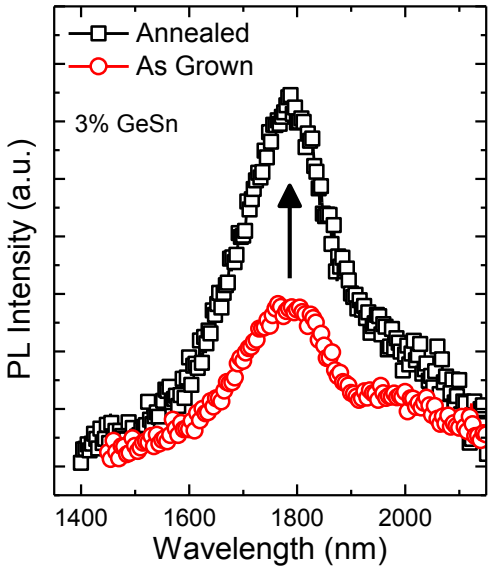


Figure 4.1 Effect of post-MBE RTA on the PL spectra of GeSn (3% Sn). Increase in direct gap PL intensity suggests improvement in material quality**.**

300 nm thick GeSn with 3% Sn is grown using low-temperature MBE on semi-insulating (100) GaAs wafer with an intermediate strain-relaxed buffer layer of

InGaAs for accommodating the lattice-mismatch between GeSn and GaAs. Due to the Arsenic contamination in the MBE chamber used generally for growth of III-V Arsenides, the GeSn layer is unavoidably doped n-type to approximately 7e17/cm^2. Post-MBE, rapid thermal anneal (RTA) at 600 ºC for 30 s is carried out to annihilate bulk point defects due to the low temperature MBE growth. **Figure 4.1** compares the photoluminescence (PL) spectra of the GeSn samples before and after the RTA. The increase in direct band PL intensity confirms the overall improvement in the GeSn material quality due to 600 ºC thermal anneal. Also, the lack of any noticeable shift in the peak PL position suggests that the RTA thermal budget does not result in any significant Sn precipitation.

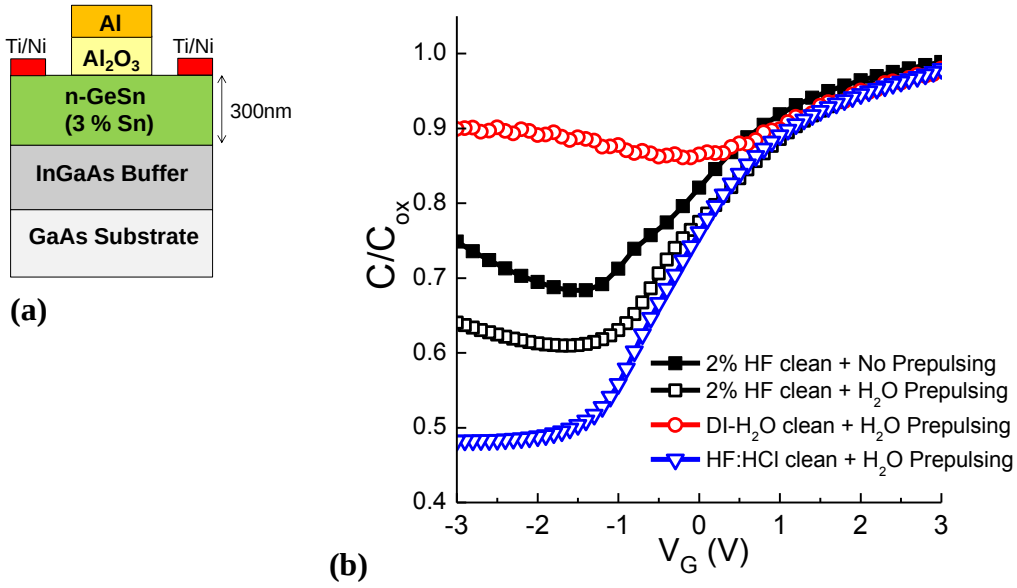


Figure 4.2 (a) Schematic of the MOS capacitors. **(b)** High frequency CV characteristics of Al/Al_2O_3/n-GeSn MOS capacitors for different pre-ALD surface treatments. Combination of 1:1 HF:HCl clean and H_2O prepulsing shows the best CV response in terms of C_{ox}/C_{min} ratio and stretch-out in depletion.

Prior to ALD Al_2O_3 deposition on these GeSn layers, different wet surface cleans are performed: (**A**) De-Ionized (DI) H_2O rinse, (**B**) 2% HF and (**C**) 1:1 HF: HCl. After wet cleaning, the samples are blown dry using high purity N_2 and immediately loaded into the ALD load-lock to minimize surface oxidation due to ambient O_2. In the main chamber of the ALD deposition system, the samples are subjected to 50 cycles of pre-Al_2O_3 deposition oxidant pulsing at 250ºC using DI-H_2O. 12nm Al_2O_3 is then deposited at 250ºC using alternate pulses of Trimethyl Aluminum (TMA) and DI-H_2O. Gate metal for the MOS capacitor is formed by sputter deposition of 150 nm Al followed by metal patterning using contact lithography. The MOS capacitors are annealed in forming gas environment (4% H_2/96% N_2) at 350ºC for 30 minutes.

Figure 4.2 shows the measured room temperature high frequency (1 MHz) response of the MOS capacitors fabricated with different surface cleaning prior to Al_2O_3 deposition. Capacitors with clean **A** (DI-H_2O rinse only) show a nearly flat high frequency capacitance-voltage (CV) response indicating the presence of very high interface state density (D_{it}). Surface cleaning with 2% HF (clean **B**) improves the inversion response with a higher C_{ox}/C_{min} ratio, suggesting improved efficiency of Fermi-level movement across the bandgap as compared with the sample treated with clean **A** only. Nonetheless, the finite slope of the high frequency curve in the strong inversion regime (large negative bias) and the failure to reach the minimum capacitance as determined by background doping, indicate pinning of the Fermi-level due to midgap D_{it} [**65**]. **Figure 4.2** also shows the effect of oxidant prepulsing on the high frequency CV response for the samples pretreated with 2% HF prior to Al_2O_3

deposition. Samples undergoing oxidant prepulsing show a higher C_{ox}/C_{min} ratio, steeper slope in depletion and weaker D_{it} response in strong inversion, indicating improved interface quality. This observation is consistent with the results of ALD Al_2O_3 deposition on Ge reported in [**66**]. Lastly, samples treated with clean **C** – a mixture of 1:1 49% HF and 36% HCl shows the best CV response in terms of C_{ox}/C_{min} ratio and stretch out in depletion.

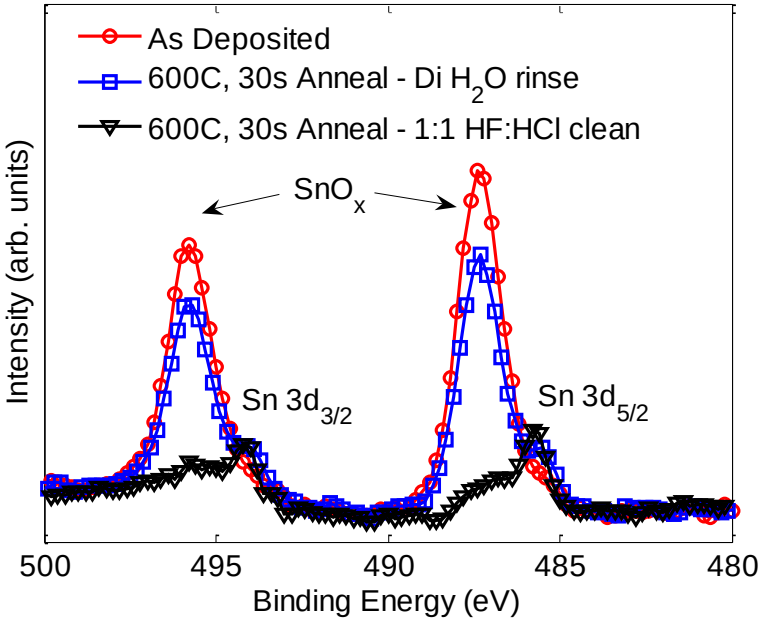


Figure 4.3 XPS spectra showing Sn3d peaks and effect of 1:1 HF:HCl clean. SnO_x concentration on surface is reduced after 1:1 HF:HCl clean and Sn3d peaks from GeSn layer are visible.

Surface analysis using X-ray photoemission spectroscopy (XPS) helps understand the change in the surface properties of GeSn after 1:1 HF: HCl clean. **Figure 4.3** shows the Sn 3d spectra for as-grown sample, sample annealed at 600 ºC with no surface treatment, and sample annealed at 600 ºC followed by clean with 1:1

HF: HCl solution. The as-grown sample and the annealed sample with no chemical treatment show a high surface Sn concentration. The shift in the Sn $3d_{5/2}$ peak in these samples towards higher binding energy from 485.6 eV to 487.4 eV indicates that the surface Sn is present mainly in its higher oxidation states – in form of SnO_x. After HF: HCl clean, the concentration of surface Sn reduces drastically and Sn 3d peaks corresponding to metallic Sn are visible.

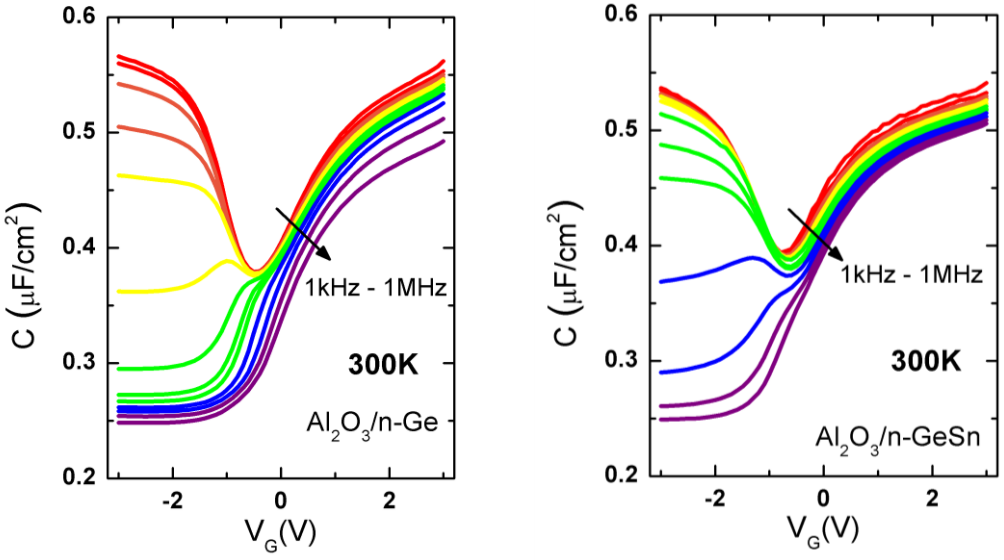


Figure 4.4 CV characteristics for Ge and GeSn (3% Sn) MOS capacitors. 12 nm Al_2O_3 is used as the gate oxide.

Figure 4.4 shows the multi-frequency CV response at 300 K on capacitors formed on Ge control sample and 3% GeSn using the optimal surface preparation technique (clean **C**) and DI-H_2O pre-pulsing. MOS capacitors on both Ge and GeSn (3% Sn) show similar characteristics in terms of CV characteristics. The stronger inversion response for GeSn MOS capacitors can be attributed to the smaller band gap of GeSn as compared with Ge. The capacitors show gate leakage of less than 10^{-6}

A/cm^2, indicating that the gate stack formation method adopted here does not result in any Sn diffusion into the gate oxide.

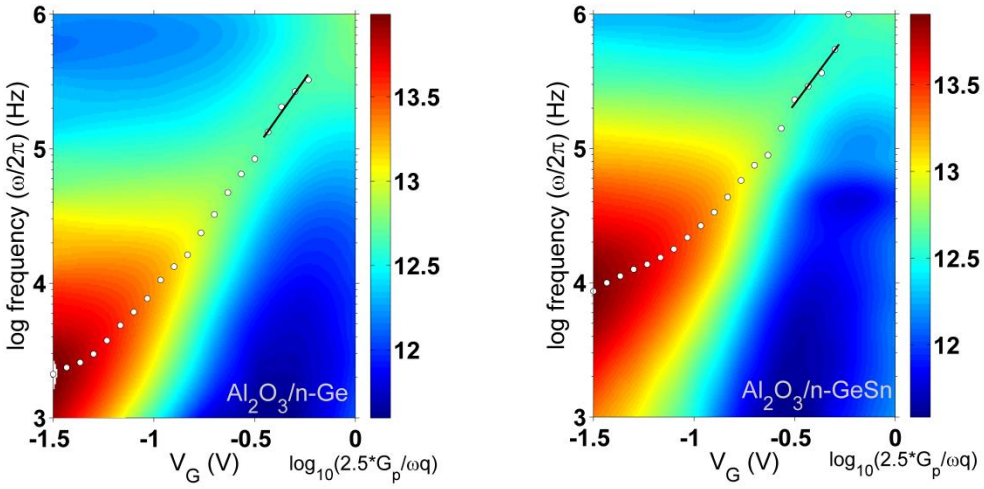


Figure 4.5 Parallel conductance (G_p/ω) as a function of measurement frequency and applied gate bias V_G for Ge and GeSn (3% Sn) MOS capacitors. The trace of the peak G_p/ω is shown as the solid line.

The Fermi-level efficiency (FLE) method [**67**] is used for further comparison of the electrical characteristics of Al_2O_3/Ge and Al_2O_3/GeSn interfaces. FLE method originates from the well-known conductance method [**68**] conventionally adopted for quantification of the trap density at the oxide/semiconductor interface. In the conductance method applied on a MOS capacitor, the frequency plot of parallel conductance (G_p) divided by measurement frequency (ω) shows a peak corresponding to the frequency that maximizes the interaction between the interface trap level and the majority carrier band. This exchange of carriers between the trap states and the majority carrier band is maximized when the surface Fermi-level is aligned with the energy level of the trap state within the band gap. Hence the frequency f of peak G_p/ω

at a given applied gate bias can be expressed in terms of the energy separation of the Fermi-level from the majority band (ΔE)

$$f = \frac{\exp\left(\Delta E / \kappa T\right)}{\sigma v_t N}, \tag{4.1}$$

where σ is the trap capture cross-section, v_t is the carrier thermal velocity, and N is the density of states in the majority carrier band. The change of the Fermi-level position with the change in applied bias is a measure of the D_{it} at interface. For a surface with very high D_{it}, the Fermi-level shows negligible change with the applied bias. FLE defined as the derivative of the surface Fermi-level position with respect to the applied gate bias V_G can be used to gauge the effectiveness of the surface passivation scheme.

$$FLE = \frac{dE_f\left(V_G\right)}{dV_G} \cong \frac{\Delta E_1 - \Delta E_2}{q\left(V_1 - V_2\right)} = \ln\left(\frac{f_2}{f_1}\right)\frac{\kappa T}{q\left(V_1 - V_2\right)} \quad (\%) \tag{4.2}$$

FLE can be estimated from the slope of the trace of peak G_p/ω plotted as a function of applied bias and frequency (**Figure 4.5**). At a measurement temperature of 300 K, traps near the middle of the band gap (mid-gap states) have characteristic frequency f in the measurable range of 1kHz - 1MHz. FLE in the mid-gap is ~20% for both Ge and GeSn implying that surface properties are not aggravated by alloying Ge with Sn. The change in the slope of the conductance peak trace at higher negative bias suggests that weak inversion response dominates the measured conductance at room temperature [**69**]. This effect is stronger for GeSn due to its smaller bandgap. From the conductance peak at V_G of -0.3V, D_{it} close to the midgap was extracted to be

~2e12/cm^2 for both the samples and possibly overestimated due to weak inversion response.

Low thermal budget pMOSFET fabrication

A 150 nm thick layer of GeSn with 3% Sn is grown using MBE in a manner similar to described earlier. However, for the purpose of fabrication of pMOSFETs, Ge is chosen as the substrate for GeSn epitaxy. Due to the larger lattice constant of GeSn as compared with Ge, epitaxial layers of GeSn grown on Ge are compressively strained. This is confirmed by the (224) reciprocal space mapping of the 150 nm thick GeSn grown on Ge substrate, annealed at 600 ºC for 30 s (**Figure 4.6**). The biaxial compressive strain in the GeSn layer is estimated to be 0.42%.

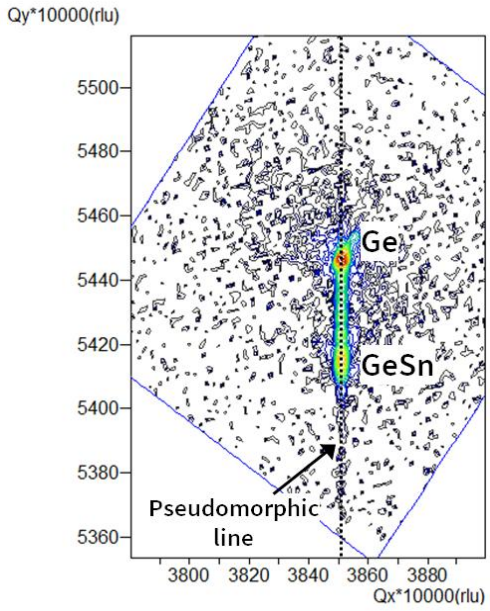


Figure 4.6 (224) reciprocal space map of GeSn (3% Sn) grown on Ge and annealed at 600 ºC for 30 s.

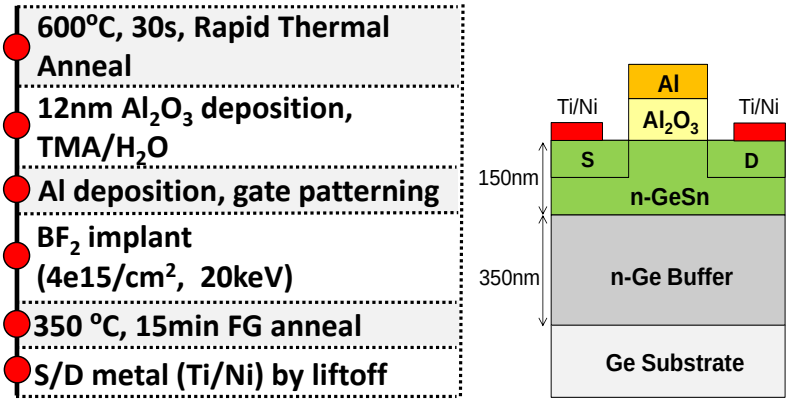


Figure 4.7 Process flow for fabrication of self-aligned Ge, GeSn pMOSFET

The surface passivation scheme described above is used for fabrication of Ge and GeSn surface channel pMOSFETs using the process flow outlined in **Figure 4.7**. After gate-stack formation, source/drain regions are formed by ion-implantation of BF_2 with a dose of 4e15/cm^2 at energy of 20 keV. A 350 ºC, 15 min furnace anneal in forming gas (4% H_2/96% N_2) ambient anneals out the implant damage and activates the dopants in the source and drain. Control pMOSFETs are also fabricated on bulk n-Ge (N_D=1e16/cm2) using the same process flow.

Figure 4.8 shows the I_DV_G characteristics of pMOSFET fabricated on GeSn (3% Sn). The devices show a subthreshold slope of 250mV/dec and I_{ON}/I_{OFF} ratio of ~ 10^3. Gate leakage current (I_G) is negligible in the entire range of device operation. GeSn pMOSFETs show an improvement in the drain current over Ge as shown in **Figure 4.8b**. Effective hole mobility (μ_{eff}) as a function of inversion sheet charge density (N_{inv}) is extracted using the split-CV method for GeSn and Ge pMOSFETs. As shown in **Figure 4.9** GeSn channel pMOSFETs show approximately 20% increase in hole mobility when compared with control Ge pMOSFETs. This improvement in hole

mobility is attributed to the biaxial compressive strain present in the GeSn layers due to epitaxial growth on Ge.

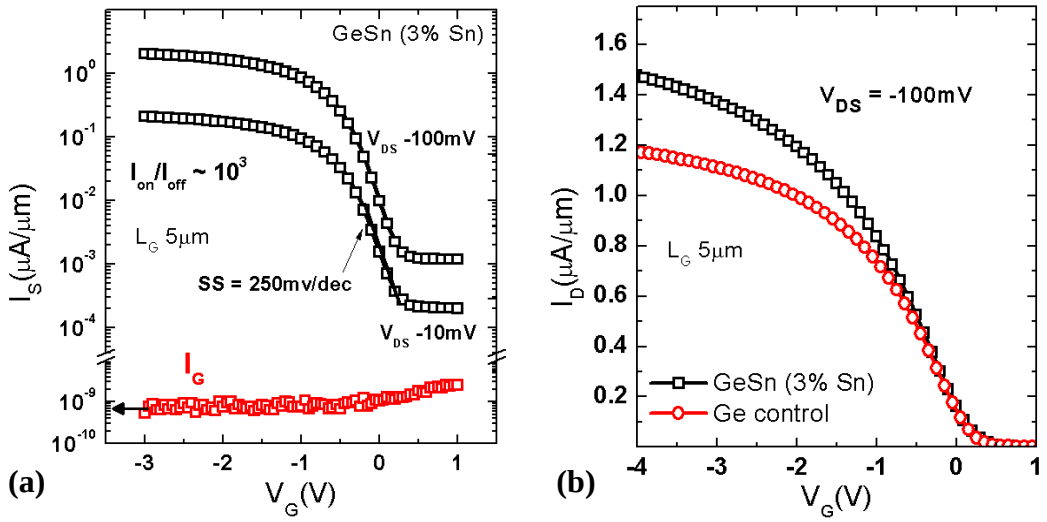


Figure 4.8 (a) I_S-V_G characteristics of GeSn (3% Sn) pMOSFETs. **(b)** Comparison of drain current of GeSn (3% Sn) and control Ge pMOSFETs.

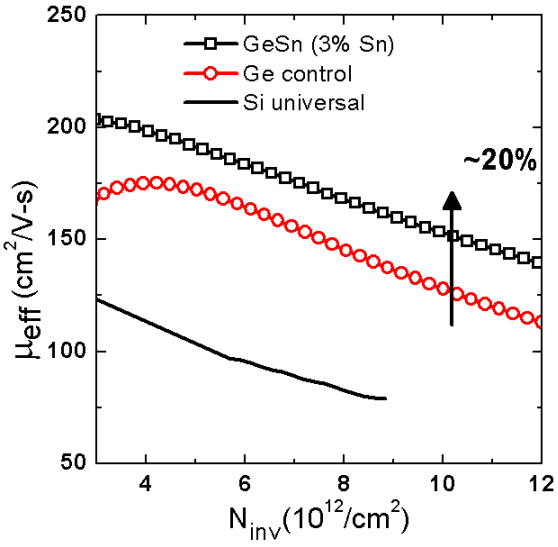


Figure 4.9 Effective hole mobility as a function of channel inversion charge for Ge and 3% GeSn pMOSFETs as extracted by split-CV method.

4.1.2 CVD-GeSn

Sample preparation

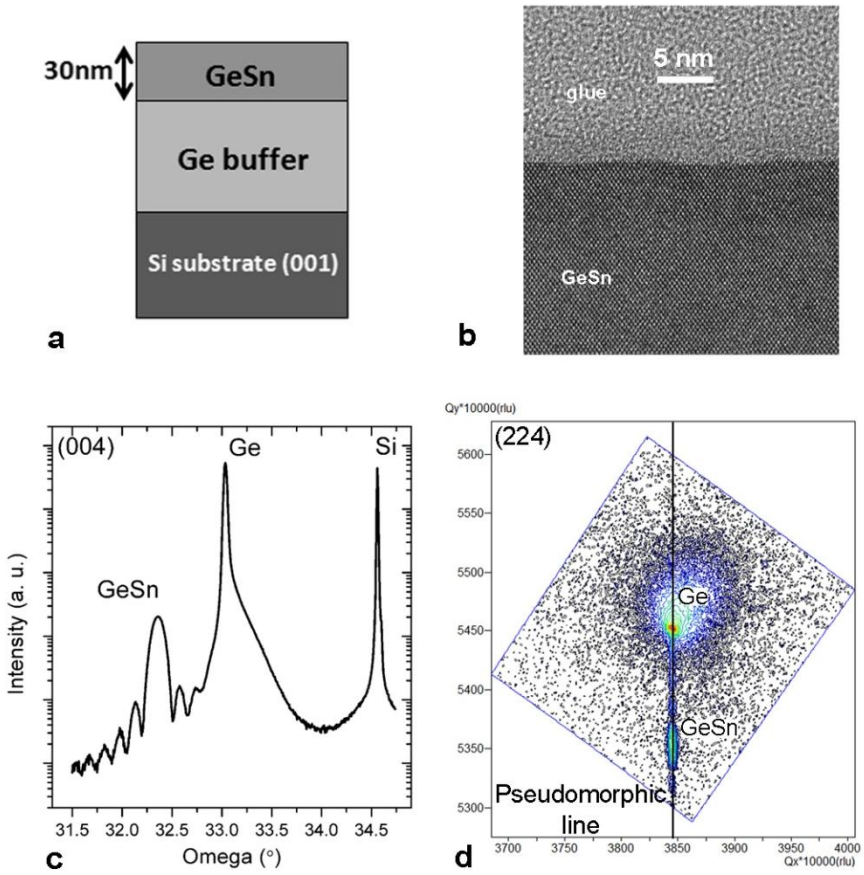


Figure 4.10 (a) Schematic of the material stack used for pMOSFET fabrication **(b)** High resolution TEM image of the top GeSn layer **(c)** (004) HRXRD scan for extracting out-of-plane lattice constant and strain in Ge and GeSn layers. The Sn content in the GeSn layer is 7% **(d)** (224) RSM showing GeSn fully strained with respect to Ge buffer.

A 30 nm thick GeSn (7% Sn) is grown epitaxially on strain relaxed Ge-on-Si (001) buffer layers using the CVD technique described in section 3.2.2. Digermane (Ge_2H_6) and tin tetrachloride ($SnCl_4$) are used as CVD precursors. The growth

temperature during GeSn CVD is kept below 350 ºC. The Ge buffer layer thickness is ~3.7 μm. Schematic of the material stack used for fabrication of GeSn pMOSFETs shown in **Figure 4.10a**. The GeSn growth method adopted produces high quality crystalline GeSn as confirmed by the cross sectional TEM image of **Figure 4.10b**. From (004) high resolution x-ray diffraction (HRXRD) omega-2theta scan of **Figure 4.10c**, the out of plane lattice constant of Ge and GeSn layers is determined to be 5.652Å and 5.759Å respectively. As reported previously [**70**], CVD grown Ge on Si is slightly tensile strained due to the thermal mismatch between Ge and Si. The residual strain in Ge buffer layer is biaxial tensile and estimated to be 0.139%.

Due to its larger lattice constant than Ge thin epitaxial layers of GeSn are fully compressively strained with respect to the Ge buffer layer. This is confirmed by the (224) asymmetric 2D reciprocal space map (RSM) shown in **Figure 4.10d**. Both Ge and GeSn peaks lie along the same in plane reciprocal lattice vector indicating that GeSn is fully strained with respect to the underlying Ge buffer. The biaxial compressive strain in the GeSn layer is calculated to be 1.02% with respect to fully relaxed GeSn (7% Sn). Ge buffer on Si (without the GeSn layer) forms the control sample (Ge control).

As-grown CVD Ge and GeSn samples are slightly p-type with the carrier density of the order of $10^{16}/cm^3$. Therefore, the pMOSFET fabrication begins with n-well formation. Two-step phosphorus implant is used for forming the n-well: 1) $2.5e12/cm^2$ dose at 150 keV followed by 2) $1.5e12/cm^2$ dose at 60 keV. The n-well implant is activated through a thermal anneal at 400 ºC for 5 minutes. Gate-first

process flow is adopted for ring type pMOSFET fabrication. 6nm Al_2O_3 is used as the gate oxide and deposited using atomic layer deposition (ALD) at 350 ºC with trimethyl aluminum (TMA) and ozone (O_3) as precursors. Prior to Al2O3 deposition, the samples are treated with dilute HCl (1:1 solution by volume of 38% HCl and DI-H_2O). As shown in the Ge3d and Sn 4d PES spectra of **Figure 4.11**, dilute HCl clean is effective in removing the native SnO_x from the surface of CVD-grown GeSn. TiN/W is used as gate metal and patterned using dry etching. Source/drain regions are formed using a BF_2 (49) ion implant at 20 keV energy and activated at 400 ºC anneal for 5 minutes. Ti/Ni is used for contacting the source/drain. As shown in the previous chapter, the thermal budget used in this process flow does not result any strain relaxation in GeSn.

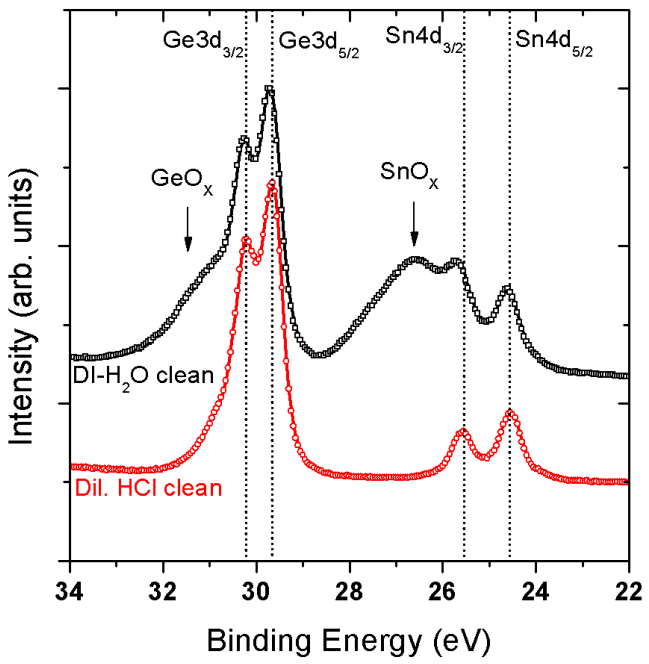


Figure 4.11 PES spectra showing Ge3d and Sn4d peaks. Dilute HCl clean is effective in removing the native SnO_x from the surface.

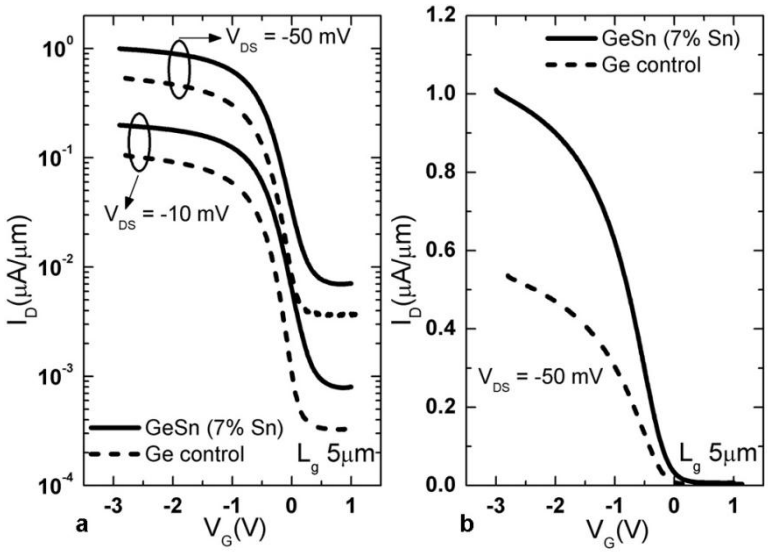


Figure 4.12 Comparison of I_D-V_G characteristics of pMOSFETs on GeSn (7% Sn) and Ge with I_D on **(a)** log scale **(b)** linear scale. GeSn pMOSFETs show nearly 2X gain in drive current.

The I_D-V_G characteristics of surface channel pMOSFETs on GeSn and control Ge are shown in Fig. 2. Both set of devices show similar characteristics in terms of MOSFET I_{ON}/I_{OFF} ratio at 300K and subthreshold swing. Drain-body diode leakage limits the off current of these devices. GeSn shows smaller band gap than Ge and hence the higher off current for GeSn channel pMOSFETs. Nonetheless GeSn pMOSFETs show nearly 2X enhancement in drive current over the control Ge devices as shown in **Figure 4.12b**

Next, the effectiveness of TMA/O_3 ALD process in passivating the Ge, GeSn surface is investigated. The temperature-dependent full conductance method [**69**] on pMOSFETs is used in order to estimate the interface trap density (D_{it}) within the band gap. **Figure 4.13a** plots the parallel conductance (G_p/ω) measured at 77K as a function

of applied bias and measurement frequency. The conductance peaks indicated in **Figure 4.13a** correspond to the interface trap response from which the trap density can be estimated. The interface trap density thus mapped out in the lower half of the band gap for Ge. Both Ge and GeSn device show similar trap distribution with near valence band D_{it} in the 1e12/cm^2 regime.

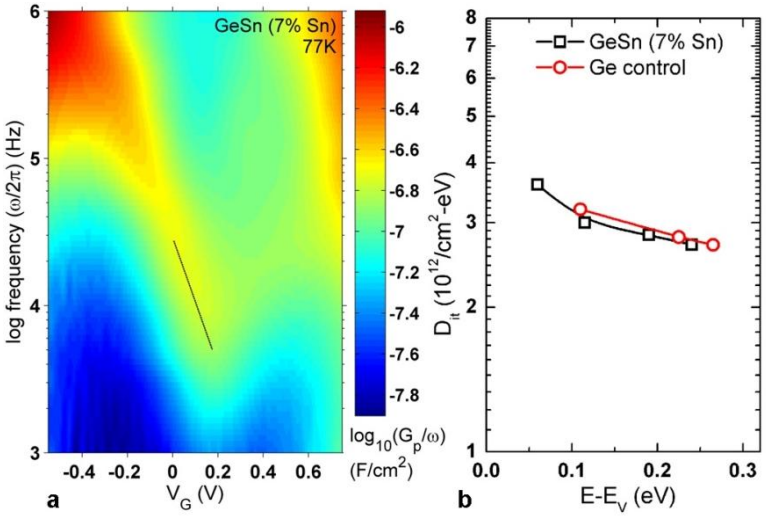


Figure 4.13 (a) Parallel conductance (G_p/ω) measured on GeSn pMOSFETs at 77K. Solid line corresponds to the trace of peak G_p/ω from which D_{it} as a function of trap energy in the band gap can be estimated **(b)** D_{it} in the bottom half of the band gap for Ge and GeSn pMOSFETs as extracted from temperature-dependent conductance measurements.

Inversion channel hole mobility in pMOSFETs is extracted using the split CV technique on long channel devices. **Figure 4.14a** compares the extracted hole mobility in GeSn and Ge control devices. An enhancement of 85% in hole mobility at high inversion sheet charge density is observed for GeSn channel pMOSFETs as compared with Ge control. As similar interface properties are achieved for both Ge and GeSn

channel devices, the observed hole mobility enhancement can be attributed to the presence of compressively strained GeSn as the channel material. As shown in **Figure 4.14b**, the effective hole mobility in GeSn pMOSFETs increases as temperature decreases indicating that inversion channel mobility is limited by phonon scattering. Further improvement in both Ge and GeSn pMOSFET mobility can be achieved by employing passivation schemes that achieve lower D_{it} – such as thin Si passivation on Ge and GeSn [**71**],[**72**] or use of $GeO_x/GeSnO_x$ as the interfacial passivation layer (described in section 4.2).

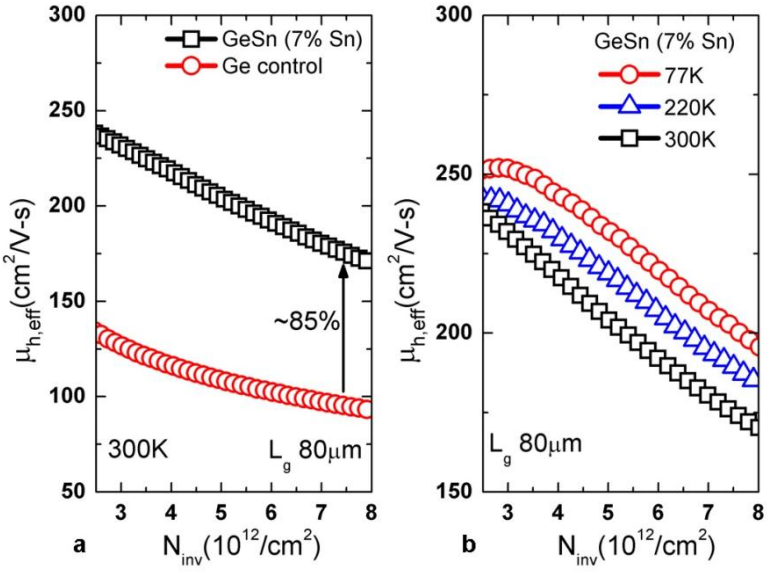


Figure 4.14 (a) Comparison of effective hole mobility at 300K in GeSn (7% Sn) and Ge control pMOSFETs. **(b)** Temperature dependent effective hole mobility in GeSn pMOSFETs.

Mobility enhancement in strained Ge [**9**], [**73**],[**74**] can be attributed to the fact that compressive stress breaks the degeneracy of light hole (LH) and heavy hole (HH) bands and reduces both the density of states and conductivity effective masses. With

the exception of slight reduction in hole effective masses upon Sn incorporation, the overall valence band electronic structure of GeSn remains similar to that of Ge. An increase in alloy Sn composition in GeSn layers grown pseudomorphically on Ge is accompanied by a proportionate increase in the channel compressive strain, thereby boosting GeSn hole mobility by the mechanism similar to that in strained Ge. At the same time, however, additional mobility degradation due to alloy scattering in GeSn may potentially offset hole mobility improvement due to compressive strain.

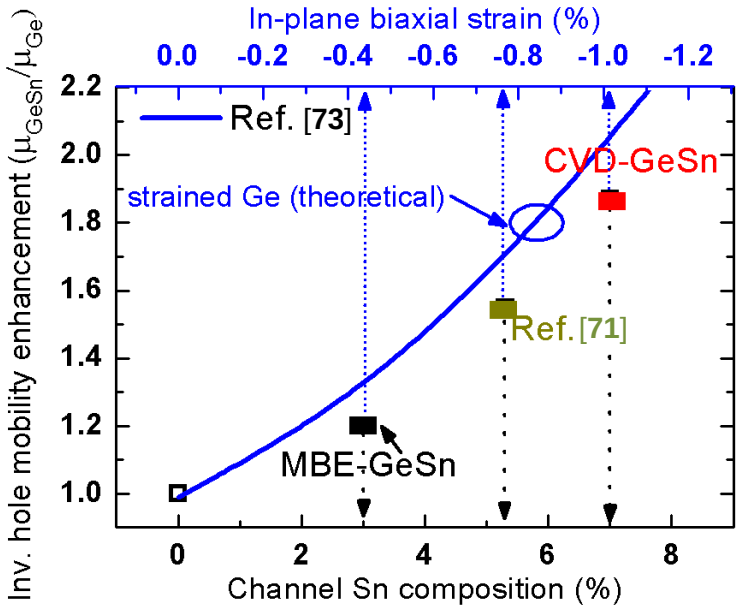


Figure 4.15 Calculated hole mobility enhancement in strained Ge over relaxed Ge as a function of in-plane biaxial strain (line) [**73**]. Also shown are experimental results (symbols) for hole mobility enhancement in strained GeSn pMOSFETs over Ge as obtained for MBE-GeSn, CVD-GeSn and in [**71**].

Figure 4.15 plots the comparison of measured hole mobility enhancement in GeSn pMOSFETs and theoretical calculations of hole mobility gain in strained Ge

[**73**]. Inversion channel hole mobility in GeSn increases with increasing Sn (and hence increasing compressive strain) and closely follows the expected hole mobility enhancement in strained Ge. It can thus be concluded that alloy scattering is not the dominant scattering mechanism in strained GeSn inversion layers for Sn% as high as 7%.

4.2 GeSn channel nMOSFETs

GeSn grown using CVD on Ge buffer layer is used as a platform for fabrication of n-channel MOSFETs. From the simulations results of Chapter 2, it is clear that growth on Ge induces a compressive strain in GeSn and offsets any potential advantages of using GeSn over Ge in terms of gain in electron mobility. Nevertheless, such a material platform can be used for developing other equally critical elements of GeSn nMOSFET technology such as surface passivation and S/D formation.

The first generation of nMOSFET devices were fabricated using a gate-last process flow. These devices helped identify some of the important challenges involved in realization of n-channel devices using GeSn as the channel material. Subsequently, an ozone oxidation method was developed to engineer the GeSn/high-κ interface and significantly reduce the density of interface traps near the conduction band. This novel interface formation method allowed for migration to a simpler gate-first fabrication process for the second generation of GeSn nMOSFETs.

4.2.1 Gate-last process

A 40 nm GeSn layer with 6% Sn is grown epitaxially on Ge using atmospheric pressure chemical vapor deposition (AP-CVD). nMOSFETs are fabricated using the

gate last process flow outlined in **Figure 4.16.** In the gate-last process flow, the gate-stack is formed after source/drain implantation and anneal. This is done in order to minimize any possible damage to the gate-stack during the source/drain anneal step. Source/drain junctions are formed by implanting $10^{15}/cm^2$ of phosphorus (P) at energy of 25 keV followed by a thermal anneal at 400 ºC for 30 min for dopant activation. 8 nm of ALD Al_2O_3 using TMA/O_3 forms the gate oxide. Two sets of samples are prepared: (a) **D08**: No capping layer on GeSn (b) **D09**: GeSn layer is capped with 5nm Ge.

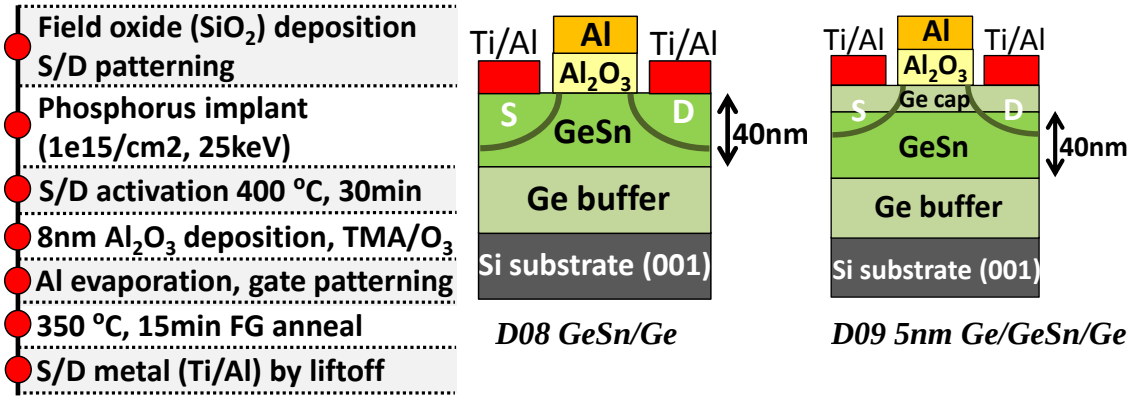


Figure 4.16 Low thermal budget gate-last process flow for fabrication of GeSn channel nMOSFETs.

The interface trap density (D_{it}) is extracted for nMOSFETs fabricated on D08 and D09 using the full conductance method. Measurements are performed at temperatures in the range 77K to 300K to map D_{it} as a function of trap energy ($E-E_v$). As shown in **Figure 4.17**, measured D_{it} is higher for devices without Ge cap on GeSn layer (D08). In both D08 and D09, D_{it} increases significantly towards the conduction band edge and limits the MOSFET drive current, threshold voltage stability.

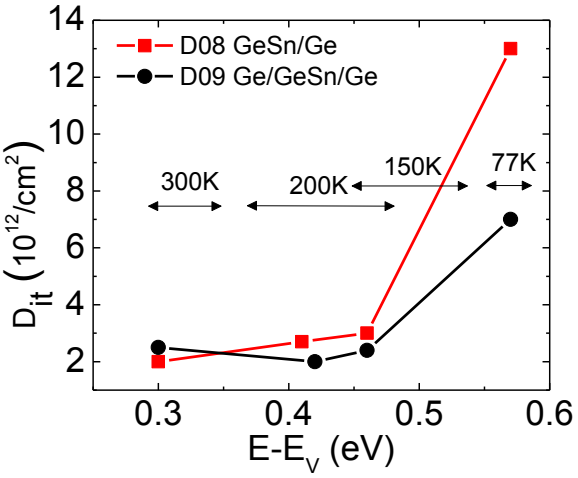


Figure 4.17 D_{it} as a function of energy in the band gap for GeSn nMOSFET. Introduction of Ge cap on GeSn helps reduce the D_{it} near the conduction band.

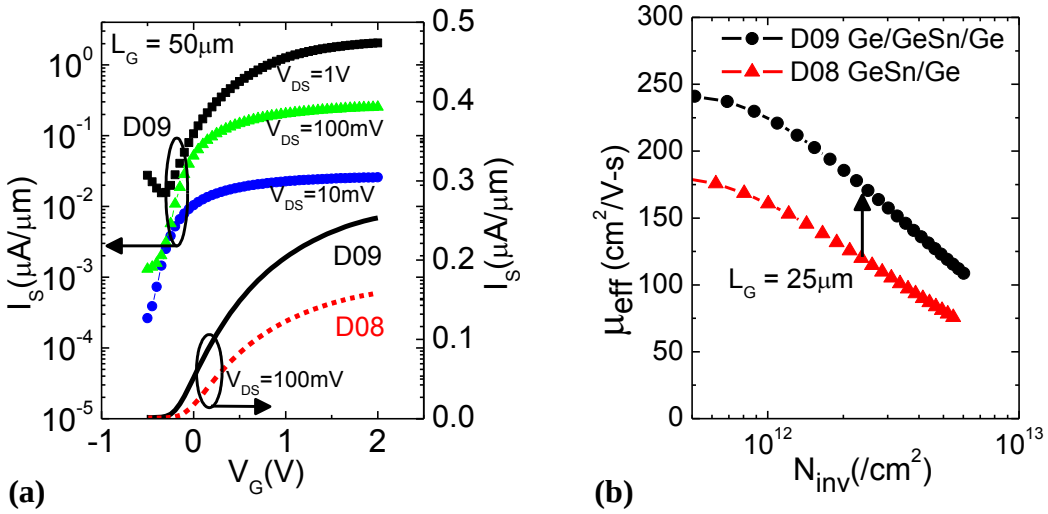


Figure 4.18 (a) I_D-V_G characteristics of nMOSFETs on D08 and D09. D09 shows ~2x higher current than D08. **(b)** Inversion layer electron mobility extracted using split CV method. Higher electron mobility is observed in nMOSFET on D09 (GeSn capped with Ge)

Measured I_D-V_G characteristics and effective mobility are shown in **Figure 4.18**. Devices on D09 show higher drive current and effective electron mobility than

on D08 due to the reduction in the conduction band D_{it} upon addition of the thin Ge cap. Depending upon the band offset between GeSn (5% Sn) and Ge, conduction through 5nm Ge cap may also contribute to higher drive current in D09.

Next, the method of forming n+/p junction through phosphorus ion implantation followed by a thermal anneal is investigated in more detail. **Figure 4.19a** shows the (004) omega-2theta XRD scan of the GeSn sample implanted with $10^{15}/cm^2$ of phosphorus (P) at energy of 25 keV, both before and after the activation thermal anneal. The XRD scan of the as-grown GeSn sample subjected to the same thermal budget is also plotted for comparison.

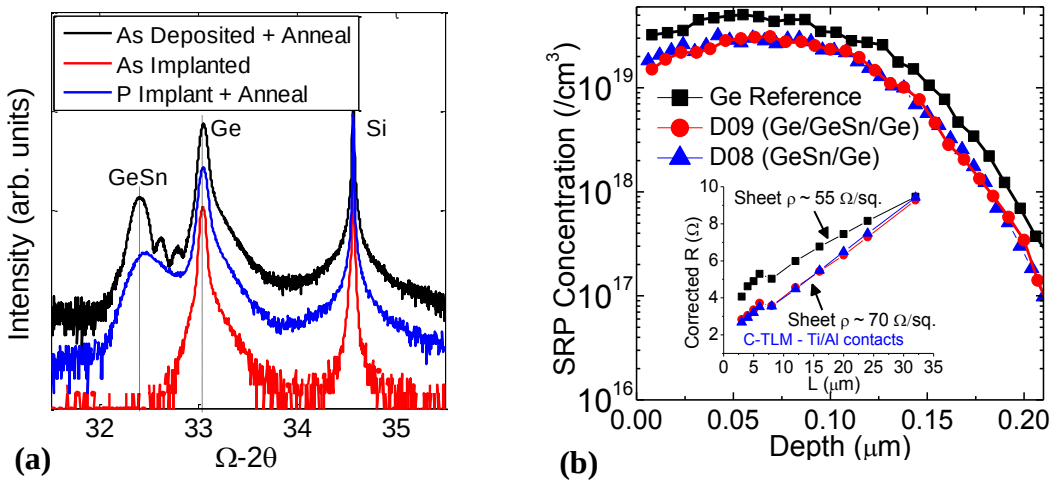


Figure 4.19 (a) (004) omega-2theta XRD scan showing the effect of P implant and thermal anneal on the crystallinity of GeSn layer. **(b)** Active dopant concentration in the Ge and GeSn n+ regions formed by P implant+anneal as measured by SRP method. Inset in (b) shows the results from c-TLM measurements on GeSn and Ge n+ layers formed by P implant+anneal.

In **Figure 4.19a**, the absence of GeSn peak in the as-implanted samples indicates complete amorphization of GeSn layer upon P implant. A subsequent thermal anneal results in a broad GeSn peak without noticeable thickness fringes, suggesting only a partial annihilation of the implant damage. Therefore, the thermal anneal is unable to recover the GeSn crystallinity to as-grown levels. Note that the thermal budget used here (400 ºC, 30 min) does not result in any strain-relaxation or Sn precipitation in the GeSn layer.

The spreading resistance profiling (SRP) method used for estimating the concentration of active dopants shows that the residual implant damage in GeSn contributes towards deactivation of the implanted P (**Figure 4.19b**). The n+ regions in GeSn show ~2X reduction in the concentration of active n-dopants as compared with a Ge-control. Additionally, the sheet resistance extracted from circular TLM measurements is ~50% higher on GeSn than on control Ge samples. This increase in sheet resistance of the GeSn n+ layer can be attributed to the lower n+ concentration in GeSn as compared with Ge-control. Therefore, GeSn devices suffer from larger parasitic source/drain and contact resistance due to poor P activation. This analysis suggests that the conventional technique of ion-implantation and thermal anneal is not well-suited for forming n+/p junctions in GeSn. *In-situ* doped, epitaxial re-growth of the source/drain regions is perhaps a more fitting solution in this scenario.

4.2.2 Interface engineering for Ge, GeSn nMOSFETs

In the previous section, it was discovered that the conventional Al_2O_3 ALD process using TMA/O_3 results in a high interface trap density at the Al_2O_3/GeSn

interface – especially near the conduction band. These traps capture some of the mobile, inversion channel electrons and reduce the nMOSFET drive current. Coulomb scattering from the trapped electrons results in further reduction of the electron mobility in the inversion channel.

This section describes a novel method for engineering the high-κ/GeSn (or Ge) interface. The method relies on ozone (O_3) oxidation for formation of an interfacial passivation layer (IPL) of $GeSnO_x$ (or GeO_x) at the high-κ/GeSn (or Ge) interface. Key steps involved in gate stack formation are listed in **Figure 4.20**. As shown previously in **Figure 4.11**, dilute HCl clean effectively removes native Sn oxides from the surface. After deposition of 1 nm Al_2O_3 using TMA/O_3 ALD, *in-situ* O_3 oxidation at 400 ºC is carried out to form an interfacial layer of $GeSnO_x$ (or GeO_x) between Al_2O_3 and GeSn (or Ge). In order to increase the total gate oxide thickness and reduce the gate leakage current, an additional capping layer of Al_2O_3 is deposited after the O_3 oxidation step.

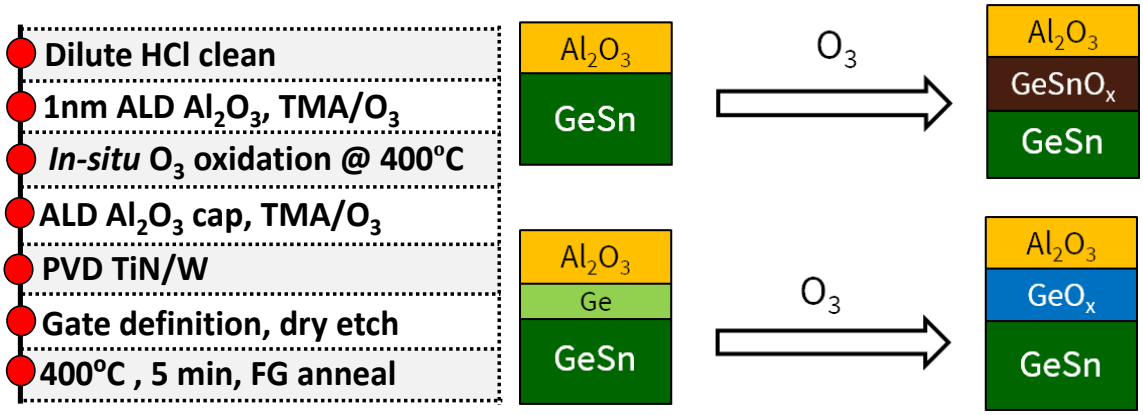


Figure 4.20 Process flow for formation of gate stack on GeSn (or Ge) with an interfacial passivation layer of $GeSnO_x$ (or GeO_x)

A bilayer stack of 30 nm TiN, followed by 40 nm W is used as the gate metal. Metal layers are deposited by sputtering. The W cap avoids increase in the sheet resistance of the TiN layer due to oxidation during the subsequent processing steps. Capacitors are fabricated by patterning the gate metal using reactive ion etching in SF_6 plasma[3].

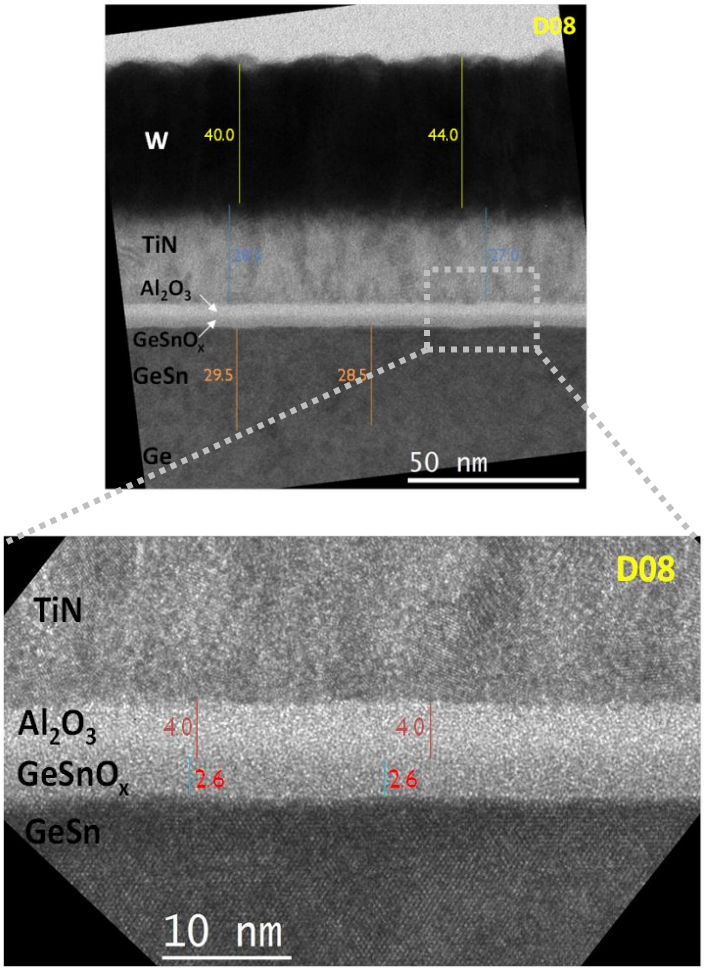


Figure 4.21 X-TEM images showing the gate stack formed on D08 (GeSn (6%)/Ge) using the novel O_3 oxidation process. An oxide interfacial passivation layer (IPL) of $GeSnO_x$ is clearly visible. Thickness of different layers in the stack is indicated in nm.

[3] Al_2O_3 is an excellent etch-stop for SF_6 dry etch.

Figure 4.21 shows the cross sectional TEM images of the resulting gate stack on sample D08 (GeSn (6% Sn)/Ge). The $GeSnO_x$ IPL thickness is measured to be ~2.6nm. Note that if GeSn is capped with Ge, the oxide formed as a result of the *in-situ* oxidation will consume part of the Ge cap layer – forming an IPL of GeO_x. In this particular sample, the O_3 oxidation was performed at a pressure of 6 Torr for a total duration of 10 mins. Note that a precise thickness control of the oxide IPL can be achieved by controlling the initial thickness of Al_2O_3 layer and the O_3 oxidation time. The equivalent oxide thickness of the gate-stack used here is ~4nm.

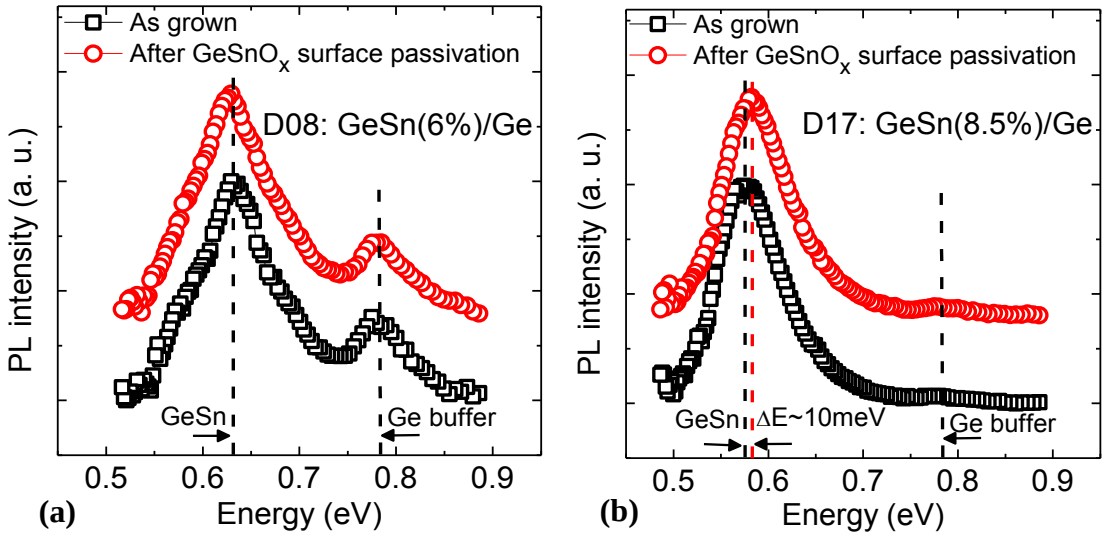


Figure 4.22 PL spectra obtained for **(a)** GeSn (6% Sn) and **(b)** GeSn (8.5% Sn) before and after O_3 oxidation to form $GeSnO_x$ IPL.

The metastable nature of GeSn raises concerns over the thermal stability of the material as it undergoes processing involving a sizeable thermal budget. Since the band gap in GeSn is strongly dependent upon the substitutional Sn content in the alloy (**Figure 2.10**), a change in the peak PL position can be considered as a reliable

indicator of any signs of Sn precipitation (surface or bulk). **Figure 4.22** shows the PL spectra as recorded for samples containing 6% and 8.5% Sn – both before and after the 400 ºC O_3 oxidation step. As the Sn content in GeSn is increased from 6% to 8.5%, the peak PL shifts to smaller energies indicating a reduction in the band gap. Also, since the strain splits the degeneracy of light and heavy hole (LH, HH) valleys, the direct-gap transitions from Γ-LH, Γ-HH and the indirect-gap transitions from L-LH, L-HH are expected to contribute to the broadening of the PL peak. Nonetheless, the strong PL spectra obtained for GeSn containing 6% Sn and 8.5% Sn prior to gate stack formation, confirms the high initial quality of GeSn layers. The PL spectra obtained on these samples after Al_2O_3 deposition and O_3 oxidation do not show any significant shift in peak PL energy. This suggests that the oxidation thermal budget does not result in any Sn precipitation or any noticeable degradation in the GeSn material quality.

4.2.3 Gate-first process

Using the $GeSnO_x$ (or GeO_x) IPL formation method described above, MOS capacitors are fabricated on the following GeSn samples:

- **D08**: GeSn (6% Sn), no Ge cap
- **D09:** GeSn (6% Sn), 5 nm Ge cap
- **D10:** GeSn (6% Sn), 2 nm Ge cap
- **D17**: GeSn (8.5% Sn), no Ge cap
- **D19**: GeSn (8.5% Sn), 2 nm Ge cap

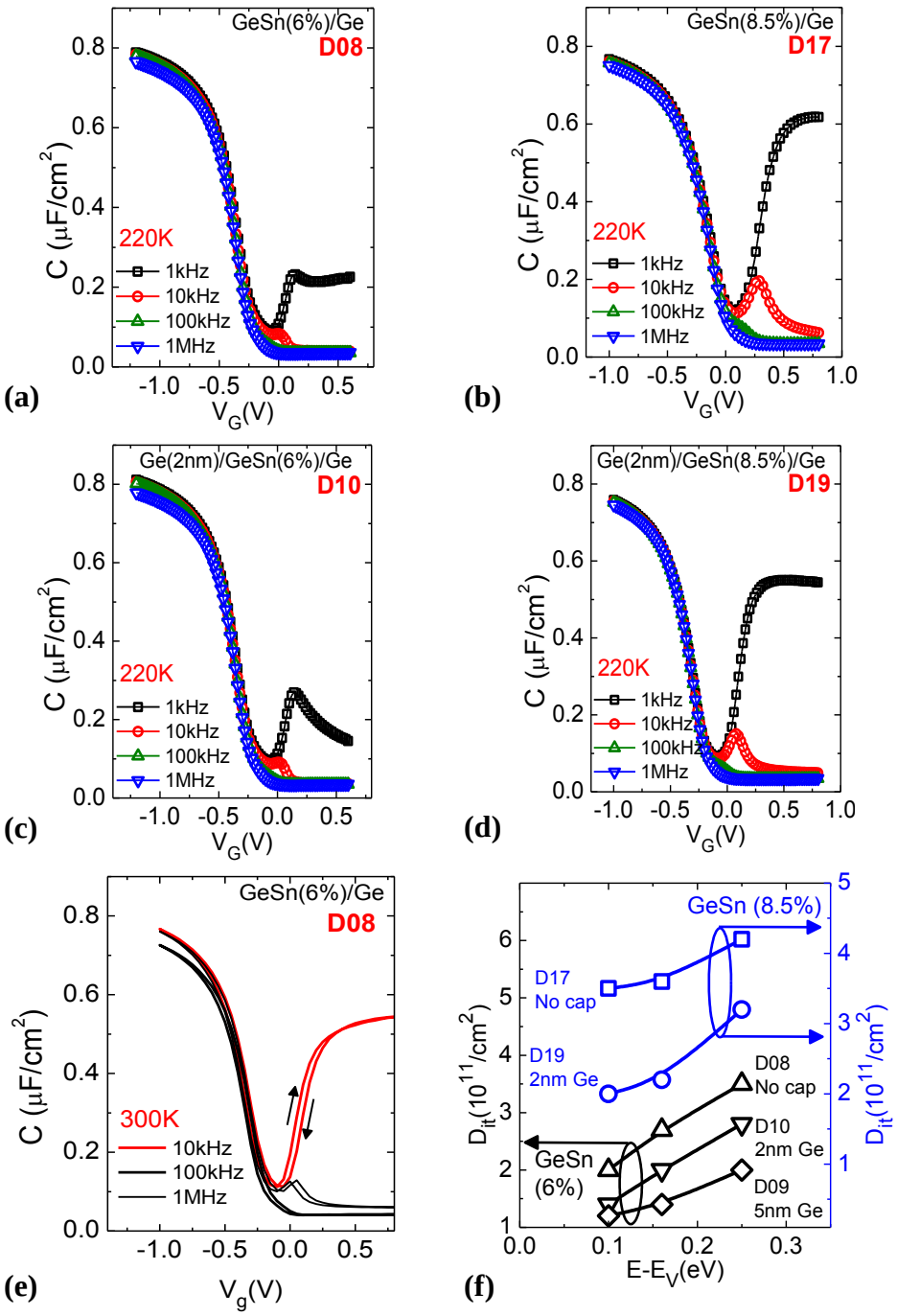


Figure 4.23 p-MOSCAP C-V characteristics at 220 K for MOS capacitors on GeSn with **(a)** 6% Sn, no Ge cap, **(b)** 8.5% Sn and no Ge cap, **(c)** 6% Sn, 2 nm Ge cap and (d) 8.5% Sn, 2 nm Ge cap, **(e)** Hysteresis in C-V characteristics for p-MOSCAPs on GeSn (6% Sn), no Ge cap **(f)** D_{it} near the valence band.

Figure 4.23a-d shows the C-V characteristics of MOS capacitors fabricated on these GeSn samples. Note that the undoped as-grown CVD Ge and GeSn tend to be slightly p-type with hole concentration of ~ $10^{16}/cm^3$. The MOS capacitors show negligible frequency dispersion in both depletion and accumulation. In addition, the steep transition from accumulation to inversion as well as the low flat band hysteresis of less than 50mV (**Figure 4.23e)** attest to the high quality of the oxide/semiconductor interface.

Low temperature conductance method for measuring the D_{it}, when applied to p-MOSCAPs, reveals the trap distribution in the lower half of the band gap (towards the valence band). As shown in **Figure 4.23f**, the D_{it} near the valence band stays in the 10^{11}/cm2 regime for all the samples. There is only a slight increase in trap density as the Sn% in the GeSn is increased from 6% to 8.5%. As seen previously in section 4.2.1, introduction of a thin Ge cap helps reduce the trap density for both 6% and 8.5% GeSn. Also, note that the extracted D_{it} increases as the trap energy approaches mid-gap. This is most likely an artefact of the conductance measurement on MOS capacitors. The small band gap of GeSn makes it particularly susceptible to the "weak inversion" phenomenon, causing an overestimation of the conductance response (and hence the D_{it}) near the mid-gap. The contribution of weak inversion towards the MOS conductance response can be eliminated by applying the conductance method on a MOSFET (the full-conductance method as explained in [**69**]).

The W/TiN/Al2O3/$GeSnO_x$/GeSn gate stack can be integrated into a low-thermal budget process flow as shown in **Figure 4.24**. Source/drain are formed by

phosphorus implantation at dose of $10^{15}/cm^2$ followed by activation anneal at 400 ºC for 5 minutes.

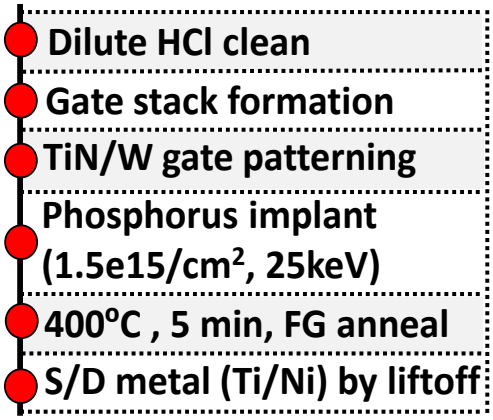


Figure 4.24 Key steps in the low thermal budget gate first process flow for fabricating nMOSFETs on CVD-grown GeSn.

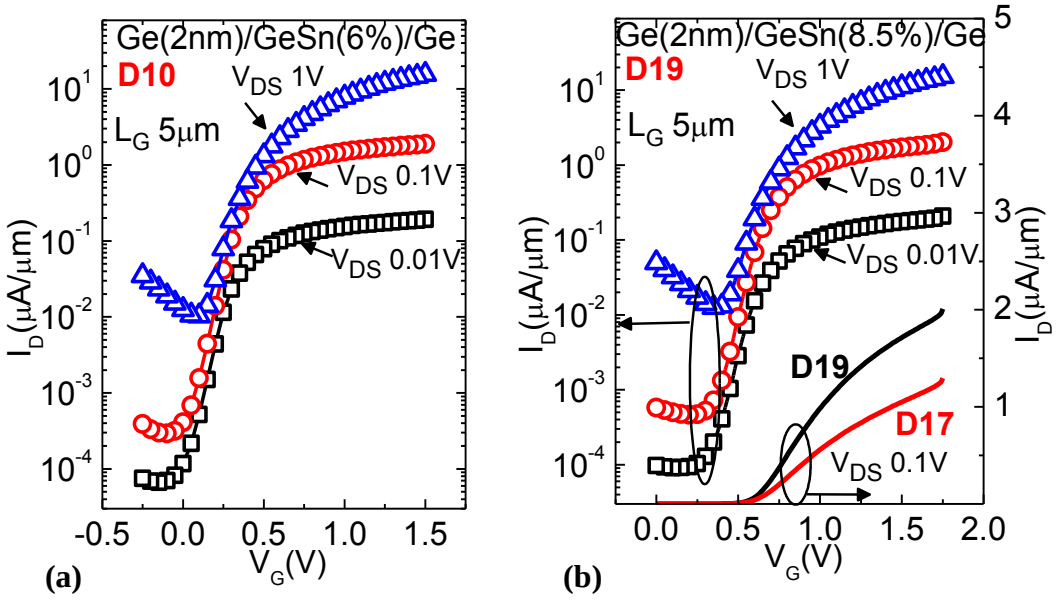


Figure 4.25 I_D-V_G characteristics for **(a) D10**: 2 nm Ge cap/GeSn (6% Sn)/Ge and **(b) D19**: 2 nm Ge cap/GeSn (8.5% Sn)/Ge.

It was shown in the previous section that such a method of source/drain formation is sub-optimal in the case of GeSn due to a potential increase in the source/drain parasitic resistances (R_{SD}). However, the elevated R_{SD} is not expected to significantly distort the overall DC characteristics of the long-channel (>1 μm) nMOSFET being investigated here. This is mainly because in the long-channel transistor, the channel resistance is much larger (by at least 1-2 orders of magnitude) than R_{SD}. In **Figure 4.25**, the nMOSFETs on GeSn with 6% and 8.5% channel Sn content show excellent DC I_D-V_G characteristics, confirming the effectiveness of the low thermal budget process and the surface passivation scheme for a wide range of Sn compositions.

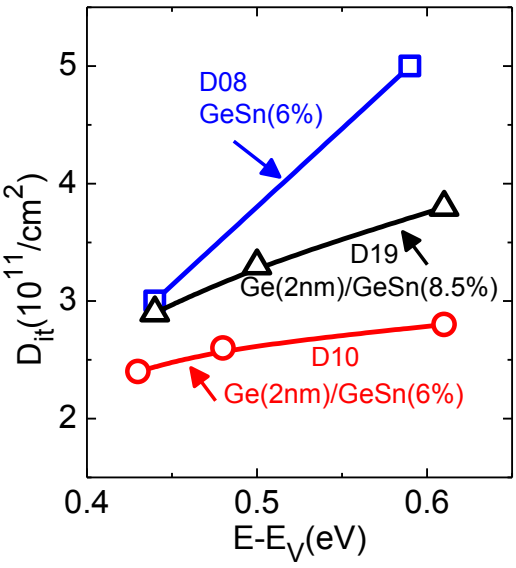


Figure 4.26 D_{it} near the conduction band as extracted using the full-conductance method on nMOSFETs with 6% and 8.5% Sn.

The full-conductance method is applied to the nMOSFET inversion regime to extract the D_{it} in the top half of the band gap (near the conduction band) as shown in

Figure 4.26. The D_{it} is found to be in the low $10^{11}/cm^2$ range, even near the conduction band edge. This corresponds to more than an order of magnitude reduction in D_{it} as compared with that obtained for the conventional TMA/O_3 ALD process without any $GeSnO_x$ or GeO_x IPL (**Figure 4.17**). Also, note that addition of thin Ge cap on GeSn, followed by oxidation of the Ge cap layer to form GeO_x IPL helps reduce D_{it} quite significantly.

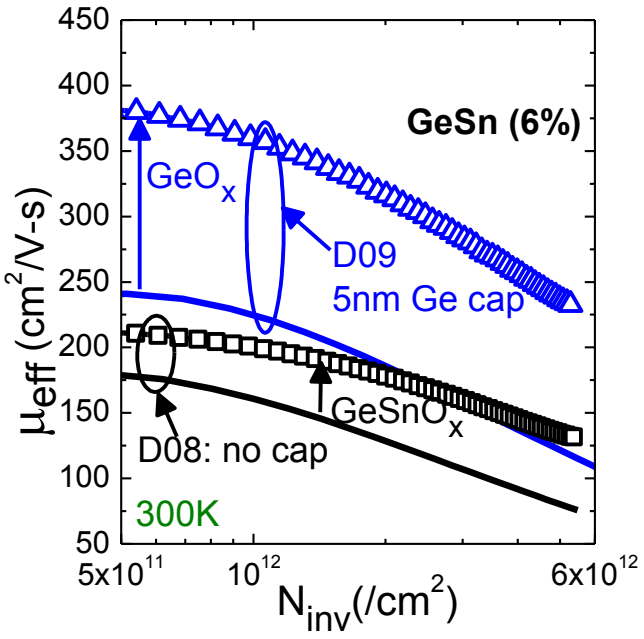


Figure 4.27 Effect of $GeSnO_x$ or GeO_x IPL: Comparison of electron effective mobility extracted for GeSn nMOSFETs with (symbols) and without (lines) $GeSnO_x$ or GeO_x IPL.

The reduction in D_{it}, especially near the conduction band, increases the nMOSFET on-current and improves the electron mobility. **Figure 4.27** compares the electron mobility for GeSn (6% Sn) nMOSFETs both with and without the $GeSnO_x$ passivation layer. The addition of an IPL of $GeSnO_x$ results in approximately 50%

increase in effective electron mobility. Using this method, a larger improvement is observed if GeSn is capped with Ge (sample D09 in **Figure 4.27**). In such a case, the IPL is composed of a thin layer of GeO_x. This suggests that GeO_x may be a better suited as the IPL. However, since the sample D09 has a Ge cap thickness of 5 nm, it is unlikely that the entire Ge cap is consumed during the oxidation process to form GeO_x. Therefore, it is possible that the remainder of the Ge cap still contributes to the electron conduction in the nMOSFET on D09.

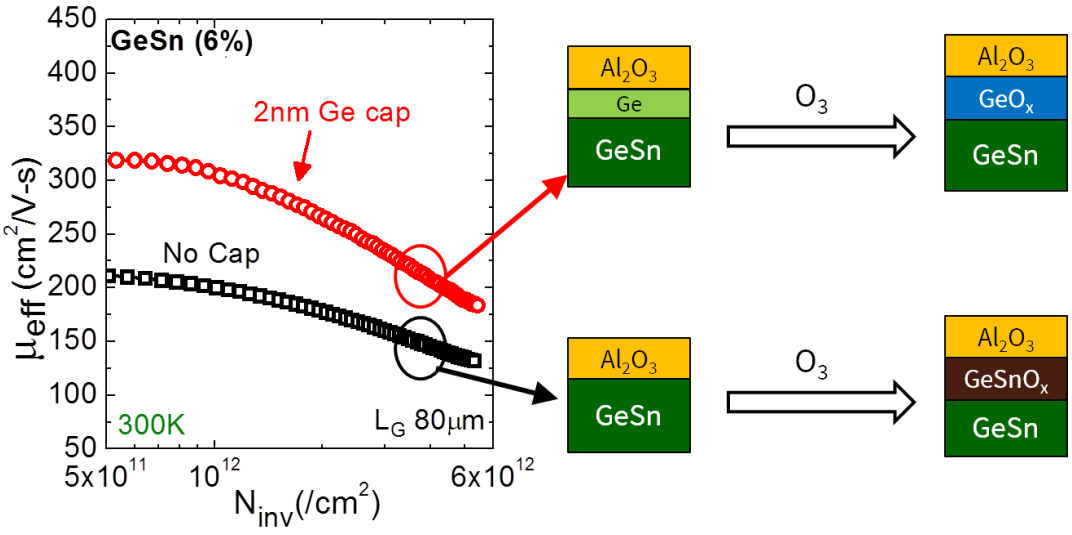


Figure 4.28 Effect of Ge cap thickness: Comparison of effective electron mobility as extracted for nMOSFETs on GeSn (6% Sn) with no Ge cap and 2 nm Ge cap.

To investigate this further, electron mobility is extracted for nMOSFETs fabricated on GeSn (6% Sn) with 2 nm Ge cap (sample D10). **Figure 4.28** shows the comparison of extracted electron mobility on samples with the same Sn content of 6% Sn and a gate stack containing the oxide IPL but different Ge cap thicknesses (no Ge cap and 2 nm Ge cap). As shown in **Figure 4.21**, the thickness of the oxide layer

formed during the O_3 oxidation step is ~2.6 nm. Hence, it is very likely that the 2 nm thick Ge cap in sample D10 is fully consumed during the gate stack formation step, forming an IPL of GeO_x and resulting in the inversion channel to lie primarily in the GeSn layer. The reduction in D_{it} observed upon introduction of Ge cap and subsequent O_3 oxidation to form a GeO_x IPL, translates into increase in electron mobility. The higher electron mobility observed for GeO_x (D10) compared with $GeSnO_x$ (D08) as the IPL suggests *controlled oxidation of a thin Ge cap on GeSn as the optimal route towards achieving high quality GeSn surface passivation*.

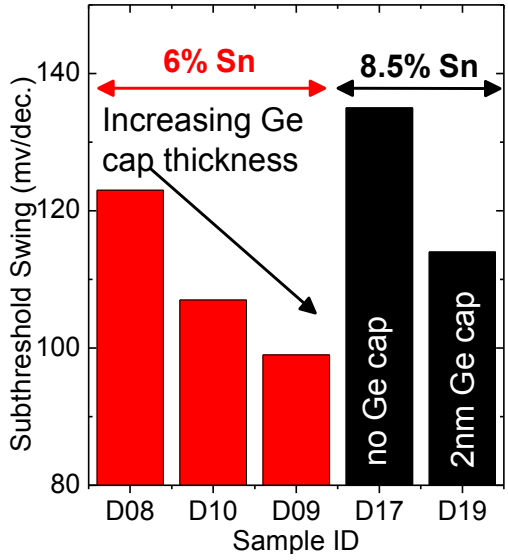


Figure 4.29 Comparison of the SS at 300 K as extracted for GeSn nMOSFETs with $GeSnO_x$ or GeO_x IPL.

In addition to the large drive current, another important metric for estimating the overall performance of the MOSFET is its ability to switch from off-state to on-state over a small range of gate voltage. The subthreshold swing (SS) of the MOSFET measures the amount of gate voltage needed to induce an order of magnitude change

in the drain current. For a surface channel MOSFETs, the SS depends critically on the number of traps at the interface. For an ideal MOSFET, with no interface traps and perfect gate control of the channel, the minimum possible SS at 300 K is ~60mV/dec. As shown in **Figure 4.29,** the nMOSFET subthreshold swing (SS) at 300 K reduces with introduction of thin Ge cap. Only a slight increase in SS is noticeable for D19 (8.5% Sn, 2 nm Ge cap) as compared with D10 (6% Sn, 2nm Ge cap) corresponding to marginal increase in D_{it} observed in D19. SS for all devices has been measured to be less than 135mV/dec. The trend in SS correlates well with the trend observed in D_{it} and electron mobility amongst the different samples considered here. A reduction in D_{it} improves both the SS as well as the effective electron mobility.

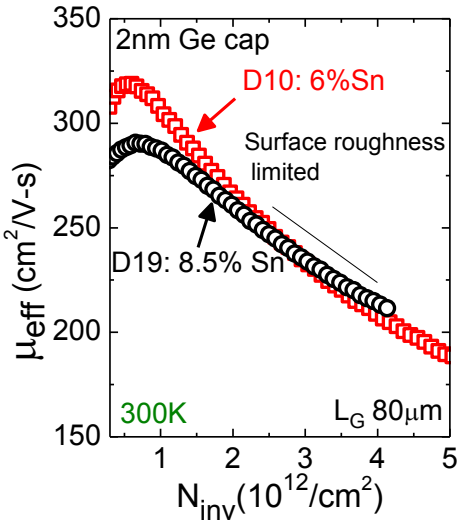


Figure 4.30 Effect of increase in channel Sn%: Comparison of effective electron mobility in nMOSFETs with different Sn% in the channel. GeO_x forms the IPL.

A comparison of the effective electron mobility between nMOSFET on D10 (6% Sn, 2 nm Ge cap) and D19 (8.5% Sn, 2 nm Ge cap) in **Figure 4.30** reveals high field mobility to be limited by surface roughness scattering and independent of

channel Sn%, indicating alloy scattering to not be the dominant mobility degradation mechanism in current devices. All devices show slight reduction in peak and high field mobility with decreasing temperature suggesting mobility limited by coulomb scattering and surface roughness scattering as shown in **Figure 4.31.**

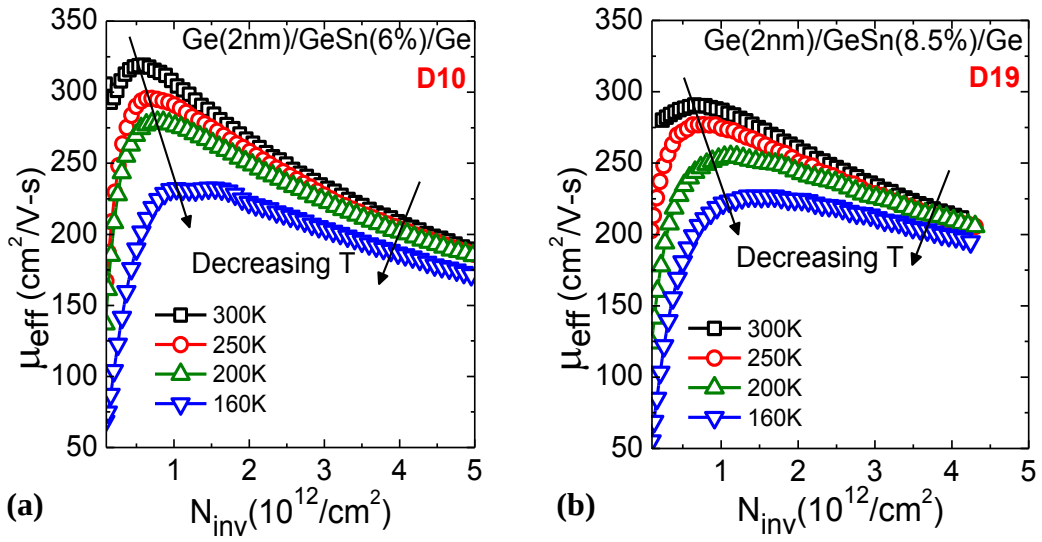


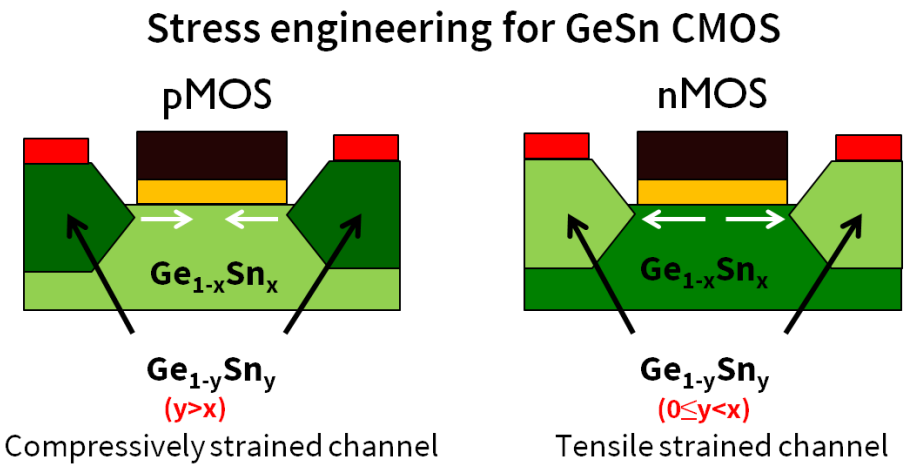
Figure 4.31 Temperature dependent inversion channel mobility for (a) D10: 2 nm Ge cap/ GeSn (6% Sn) (b) D19: 2 nm Ge cap/GeSn(8.5% Sn).

4.3 Summary

In this chapter, important aspects of a CMOS technology using GeSn as a channel material were developed. GeSn thin films grown on Ge, containing Sn% as high as 8.5% were used as a platform for fabrication and characterization of p and n channel GeSn MOSFETs. Low thermal budget fabrication processes were developed in order to preserve the integrity of the metastable GeSn and avoid Sn precipitation in the channel region. The compressive strain present in the GeSn films grown epitaxially on Ge was shown to improve the hole mobility. Compressively strained

GeSn pMOSFETs were found to outperform the control Ge devices in terms of inversion channel hole mobility and drive current. On the contrary, compressive strain in GeSn was found to degrade the electron mobility. Nevertheless, the current material platform, that reflects the state-of-the-art in high quality GeSn material growth, was used for developing a novel GeSn surface passivation scheme that achieves record low interface trap density at the high-κ/GeSn interface.

With further advances in material growth to achieve strain-free or tensile strained GeSn, in conjunction with the interface engineering techniques presented here, significant performance benefits can be expected from this material system. The figure below shows a possible CMOS solution built around the idea of stress engineering the channel to obtain the desired enhancement in performance for both n and p channel devices. For instance, the source/drain regions formed of GeSn with lower Sn content than the channel induce tensile stress in the channel region which can potentially boost the nMOSFET performance. In the next chapter, this idea is explored is more detail.



Chapter 5

A Solution for 7 nm FinFET CMOS: Stress Engineering using Si, Ge and Sn

In this chapter the Ge and GeSn MOSFET technology developed in the previous chapters is applied for designing a FinFET-based CMOS solution for transistor dimensions expected in a 7 nm technology node. Si and Si-compatible group IV elements (Ge and Sn) and their alloys (SiGe, GeSn and SiGeSn) are employed for channel stress engineering in order to achieve high on-current while meeting the ITRS requirements for transistor off-current.

5.1 Background

Over the past decade, stress engineering has proved to be critical in achieving improved Si-CMOS device performance every successive technology node. Strained-Si technology was first introduced in production at the 90 nm technology node in order to boost the transistor performance [**75**]. The use of embedded SiGe stressors in the source/drain provided the necessary uniaxial compressive stress in the channel to improve hole mobility (pMOSFET performance). For electron mobility enhancement (nMOSFET performance), a silicon nitride stress layer induced the required tensile

stress in the channel. Since then, several innovations in transistor technology have been built on top of the strained-Si technology to deliver the performance benefits of transistor scaling in accordance with Moore's law (**Figure 5.1**).

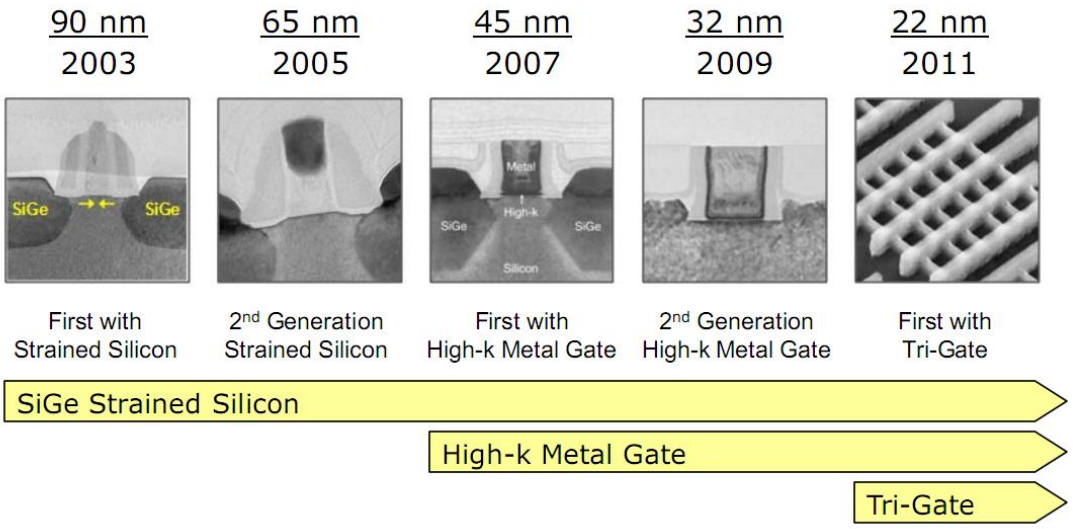


Figure 5.1 Key innovations driving the Si-CMOS beyond the 90 nm technology node. (Source: Intel Developer Forum, 2011)

These innovations include the use of high-κ metal gate technology which helps reduce the equivalent gate oxide thickness without incurring a penalty in terms of excessive gate leakage current. More recently, the migration from conventional planar transistors to non-planar 3D transistors (Tri-gate/FinFETs) has enabled further device scaling by providing good electrostatic control of the transistor channel and mitigating the short-channel effects [**76**]. As a result, tri-gate/FinFET transistors show reduced leakage compared with their planar counterparts (**Figure 5.2**).

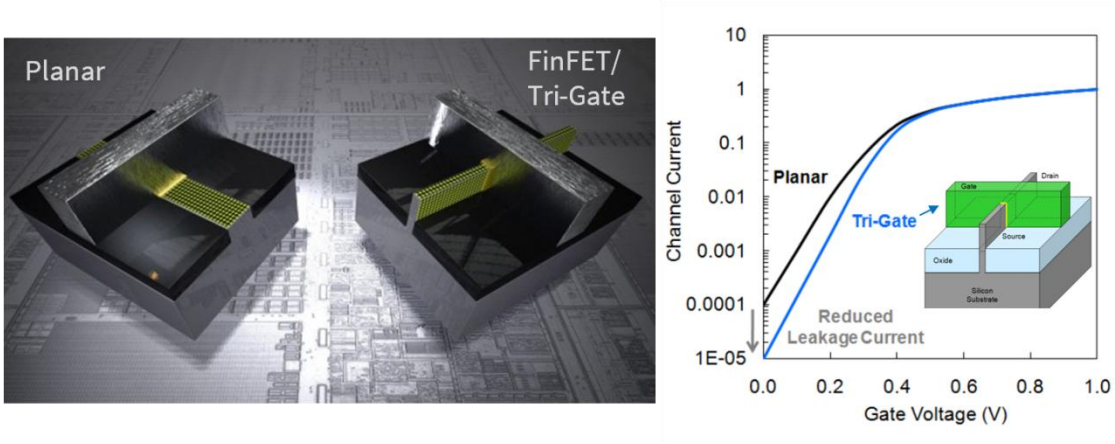


Figure 5.2 Better gate control of the channel in tri-gate/FinFETs result in lower leakage current. FinFET has become the preferred transistor design for high performance Si-CMOS logic post-22 nm technology (Source: Intel Developer Forum, 2011).

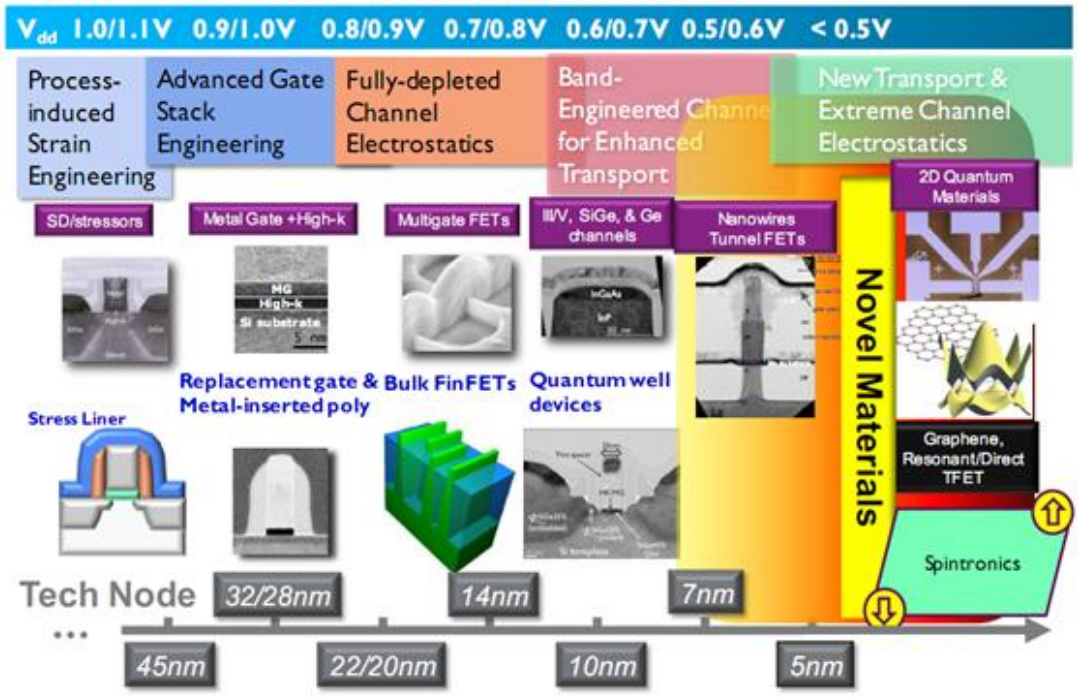


Figure 5.3 Different solutions proposed for future CMOS technologies (Source: IMEC)

As search continues for solutions that extend the life of Moore's law beyond Si-CMOS, several options are under investigation that promises to deliver the performance benefits of further device scaling. **Figure 5.3** shows a possible roadmap for future technology scaling. Alternate channel materials such as III-V and Ge that show higher electron and hole mobilities compared with Si are being considered for future technology nodes. High electron mobility III-V channel materials such as InGaAs, co-integrated with materials such as SiGe and Ge that show high hole mobility, has been touted as one of the more feasible route for realizing the next generation of CMOS devices. Although III-V based proof-of-concept MOSFET devices have already been shown to deliver high performance [**77**,**78**], such solutions are riddled with formidable challenges in integration of III-V materials on Si platform, resulting in potentially higher costs and associated difficulties in high-volume manufacturing.

This chapter presents a FinFET-based CMOS solution using group IV elements and alloys for device dimensions expected in a 7 nm technology node. The inclusion of Sn-based alloys – GeSn and SiGeSn significantly expands the design space for continued band gap and stress engineering in a Si-compatible platform. In the proposed design, the use of a common buffer layer for n and p channel devices is leveraged to alleviate the difficulties in integration of different channel materials. A detailed simulation study is performed in order to evaluate the performance of the CMOS devices.

5.2 Proposed CMOS design

In the simulated design, starting with Si (001) substrate, a buffer layer of relaxed-Ge is grown using well-established heteroepitaxy methods [**79**] that can achieve $<10^6/cm^2$ threading dislocation density [**80**] in the top Ge region. Next, a layer of $Si_{0.32}GeSn_{0.08}$ is grown on top of this Ge virtual substrate.

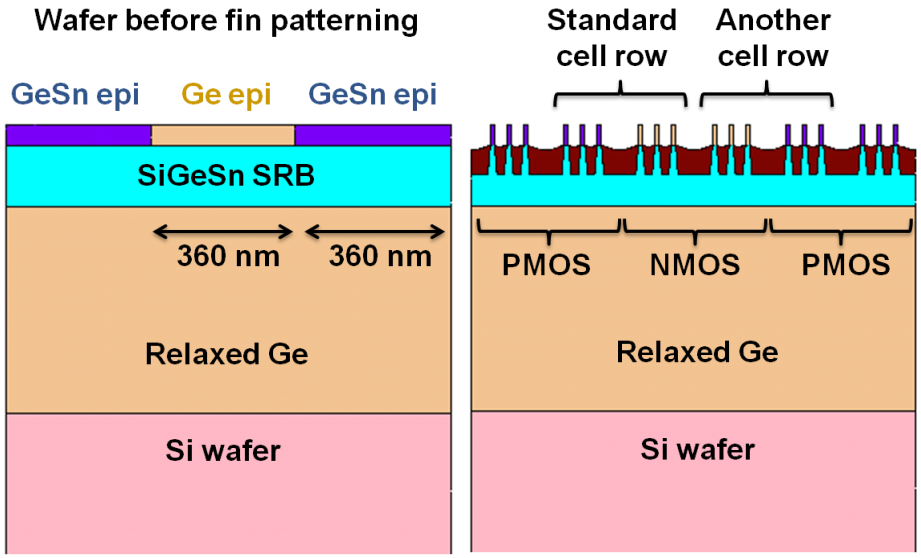


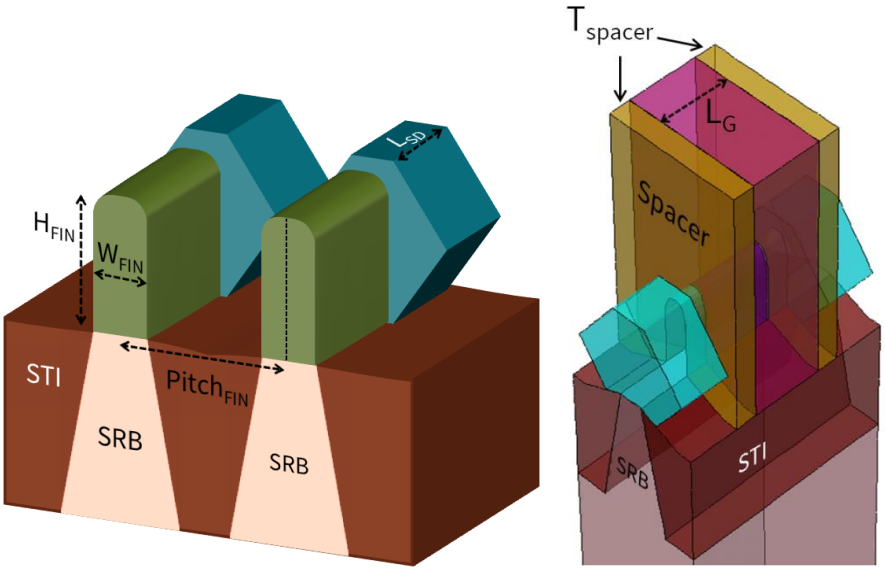
Figure 5.4 Common strain-relaxed buffer (SRB) solution for p and n MOSFETs. SiGeSn lattice-matched to Ge is used as SRB, Ge as the channel for NMOS and GeSn (4% Sn) as the channel for PMOS.

The use of the ternary SiGeSn alloy enables decoupling of the band gap with the lattice constant i.e. the alloy band gap can be varied while keeping the lattice constant invariant by suitably adjusting the Si/Sn ratio. SiGeSn with 32% Si and 8% Sn is lattice matched to Ge and has a band gap of 0.87 eV [**81**]. The larger band gap of SiGeSn as compared with Ge (0.87 eV v/s 0.66 eV) helps reduce the parasitic MOSFET leakage through the substrate. This SiGeSn layer serves as the common

strain-relaxed buffer (SRB) for selective epitaxy of p and n MOSFET channel materials: GeSn (4% Sn) and Ge, respectively as shown in **Figure 5.4**.

Table 5.1 FinFET design rules for 10 nm and 7nm technology nodes. All dimensions are in nm. Schematics indicating important device dimensions are also shown.

Technology	**10 nm**	**7 nm**
Gate pitch	60	45
Channel length (L_G)	20	15
Spacer thickness (T_{spacer})	10	7
Fin width (W_{FIN})	8	6
Fin height (H_{FIN})	27	20
Fin pitch ($Pitch_{FIN}$)	45	35
Contact size (L_{SD})	20	15
EOT	0.85	0.80
S/D epi width	38	30



Here, the focus is on the device dimensions as expected for the 7 nm technology node. Some of the key FinFET design rules for this technology are listed in **Table 5.1**. Key steps in the fabrication of p and n channel MOSFETs in accordance with 7 nm design rules are shown in **Figure 5.5**. After fin patterning and dummy gate, spacer formation, source/drain (S/D) regions are recessed and *in-situ* doped GeSn (8% Sn) (PMOS) and $Si_{0.3}Ge_{0.7}$ (NMOS) are epitaxially re-grown. S/D regions of adjoining fins do not merge. The channel region is kept undoped.

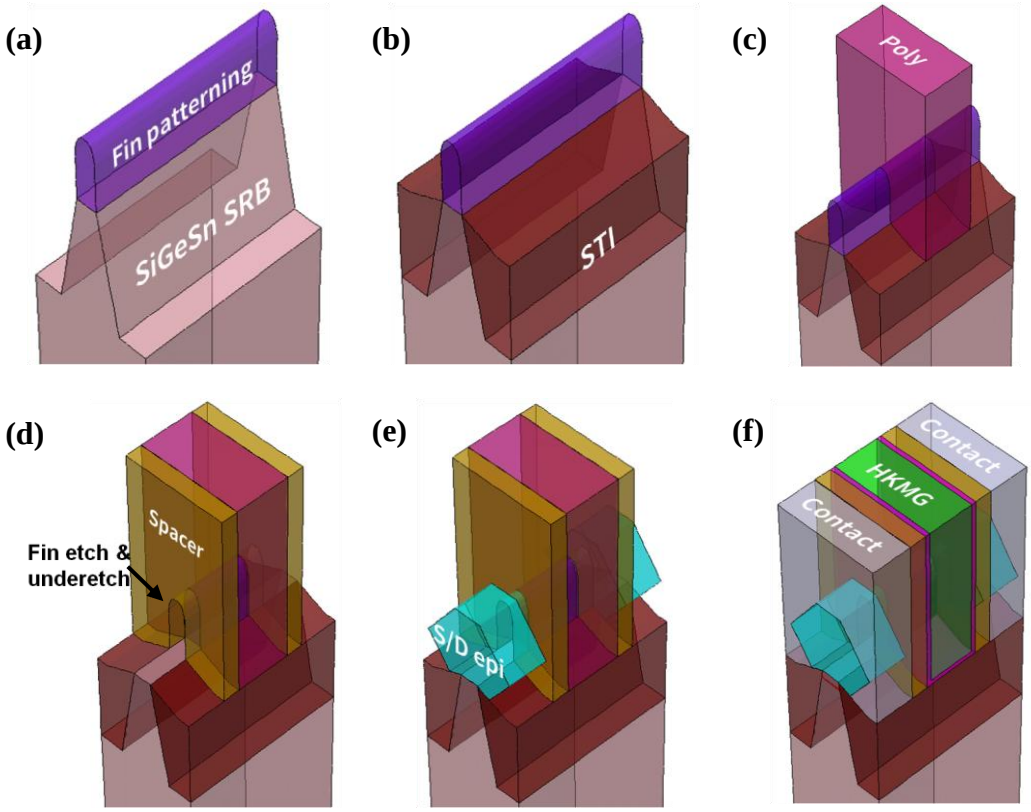


Figure 5.5 MOSFET fabrication process flow **(a)** Fin, SiGeSn SRB patterning, **(b)** STI formation, **(c)** Poly gate definition, **(d)** Spacer formation and S/D recess, **(e)** *In-situ* doped S/D epitaxial re-growth and **(f)** Poly removal and gate-last high-κ metal gate (replacement metal gate). Sentaurus sprocess is used for process simulation.

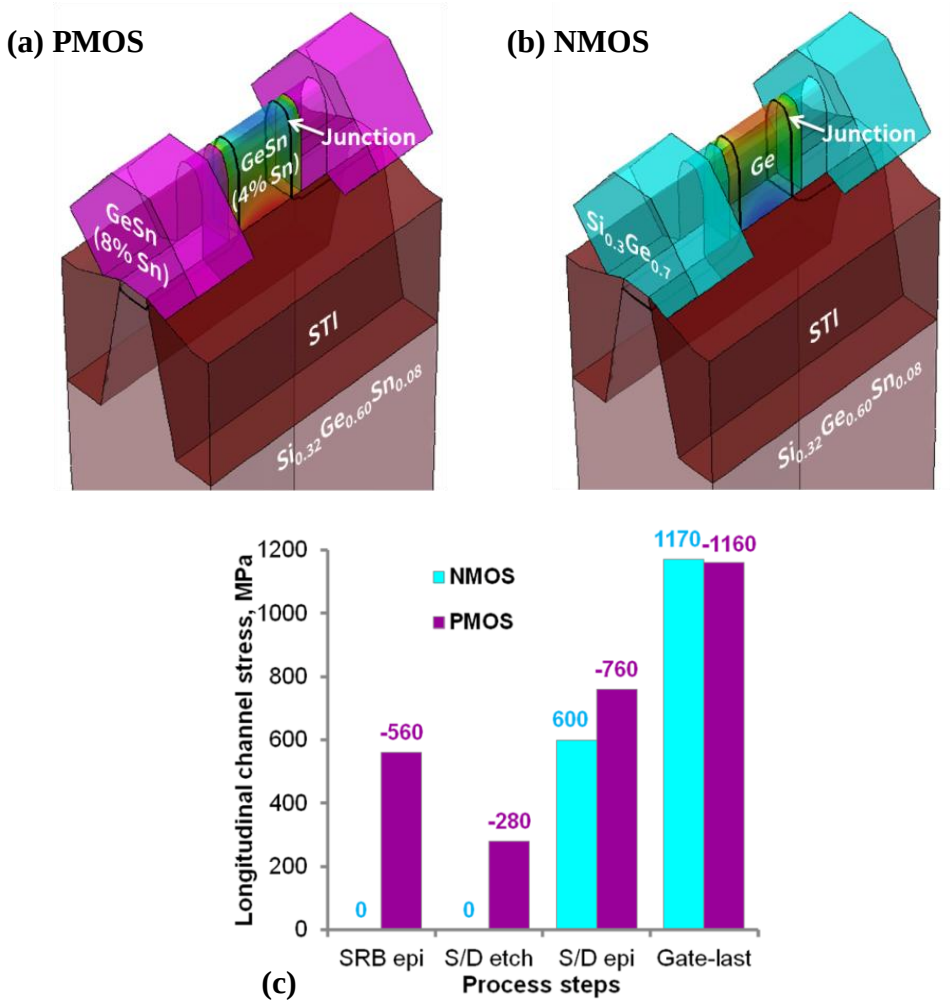


Figure 5.6 (a, b) PMOS and NMOS devices (gate stack, spacers, contacts omitted) fabricated using 7 nm design rules. **PMOS**: GeSn (4% Sn) channel, *in-situ* B-doped GeSn (8% Sn) S/D. **NMOS**: Ge channel, *in-situ* P-doped $Si_{0.3}Ge_{0.7}$ S/D. **(c)** Evolution of average longitudinal stress in p and n MOSFET channel during the process flow outlined in **Figure 5.5**.

Figure 5.6a, b shows the final device configuration for p and n MOSFET devices, respectively. Compressive stress required for hole mobility enhancement is achieved through a combination of growth of GeSn (4% Sn) on SiGeSn SRB and use of GeSn (8% Sn) as PMOS S/D. Similarly, tensile strain for boosting NMOS drive

current is obtained by employing $Si_{0.3}Ge_{0.7}$ S/D stressors. **Figure 5.6c** shows the evolution of PMOS, NMOS channel stress during the fabrication process flow. Note that the dummy gate removal and replacement metal gate formation amplifies the channel stress quite significantly.

This configuration of SRB, channel and S/D materials achieves final longitudinal stress of ±1.1 GPa. In addition to providing beneficial channel stress, high *in-situ* B doping in GeSn (8% Sn) and P doping in SiGe are used to lower the parasitic S/D series and contact resistances.

5.3 Performance evaluation

5.3.1 On-current (I_{ON})

Table 5.2 Simulation parameters for Ge, GeSn (4% Sn) and GeSn (8% Sn). Luttinger parameters are extracted from a 6 band k.p fit to the band structures of section 2.3.

Parameter		**Ge**	**GeSn (4% Sn)**	**GeSn (8% Sn)**
Lattice Constant (Å)		5.650	5.683	5.716
Unstrained Band gap (eV)		0.660	0.615	0.540
Luttinger params.	γ_1	9.37	10.54	11.71
	γ_2	3.01	3.38	3.75
	γ_3	4.02	4.52	5.03
	Δ_{so}	0.306	0.332	0.354

MOSFET on-current (I_{ON} or $I_{D,SAT}$) is estimated using the ballistic MOSFET model described previously in section 2.4. Band structure of Ge, GeSn is calculated

using the alloy-disorder-corrected empirical pseudopotential method as described in section 2.3 and fitted to 6 band k.p dispersion relationship. Table lists the important simulation parameters extracted for Ge and GeSn. The conduction and valence band deformation potentials for GeSn were found to not differ appreciably from that of Ge [**9**].

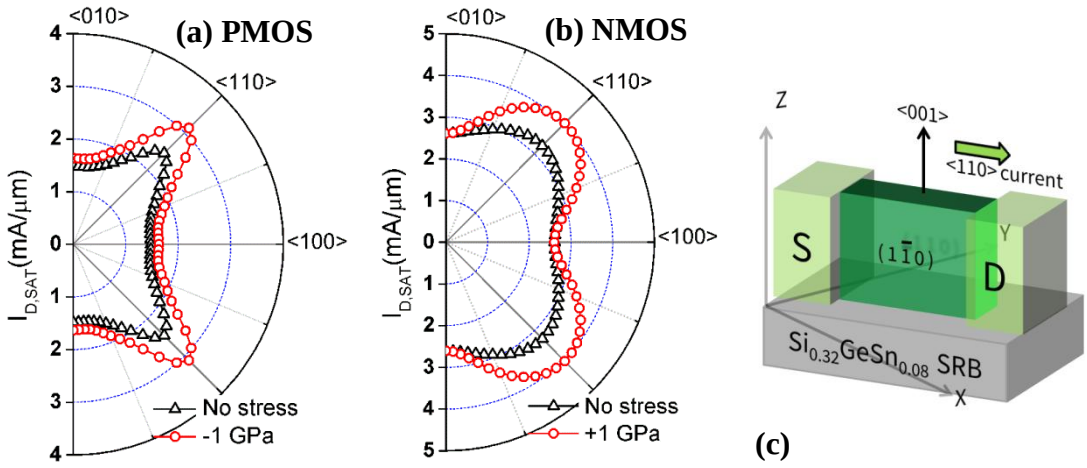


Figure 5.7 Dependence of **(a)** PMOS (GeSn 4% Sn) and **(b)** NMOS (Ge) $I_{D,SAT}$ on fin orientation. (7 nm design rules, V_{DD} = 0.7V, R_S = 0). **(c)** Schematic of a fin aligned with <110> direction on a (001) substrate. (1-10) surface forms the fin sidewall. Current and stress are in <110> direction.

The anisotropic nature of valence and conduction bands, in conjunction with stress-induced band splitting causes I_{ON} to be dependent on the fin orientation. On a (001)-oriented substrate, ballistic I_{ON} is calculated for varying fin orientations and the results are plotted in **Figure 5.7**. The off-current is kept fixed at 100 nA/μm by suitably adjusting the gate metal workfunction. Clearly, fins aligned with the <110>

direction show maximum drive current and maximum gain with uniaxial stress for both PMOS and NMOS.

Insights into the orientation dependence of hole mobility and PMOS I_{ON} in strained Ge can be found elsewhere (for example: [**82**]). Here, the NMOS case is studied in more detail. In the ballistic limit, the MOSFET current can be expressed simply as the product of the carrier inversion charge density (Q_{inv}) and the injection velocity (V_{inj}).

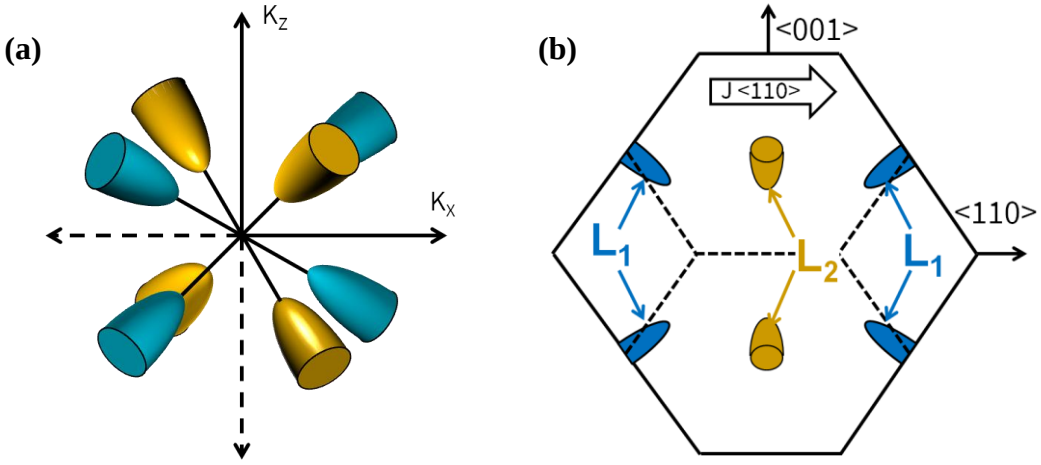
$$I_{ON} = Q_{inv} \times V_{inj}$$

$$\begin{aligned} Q_{inv} &\ \alpha\ m_{DOS} \\ V_{inj} &\ \alpha\ 1/\sqrt{m_t} \end{aligned} \tag{5.1}$$

Effective masses of the transport valley play a central role in determining the MOSFET I_{ON}. Due to 2-D carrier statistics in MOSFET inversion layer, Q_{inv} is proportional to the density of states effective mass (m_{DOS}), whereas the V_{inj} increases with reduction in the transport effective mass (m_t). Consequently, valleys that offer a combination of a high m_{DOS} and a low m_t are ideal for transport. The high electron mobility (and high V_{inj}) of most III-V materials is attributed to the electron transport in low m_{eff} Γ valley. However, the Γ valley is isotropic in nature (same m_{eff} in all directions) and therefore possesses low m_{DOS} in addition to low m_t. As a result, Γ valley electron transport in III-V channel materials is expected to be limited by the 'DOS bottleneck' arising due to the low m_{DOS}. Electron transport in anisotropic

valleys, therefore, might be a potential route for overcoming this inherent trade-off between the DOS (or Q_{inv}) and V_{inj}.

The L conduction band valleys in Ge show very high anisotropy – the ratio of the longitudinal and transverse effective masses for Ge L valley is 20. For the fin oriented in <110> direction, the (1-10) plane forms the sidewall and carries the majority of electron current. The four-fold degenerate L valley conduction band minima in Ge, when projected onto the (1-10) sidewall split into two sets: L_1 and L_2 as shown in **Figure 5.8**. L_1 valleys have high effective mass m_t in the transport direction, resulting in low V_{inj} for electrons occupying these valleys. L_2 valleys, on the other hand, are most favorable for electron transport due to its low m_t as well as high m_{DOS}. To put these numbers into perspective, m_t for Si is ~ 0.2, whereas m_t for $In_{0.53}GaAs$ is close to 0.04.



(c)

	m_t	m_{DOS}	m_{conf}	g
L_1	1.64	0.36	0.082	2
L_2	0.082	0.222	0.224	2

Figure 5.8 (a) Four-fold degenerate L valleys in Ge. **(b)** Projection of Ge L valleys onto the (1-10) sidewall. **(c)** Effective masses of the L_1 and L_2 valleys.

In the case of unstrained Ge, the L_1 and the L_2 valleys are degenerate and hence equally occupied by inversion electrons. The occupancy of low V_{inj} L_1 valleys, degrades the average electron V_{inj} for unstrained Ge. Nevertheless, channel stress, if applied along certain crystallographic directions, can split the degeneracy of the L_1 and L_2 valleys and result in preferential occupancy of low energy valleys.

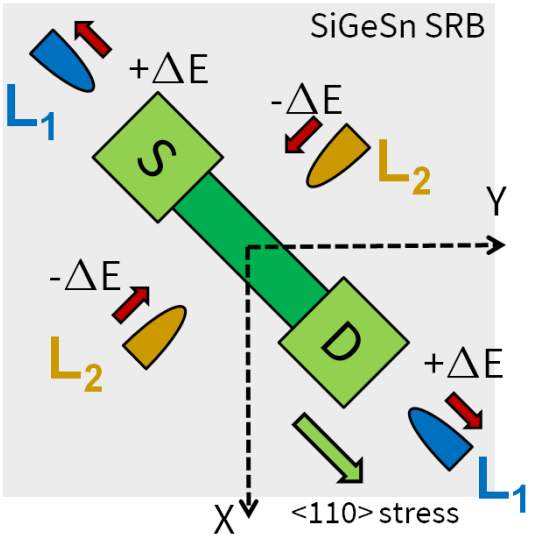


Figure 5.9 <110> uniaxial tensile stress lowers the energy, increases the occupancy of the L_2 valleys. Preferential occupancy of L_2 valleys improves NMOS I_{ON}.

More specifically, application of uniaxial tensile stress in the <110> direction lowers the energy of L_2 valleys as compared with the L_1 valleys (**Figure 5.9**) and increases the occupancy of the low m_t L_2 valleys. Therefore, Ge fins aligned with the

<110> direction, with uniaxial tensile stress also along the <110> direction are preferred for electron transport.

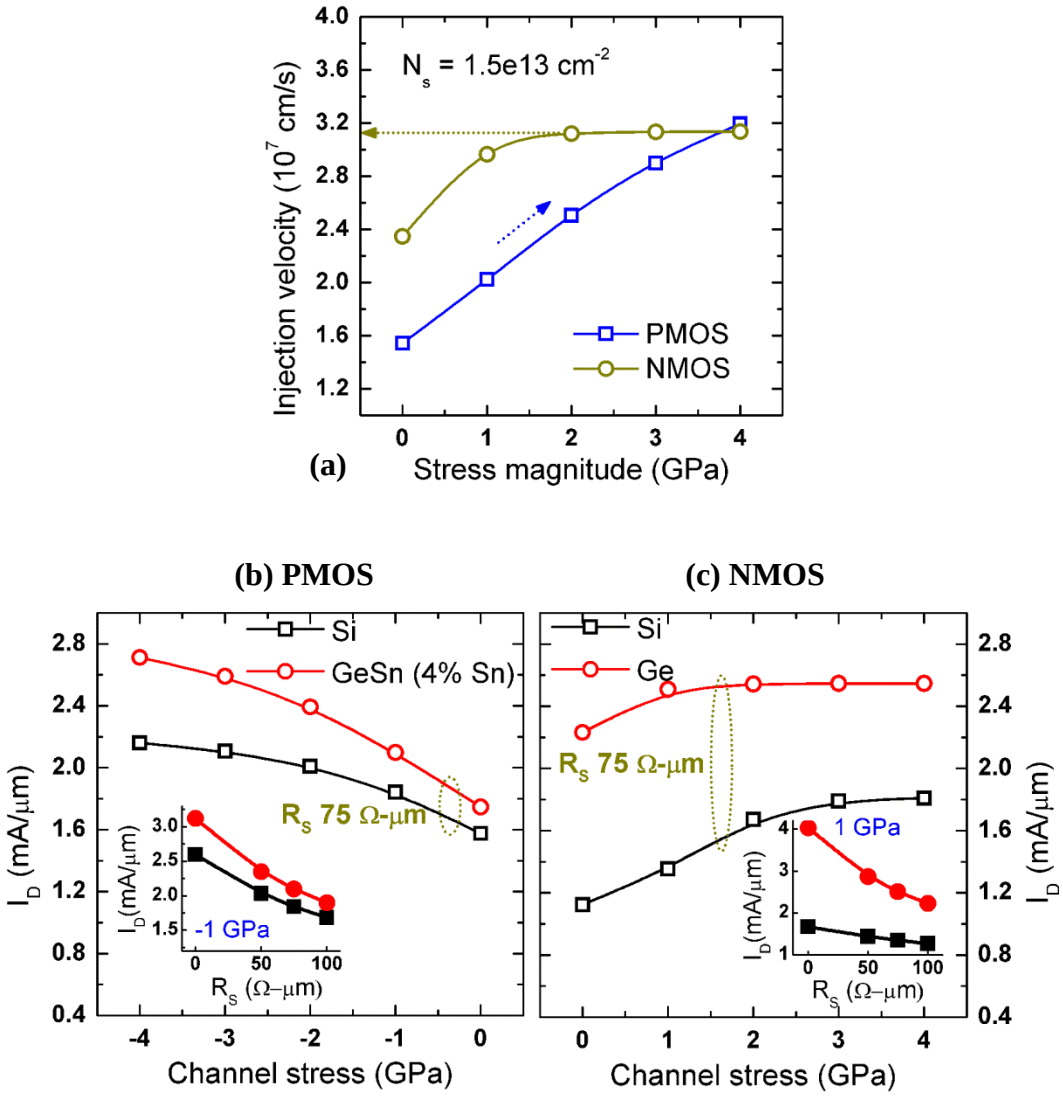


Figure 5.10 (a) Hole (PMOS) and electron (NMOS) V_{inj} as a function of channel stress. Comparison of ballistic I_{ON} for **(b)** Si and GeSn (4% Sn) PMOS, **(c)** Si and Ge NMOS. 7 nm design rules, V_{DD} = 0.7V, I_{OFF} = 100 nA/μm. Insets in **(b)**, **(c)** show the dependence of I_{ON} on R_S for ±1GPa channel stress.

For both PMOS and NMOS, the presence of channel stress improves the V_{inj} and I_{ON} as shown in **Figure 5.10a**. Note that the stress-induced gain in electron V_{inj} shows saturation at 2 GPa tensile stress. On the contrary, the hole V_{inj} continues to increase as the compressive stress in the channel increases. The ballistic I_{ON} for the proposed CMOS design is compared with Si-CMOS in **Figure 5.10b, c.** Clearly, both the strained-GeSn (4% Sn) PMOS and the strained-Ge NMOS comfortably outperform the strained-Si devices in terms of ballistic I_{ON}. Results shown here take into account the effect of parasitic source/drain resistance in the FinFET. The channel to S/D spreading resistance, doped S/D sheet resistance and contact resistance are lumped into a single parameter R_S [**83**].

5.3.2 Off-current (I_{OFF})

The off-current of the transistor is a critical design metric. The CMOS design presented in the previous sections relies on the use of high-mobility channel materials strained-Ge and strained-GeSn in order to achieve high I_{ON}. However, the band gap of both Ge and GeSn is much smaller than that of Si and this may cause excessive drain band-to-band tunneling (BTBT) leakage. Furthermore, stress-induced band gap shrinkage in Ge and GeSn exacerbates this problem.

For the fin dimensions in the 7 nm technology node, strong quantum confinement effect in the channel causes an increase in the effective channel band gap E_G. Here E_G is defined as the energy difference between lowest conduction sub-band and highest valence sub-band. **Figure 5.11** shows the dependence of E_G on channel stress and the fin width. At a channel stress of 1GPa and 6 nm wide fin, a net increase

in E_G as compared with unstrained, bulk material is observed. This increase in E_G is essential in reducing the BTBT leakage.

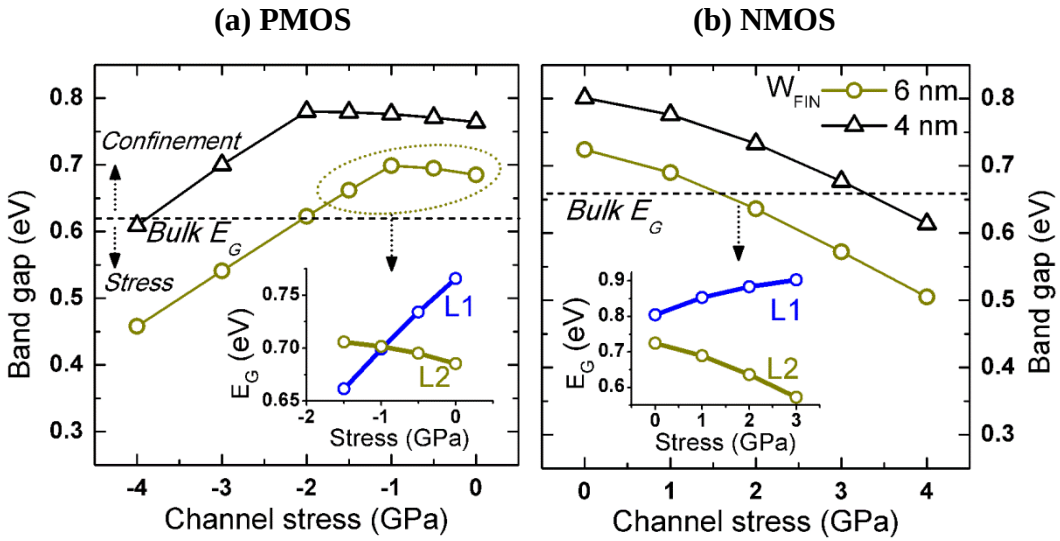


Figure 5.11 Effect of channel stress and fin width (W_{FIN}) on channel band gap (E_G) for **(a)** PMOS and **(b)** NMOS. Band gap of unstrained, bulk material is shown as 'Bulk E_G'. Insets show the effect of confinement, stress on L_1, L_2 splitting for a 6 nm wide fin.

Note that quantum confinement and channel stress have opposite effect on E_G. The increase in E_G due to confinement partly offsets the stress-induced reduction in the E_G. There also exists an interesting interplay between stress and confinement creating some subtle differences in the stress dependence of E_G for PMOS and NMOS. Recall that the PMOS channel material: GeSn (4% Sn) is under compressive strain, whereas tensile-strained Ge forms the NMOS channel. As shown previously in **Figure 5.9**, tensile stress raises the energy of the L_1 valleys above that of the L_2 valleys ($E_{L1} - E_{L2} > 0$). Naturally, compressive stress has an opposite effect, resulting in E_{L1}-$E_{L2} < 0$.

Quantum confinement splits each energy band into multiple sub-bands and the extent to which a particular energy band is affected by confinement depends on its confinement effective mass (m_{conf}). The increase in sub-band energy due to confinement is inversely proportional to m_{conf}. The L_2 valleys have higher confinement effective mass (m_{conf}) than the L_1 valleys (**Figure 5.8c**). Consequently, quantum confinement is responsible for raising the energy the first L_1 valley sub-band above that of the first L_2 valley sub-band (E_{L1}-E_{L2} > 0). The combined effect of stress and confinement on L_1 and L_2 valleys is shown in the insets of **Figure 5.11a, b**. For PMOS, the competing effect of compressive stress and confinement on the L_1, L_2 energy separation causes an initial increase then decrease in E_G as the stress is increased. In case of NMOS, tensile stress and confinement have a similar effect on L_1, L_2 energy separation, causing a monotonic decrease in E_G with increase in tensile stress. For both PMOS and NMOS, there is a net reduction in E_G as compared with the 'Bulk E_G' at large stress levels – eroding the increase in E_G due to confinement. This brings out yet another interesting trade-off in the FinFET design. As shown previously in **Figure 5.10**, CMOS I_{ON} is an increasing function of the channel stress. However, an unchecked increase in channel stress can lead to a significant reduction in E_G and a corresponding increase in I_{OFF}.

The fin design rules enable good short channel effects (SCE) control as indicated by the I_D-V_G characteristics shown in **Figure 5.12**. The BTBT-limited I_{OFF} stays below the ITRS requirement for both high performance (100 nA/μm) and low standby power (10 nA/μm) technology at a supply voltage of 0.7 V. Continued gate length scaling beyond 7 nm technology node entails further reduction in fin width in

order to ensure good SCE. The reduction in fin width results in an enhancement of the confinement effect and an increase in E_G as shown in **Figure 5.11.** This provides the additional E_G bandwidth for incorporating larger stress in the channel, boosting I_{ON} without increasing I_{OFF}. As shown in **Figure 5.12** reducing the fin width from 6 nm to 4 nm results in approximately an order of magnitude reduction in I_{OFF}. Thus, the design proposed here illuminates a clear path for continued technology scaling.

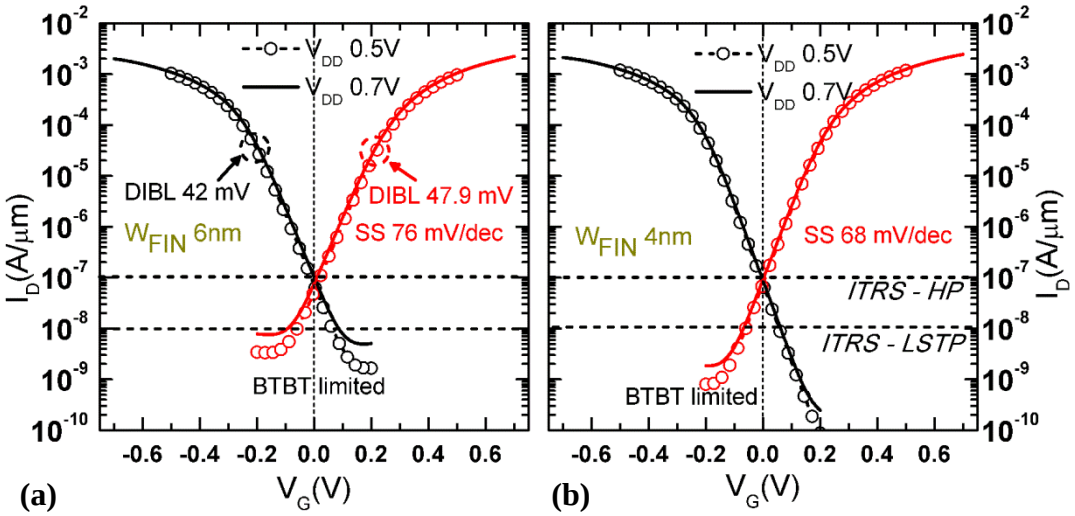


Figure 5.12 Calculated I_D-V_G characteristics of 7 nm FinFET CMOS with **(a)** W_{FIN} = 6 nm and (b) W_{FIN} = 4nm. Sentaurus sdevice parameters for BTBT taken from[**84**]. Channel stress set to ± 1GPa.

5.3.3 Options for S/D and SRB engineering

Several options exist for selecting the S/D stressor material and SRB to individually tune the channel stress in p and n MOSFETs. As shown in **Figure 5.13a**, for a given SRB, the stress in NMOS channel can be adjusted by changing the Si content in the S/D. Similarly, stress in the PMOS channel is a function of the %Sn in the GeSn S/D. Analogously, changing the lattice constant of the SRB provides another

important knob for tuning the stress levels in the channel. This enhanced engineering flexibility is a salient feature of the CMOS design methodology adopted here. Note that using the approach outlined in **Figure 5.13**, channel stress as large as ±4 GPa is also achievable.

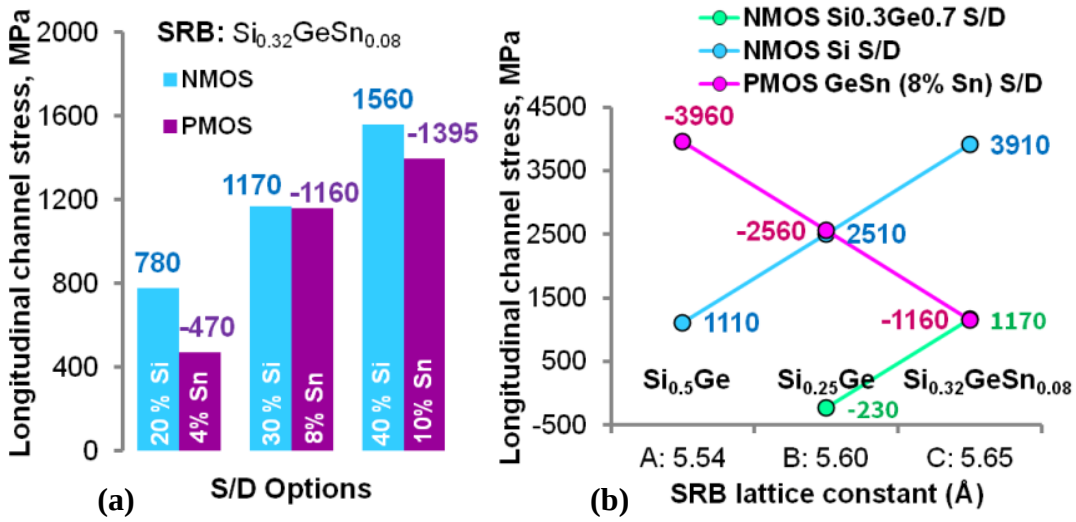


Figure 5.13 Different options for tuning the channel stress: **(a)** Si content in NMOS S/D stressor, Sn content in PMOS S/D stressor **(b)** Lattice constant of the common SRB. Channel material kept invariant: GeSn (4% Sn) (PMOS) and Ge (NMOS), 7 nm design rules.

5.4 Summary

Band gap, stress engineering using group IV materials - Si, Ge and Sn was employed to design a FinFET CMOS solution for the 7 nm technology node and beyond. Through the use of a common buffer layer for p and n MOSFETs and appropriate S/D stressors, the proposed design was shown to achieve performance benefits over strained-Si, meet the I_{OFF} requirements and provide a path for further technology scaling. In the proposed design, GeSn was used as the channel material for

PMOS devices. As already demonstrated in Chapter 4, compressively strained GeSn is a promising candidate material for PMOS channel and shows improvement in hole mobility as compared with unstrained Ge. For nMOSFETs, Ge FinFET with <110> sidewall was shown to deliver the ideal combination of high density of states and low transport effective mass for electrons (or equivalently, high electron mobility). One of the main challenges involved in realizing NMOS has been the prohibitively large density of trap states at the high-κ/ Ge interface. The novel ozone oxidation method presented in Chapter 4 was shown to be an attractive solution for overcoming this problem, thereby enabling strained-Ge for nMOSFET applications.

Chapter 6

Novel Processing Solutions: Selective Etch of Ge over GeSn

This chapter presents a novel etch chemistry that enables highly selective dry etching of Ge over GeSn. Mechanisms responsible for the observed selectivity are investigated in detail. Starting with high-quality, defect-free GeSn thin films grown pseudomorphically on Ge virtual substrate, the etch process is applied to selectively remove the stress-inducing Ge buffer layer and achieve strain-free, direct band gap $Ge_{0.92}Sn_{0.08}$. The selective etch process is also employed for fabrication of GeSn nanowires and synthesis of Ge-on-insulator and GeSn-on-insulator substrates.

6.1 Background

As discussed in previous chapters, the large lattice mismatch between Ge and Sn (~15%) and the low equilibrium solid solubility of Sn in Ge of less than 1% introduces formidable challenges in growth of defect-free $Ge_{1-x}Sn_x$ with even a few atomic % of substitutional Sn. Furthermore, growth and subsequent processing of $Ge_{1-x}Sn_x$ is further complicated by the tendency of Sn to form bulk and surface precipitates of metallic β-Sn when subjected to a thermal budget in excess of 400 ºC-500 ºC, the

precise upper bound on the thermal budget being dependent upon the composition of the alloy. In the case of heteroepitaxy of Ge on Si, misfit dislocations arising due to the 4% lattice mismatch between Ge and Si are confined close to the Ge/Si interface during a high-temperature (850 ºC) hydrogen anneal step in the growth process, resulting in a low defect density in the top Ge region. The thermal budget constraint and the high lattice mismatch of $Ge_{1-x}Sn_x$ with Si prevent the transferability of this growth method to $Ge_{1-x}Sn_x$ heteroepitaxy on Si. Therefore, the state-of-the-art in growth of high quality, low defect density $Ge_{1-x}Sn_x$ thin films relies on the use of a strain-relaxed Ge virtual substrate (buffer layer) as a template for low-temperature $Ge_{1-x}Sn_x$ epitaxy. As shown in chapter 4, $Ge_{1-x}Sn_x$ grown on Ge buffer layers (or Ge substrates) has been the preferred platform for demonstration of early MOSFET devices using $Ge_{1-x}Sn_x$ as a channel material.

Band structure calculations of strained GeSn presented in chapter 2 reveals that the compressive strain in $Ge_{1-x}Sn_x$ grown pseudomorphically on Ge works to negate the effect of alloying Sn with Ge. As a result, compressively strained epitaxial $Ge_{1-x}Sn_x$ thin films show an indirect band gap. A possible technique to overcome the compression in $Ge_{1-x}Sn_x$ thin films is through the selective removal of the stress-inducing Ge buffer layer. Such a method, if feasible, can allow realization of strain-free, direct band gap $Ge_{1-x}Sn_x$ without sacrificing the high material quality of the $Ge_{1-x}Sn_x$ layers grown epitaxially on Ge virtual substrates.

Here, this possibility is explored in detail and a novel semiconductor fabrication process that achieves extremely high etch selectivity between Ge and Ge_{1-}

$_xSn_x$ is presented. The etch recipe developed etches Ge at a rate several orders of magnitude higher than $Ge_{1-x}Sn_x$. The chemistry responsible for the observed etch selectivity is investigated in detail and process parameters for the selective dry etch are carefully chosen in order to minimize any possible damage to the $Ge_{1-x}Sn_x$ thin films during the selective etch process. Such a unique process capability can facilitate fabrication of $Ge_{1-x}Sn_x$ based nanostructures for a range of MOSFET, Si-compatible photonics and microelectro-mechanical (MEMS) device applications.

6.2 Selective etch between GeSn and Ge

6.2.1 Sample preparation

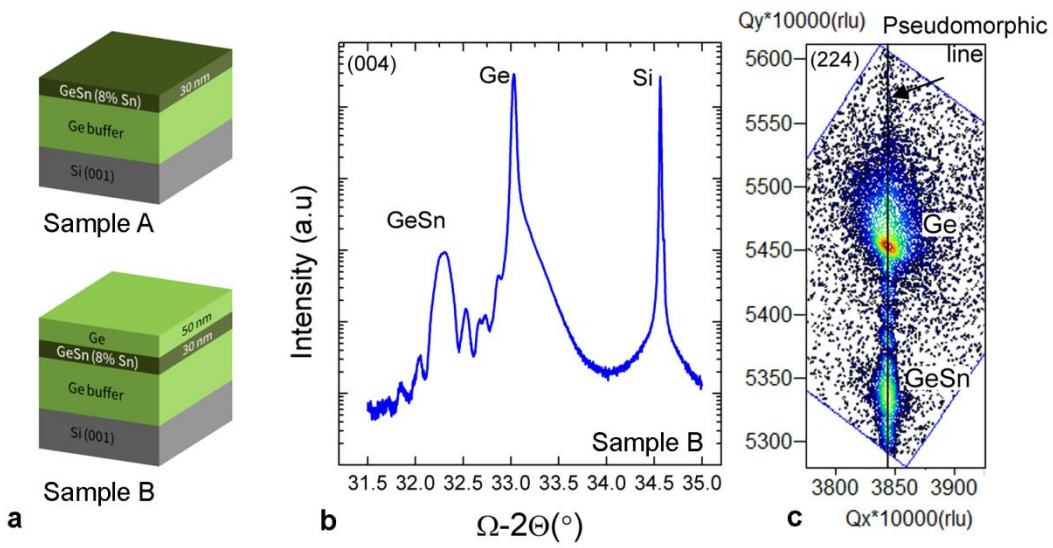


Figure 6.1 (a) Material stacks used in the investigation of the selective etch process. **(b)** High resolution (004) XRD scan of sample B. **(c)** 2D reciprocal space mapping of sample B showing Ge and GeSn peaks. GeSn is pseudomorphic to Ge and hence under compressive strain.

Ge and $Ge_{1-x}Sn_x$ layers are grown using an Applied Materials' Centura CVD reactor. A strain-relaxed Ge buffer layer with a targeted thickness of 4 μm grown on (001) oriented Si substrate forms the starting point for further $Ge_{1-x}Sn_x$ and Ge epitaxy. A 30 nm thick layer of $Ge_{0.92}Sn_{0.08}$[4] is grown epitaxially on the Ge buffer layer using digermane (Ge_2H_6), tin tetrachloride ($SnCl_4$) as CVD precursors at a growth temperature of 320 ºC (sample A). In another set of samples, an additional 50 nm thick Ge is grown on top of the GeSn layer (sample B). The growth temperature during Ge epitaxy on GeSn is also kept below 350 ºC. The low temperature during GeSn and Ge epitaxy minimizes Sn diffusion and ensures sharp material interface between GeSn and Ge. A schematic of the material stacks used in this work is shown in **Figure 6.1a**.

The (004) XRD scan for sample B is shown in **Figure 6.1b**. The presence of well-defined Pendellösung interference fringes attest to the abruptness of the GeSn/Ge interface and the high quality of the epitaxial layers. The out-of-plane lattice constant of the Ge and GeSn layers is estimated to be 5.6509 Å and 5.7708 Å, respectively. As reported previously in [**70**], CVD-grown Ge on Si is slightly tensile-strained due to the thermal mismatch between Ge and Si. Here, the residual strain in the Ge buffer layer is biaxial tensile and calculated to be 0.168%. Because of the larger lattice constant of $Ge_{1-x}Sn_x$ than Ge, thin epitaxial layers of $Ge_{1-x}Sn_x$ grown pseudomorphic to Ge are under compressive strain. This is confirmed by the (224) asymmetric 2D RSM shown in **Figure 6.1c**. Both Ge and GeSn peaks lie along the same in-plane reciprocal lattice vector indicating that the thin GeSn layer is fully strained with respect to the

[4] In this chapter, $Ge_{0.92}Sn_{0.08}$ is abbreviated as GeSn

underlying Ge buffer. The biaxial compressive strain in the GeSn layer is calculated to be 1.07% with respect to unstrained GeSn.

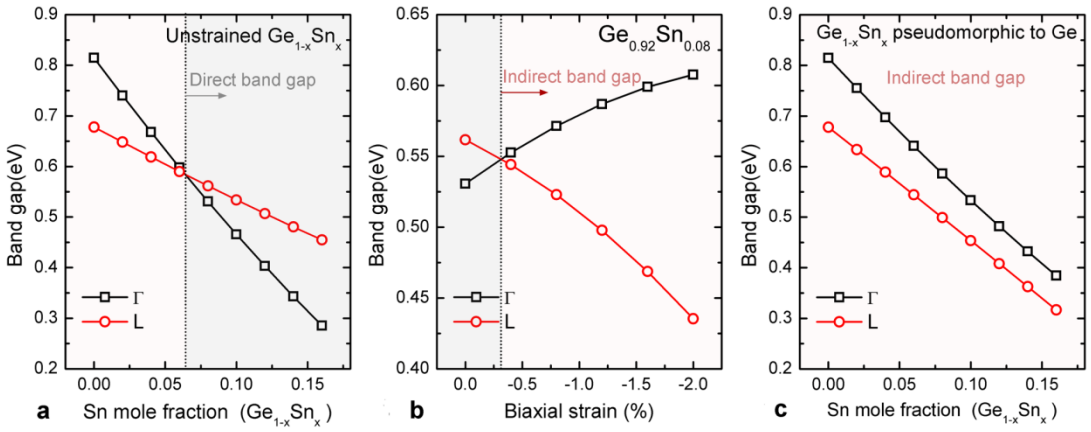


Figure 6.2 (a) Dependence of direct (Γ) and indirect (L) energy band gap in unstrained $Ge_{1-x}Sn_x$ on alloy Sn composition. **(b)** Γ and L energy gaps in $Ge_{0.92}Sn_{0.08}$ as a function of in-plane biaxial compressive strain. For compressive strain in excess of 0.32%, $Ge_{0.92}Sn_{0.08}$ is expected to be indirect band gap. **(c)** If $Ge_{1-x}Sn_x$ is grown lattice matched to Ge, compressive strain in $Ge_{1-x}Sn_x$ increases with Sn% offsetting the effect of Sn alloying. $Ge_{1-x}Sn_x$ pseudomorphic to Ge always remains indirect gap even for Sn composition as large as 16%. Band gaps are calculates using the method described in section 2.3.

It is instructive at this point to revisit the effect of biaxial compression on the electronic properties of GeSn. The electronic band structure of $Ge_{1-x}Sn_x$ is calculated using the alloy-disorder-corrected empirical pseudopotentials described in Chapter 2. For unstrained $Ge_{1-x}Sn_x$, an increase in the Sn mole fraction results in a reduction of the energy separation between the indirect (L) and the direct (Γ) conduction band

minima as shown in **Figure 6.2a**. The indirect to direct band gap transition is predicted to occur at 6.5% Sn. On the contrary, biaxial compressive strain increases the energy separation between the L and Γ conduction band valleys as shown in **Figure 6.2b**. In the case of $Ge_{1-x}Sn_x$ grown lattice-matched to Ge, an increase in the Sn mole fraction *x* is accompanied by a proportionate increase in the biaxial compressive strain in the $Ge_{1-x}Sn_x$ layer. Consequently, the reduction in the L-Γ energy separation obtained by Sn alloying is offset almost completely by the compressive strain arising due to growth of $Ge_{1-x}Sn_x$ on Ge substrate (**Figure 6.2c**). As a result, no indirect to direct band gap transition is expected in GeSn thin films pseudomorphic to Ge. Nevertheless, the GeSn samples used in this work contain substitutional Sn in excess of the minimum needed for inducing direct band gap and release of the compressive strain in these GeSn films is expected to result in a direct band gap material.

6.2.2 Selective etch recipe

Previously, Cheng et al. [**85**], proposed a hydrogen peroxide (H_2O_2) based wet etch for selective etch between Ge and $Ge_{1-x}Sn_x$. However, the H_2O_2 based wet etch was shown to achieve a maximum selectivity of Ge over $Ge_{1-x}Sn_x$ of only 8:1. Here, the selective etch between Ge and GeSn is realized through dry etching in a CF_4 (Freon-14/ tetrafluoromethane) RF plasma. Dry etching is carried out in a capacitively coupled parallel plate plasma etcher with the substrate placed on a grounded electrode. It is observed that CF_4 plasma rapidly etches Ge without any apparent impact on GeSn. For further examination of the selective etch process, disks with varying radii are patterned on Sample B using contact photolithography. Wet etching using a

solution comprising of H_3PO_4:CH_3COOH:HNO_3:H_2O in weight ratio of 72:3:3:22 [5] is used to transfer the photoresist pattern into the Ge and GeSn layers as shown in **Figure 6.3a**. This solution etches Ge and GeSn at rates of 11 nm/min and 4 nm/min, respectively.

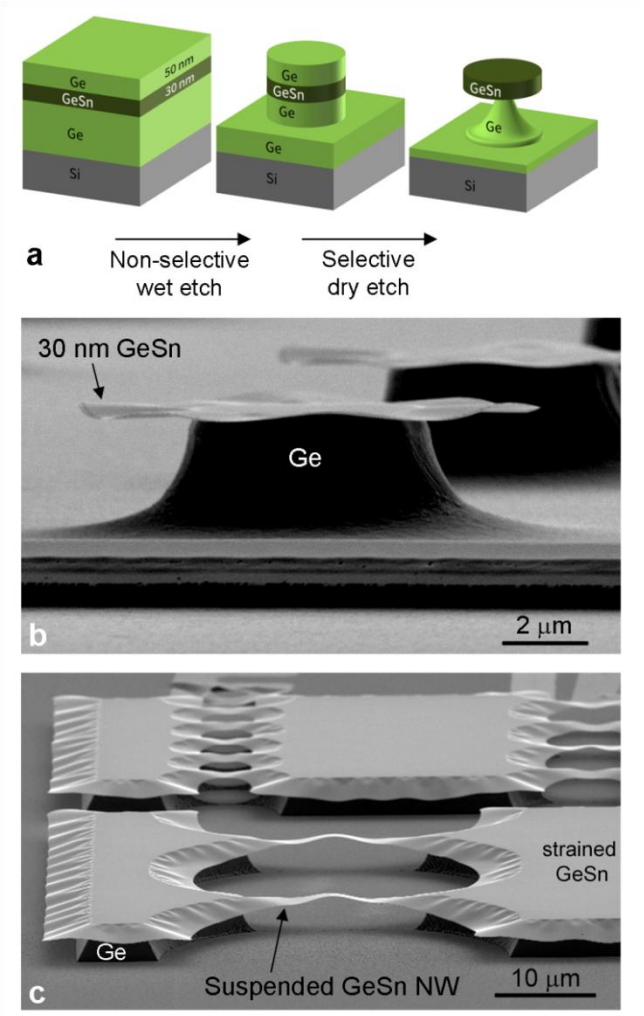


Figure 6.3 (a) Key steps in the process flow for fabrication of GeSn undercut structures on sample B. **(b)** SEM images of GeSn microdisks fabricated on sample B using the process flow of **(a)**. Note that the GeSn layer is only 30 nm thick. **(c)** SEM

[5] Commercially available as an etchant for aluminum

image of suspended GeSn nanowires. Even though the length of the suspended region is greater than 15um, the wires do not collapse onto the substrate. These SEM images prove the high resistance of GeSn to CF_4 plasma etching.

Subsequent CF_4 plasma etching results in removal of Ge on the top and bottom of GeSn, forming partially suspended GeSn microdisk structures (**Figure 6.3b**). The undercut achieved is greater than 2 μm while keeping the thin GeSn layer intact, affirming the high etch selectivity of CF_4 plasma etch. Since the GeSn layer is under a significant compressive strain, release of the stress-inducing Ge buffer layer causes the GeSn layer to relax and produce undulations in the unrestrained portion of the disk. Similar process flow is employed to fabricate GeSn nanowires as shown in **Figure 6.3c**. A 30 nm thin GeSn wire is suspended for lengths greater than 15 μm without the wire 'sticking' or collapsing onto the substrate. In addition to the high selectivity, this stiction-free fabrication of suspended structures is one of the salient features of the selective dry etch method. Typically, fabrication of suspended structures using a wet etch results in strong attractive capillary forces to develop between the suspended structure and the substrate as the liquid is removed, pulling the released structure into contact with the substrate. In fact, stiction is known to be one of the main causes of failure in MEMS devices.

In the sections to follow, results of investigation into the underlying etch chemistry are presented, and the effect of the selective etch process on both the surface and bulk properties of the GeSn etch-stop layer are analyzed.

6.2.3 Optimization of the dry etch recipe

Etching in RF plasma typically proceeds through a combined effect of surface chemical reaction due to reactive free-radicals produced in the plasma and physical sputtering due to surface bombardment by energetic ions.

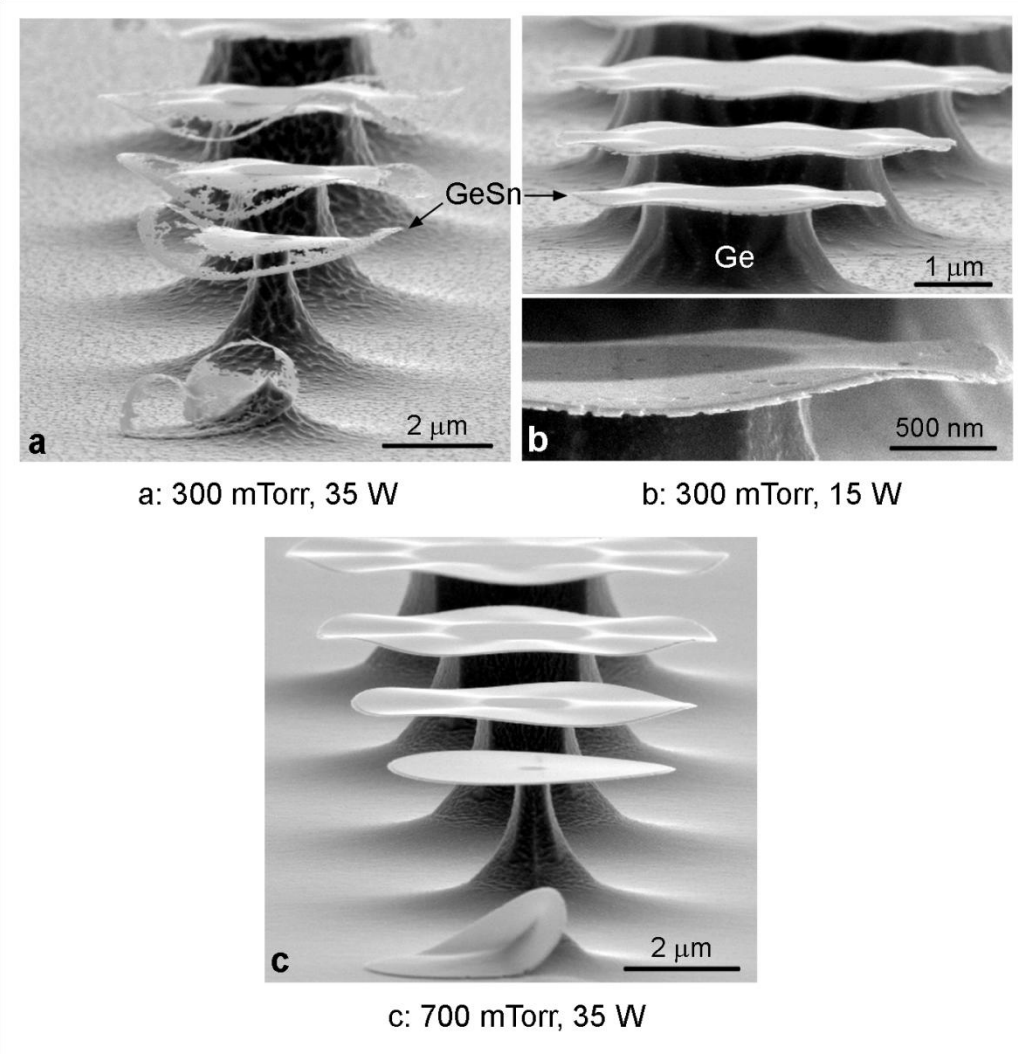


Figure 6.4 Behavior of the GeSn etch-stop layer under different dry etch processing conditions. **a**) Pressure: 300 mTorr, Power: 35 W and total etch time of 300 seconds. **b**) Pressure: 300 mTorr, Power: 15 W and total etch time of 240 seconds. **c**) Pressure: 700 mTorr, Power: 35 W and total etch time of 150 seconds. Ge etch rate follows the

trend c>a>b. Reduction of etching through physical sputtering suppresses the plasma damage to Ge and GeSn surfaces

A reduction in RF power lowers the ion energy and reduces the surface damage caused by ion bombardment. Additionally, etching at a higher gas pressure reduces the mean free path length of the ions. This results in a reduction of the average ion energy and causes the etching to be dominated by chemical reaction at the surface. Although a rigorous optimization of etch process parameters to maximize the etch selectivity between Ge and GeSn is beyond the scope of this work, the guiding principle behind the etch parameters chosen here is to minimize the etching through physical sputtering.

The effect of CF_4 plasma etch parameters such as RF power and gas pressure on the selective etch process is analyzed by means of SEM imaging of GeSn undercut structures fabricated on sample B using the process flow illustrated in **Figure 6.3**. For plasma etch performed at 300 mTorr gas pressure and RF power of 35 W, the undercut GeSn layer suffers severe damage as shown in **Figure 6.4a**. Both Ge and GeSn surfaces show enhanced surface roughness as a result of material removal due to physical sputtering. Reduction of the RF power from 35 W to 15 W (**Figure 6.4b**) during the plasma etch reduces the erosion of GeSn as confirmed by the noticeable reduction in the density of etch pits in the GeSn layer. However, lowering of the RF power is accompanied by a corresponding reduction in the concentration of reactive radicals and results in a slower etch rate. From the SEM image of **Figure 6.4c** it is evident that etching at high gas pressure minimizes the plasma damage to Ge and

GeSn layers. For the three process conditions *a*, *b* and *c* examined above, Ge etch rate follows the order *c*>*a*>*b*.

6.2.4 Photoemission study

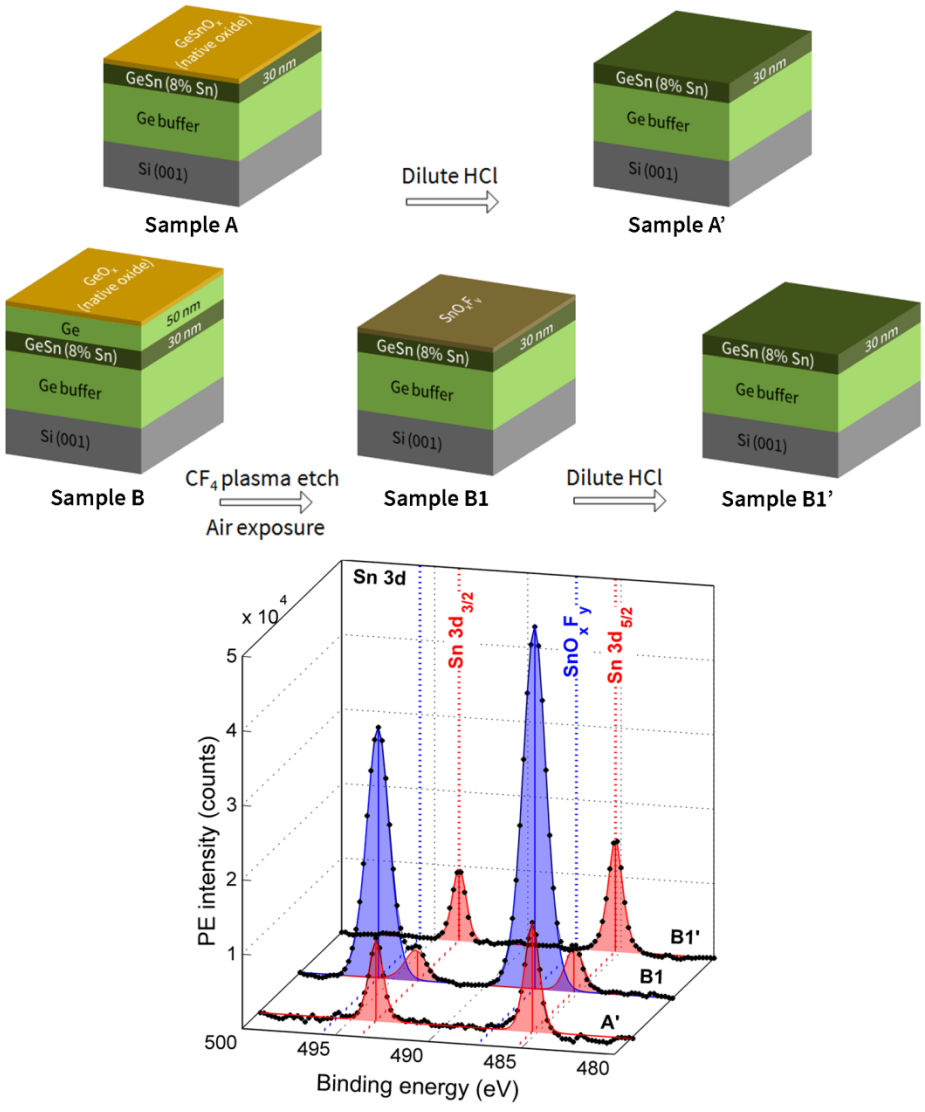


Figure 6.5 Results from photoemission study. Nomenclature adopted is as follows: 1) **A**: reference sample 2) **A**': sample A treated with dilute HCl, 3) **B1**: sample B exposed to CF4 plasma, 4) **B1**': sample B1 treated with dilute HCl. Primed sample labels refer

to samples treated with dilute HCl. **a)** Comparison of Sn 3d spectra for samples A', B1 and B1'.

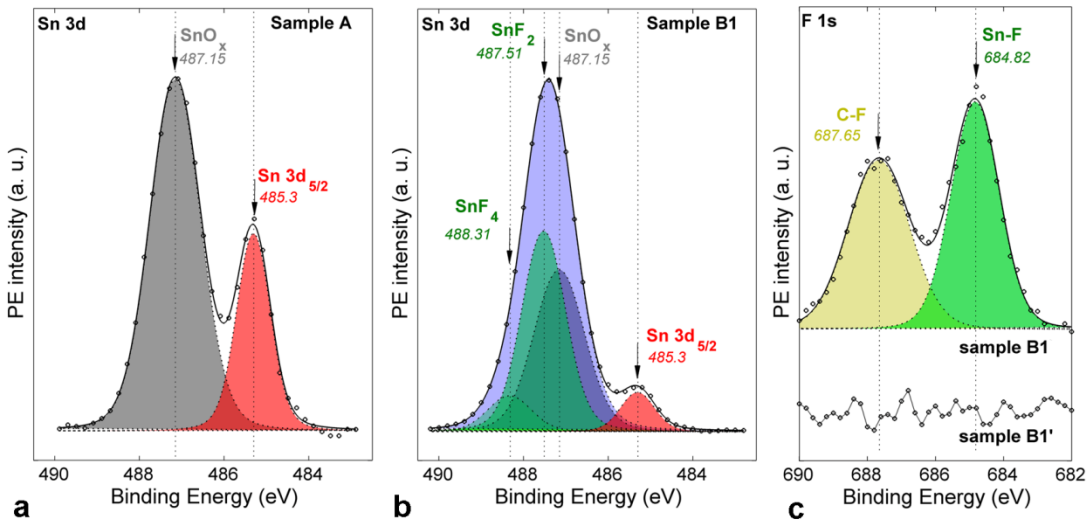


Figure 6.6 (a) Peak fitted Sn 3d spectra of the reference sample (sample A) showing the native SnO_x. **(b)** Peak fitted Sn 3d spectra of sample B1 exposed to CF_4 plasma with peaks corresponding to SnO_x, SnF_2 and SnF_4. **(c)** F1s spectra showing Sn-F, C-F bonds in sample B1. F is not detected in sample B1 after treatment with dilute HCl (sample B1').

Surface chemical analysis using X-ray photoemission spectroscopy (PES) of CF_4 etched GeSn gives further insight into the origins of the etch selectivity. Photoelectron spectra are recorded on a PHI Versaprobe Scanning XPS microprobe using Al k_α (1486.6 eV) excitation. Pass energy for narrow scan windows is set as 23.5 eV with a scan step size of 0.2 eV. PES results presented here are calibrated to C1s binding energy of 284.9 eV. The following samples are prepared and analyzed: **1)** A: reference sample, **2)** A': sample A treated with dilute HCl to remove the native oxide,

3) B1: sample B exposed to CF_4 plasma to etch the top 50 nm Ge and **4)** B1': sample B1 treated with dilute HCl. Here, dilute HCl refers to a solution comprising of equal parts by volume of concentrated HCl (38%) and deionized H_2O. Sample B is etched in CF_4 plasma using the recipe shown in **Figure 6.4c**.

In **Figure 6.5**, the PES spectrum for sample A' shows peaks at 485.3 eV and 493.7 eV corresponding to Sn $3d_{5/2}$ and $3d_{3/2}$ core levels, respectively. The lack of a shoulder at higher binding energy (BE) suggests effective removal of the Sn native oxide using a dilute HCl treatment. In the CF_4 etched sample (sample B1), the Sn 3d core levels are shifted to a higher BE indicating a positive oxidation state of Sn. This shift in BE can be attributed to the formation of surface Sn-F bonds when the GeSn layer in sample B1 is exposed to the CF_4 plasma. Note that the samples suffer an unavoidable air exposure after CF_4 etching and before PES analysis, resulting in oxidation of tin fluoride to form SnO_xF_y.

Peak fitting the Sn $3d_{5/2}$ spectrum of sample B1 is attempted (sample B exposed to CF_4 plasma) in order to further understand the chemical composition of the surface layer. However, the proximity of SnO and SnO_2 binding energies [**86**] complicates the task of achieving unique peak decomposition without making somewhat arbitrary assumptions about the chemical shifts and peak widths. To achieve a reliable peak fitting, the following methodology is adopted: First, the Sn $3d_{5/2}$ spectrum of sample A' (reference sample A treated with dilute HCl to remove the native oxide) is fitted to a Voigt line shape (Gaussian convoluted with Lorentzian) giving Sn $3d_{5/2}$ core level full width half maximum (FWHM) of 0.82 eV. Since the

reference sample (sample A) is not exposed to either CF_4 or dilute HCl, the observed core level shifts in sample A can be attributed solely to the presence of the native SnO_x on the surface. Least squares fitting of the core level shifts in the Sn $3d_{5/2}$ spectrum of the sample A results in the definition of SnO_x peak with a FWHM of 1.29 eV centered at the BE of 487.15 eV, corresponding to a chemical shift of 1.85 eV with respect to the Sn $3d_{5/2}$ core level (**Figure 6.6a**). It is reasonable to assume that the air exposure of sample B1 after CF_4 etching results in formation of Sn-O bonds on the surface that are similar to the Sn-O bonds in the native oxide seen on the reference sample. The peaks fits from the reference sample A are copied to the $3d_{5/2}$ spectrum of sample B1 (**Figure 6.6b**) and adequate peak fitting is obtained only after introduction of two additional peaks with chemical shift of 2.21 eV and 3.01 eV, each with a FWHM of 1.1 eV. To reduce the number of independent fitting parameters, the two peaks are constrained to have the same FWHM. These peaks can be attributed to SnF_2 and SnF_4, and the chemical shift extracted here matches closely with previously reported values for SnF_2 (2.06 eV [**87**], 2.16 eV [**86**], 2.46 eV [**88**]) and SnF_4 (2.96 eV [**86**], 3.26 eV [**88**]). This analysis confirms that SnF_2 and SnF_4 are formed on the sample surface during CF_4 etching. Additionally, the peak observed at a BE of 684.82 eV corresponds to the F1s core level and gives further evidence to the presence of Sn-F bonds after CF_4 etching (see **Figure 6.6c**, sample B1). A broader peak centered at 687.65 eV can be attributed to C-F bonding due to $(CF_2)_n$ polymerization on the surface.

Figure 6.7 shows the Ge 3d and Sn 4d spectra for samples A', B1 and B1' and helps evaluate the surface stoichiometry in terms of Sn/Ge ratio in the surface layer. The Sn/Ge ratio is proportional to the ratio of Sn4d and Ge3d peak areas as shown in

Figure 6.7. The CF_4 etched sample (sample B1) shows a significantly higher Sn/Ge ratio in the surface layer as compared with sample A', suggesting that CF_4 etch depletes the GeSn surface of Ge atoms and forms a Sn-rich surface layer.

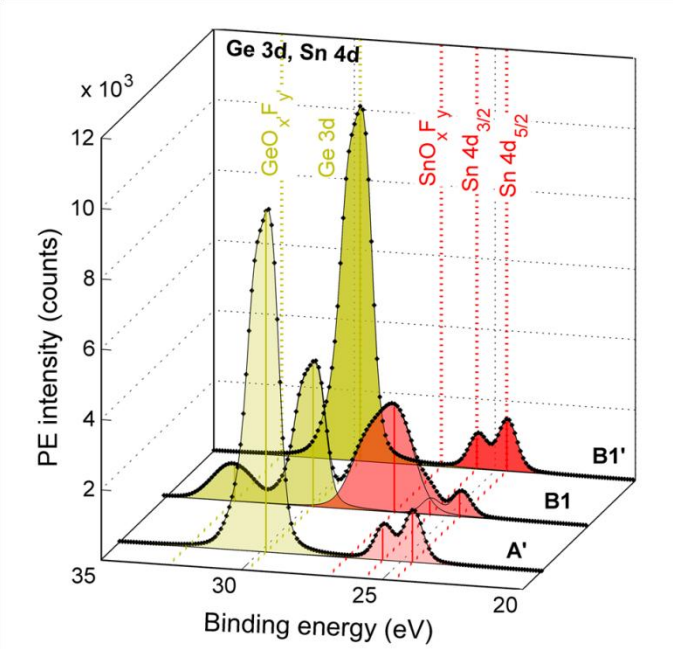


Figure 6.7 Comparison of Ge3d, Sn 4d spectra for samples A', B1 and B1'.

The SnO_xF_y layer formed on the surface of sample B1 after CF_4 etching and subsequent air exposure can be dissolved using a wet chemical treatment with dilute HCl (sample B1'). This is evident from the PES spectra of sample B1' (**Figure 6.5** and **Figure 6.7**) and absence of any detectable F1s signal in sample B1' (see **Figure 6.6c**). In **Figure 6.7**, the samples A' and B1' show a similar Sn/Ge ratio in the surface layer, confirming that the dilute HCl treatment is effective in restoring the stoichiometry of the CF_4 exposed surface to levels expected in the reference sample. The thickness of the surface layer of SnO_xF_y formed on the surface of sample B1 can be determined using

$$t = \lambda \ln\left(I_0 / I\right) \tag{6.1}$$

where λ is the electron inelastic mean free path (IMFP) in the surface layer. Here, I and I_0 represent the integrated Sn $3d_{5/2}$ core level intensity in samples with (sample B1) and without (sample B1') the SnO_xF_y surface layer. For the Sn $3d_{5/2}$ peak and an electron kinetic energy of ~1000 eV, IMFP is approximately 20Å [**89**]. From the Sn $3d_{5/2}$ spectra shown in **Figure 6.5**, the ratio I_0/I is calculated to be equal to 2.25 giving the thickness of the SnO_xF_y layer to be 16 Å.

6.2.5 AFM analysis

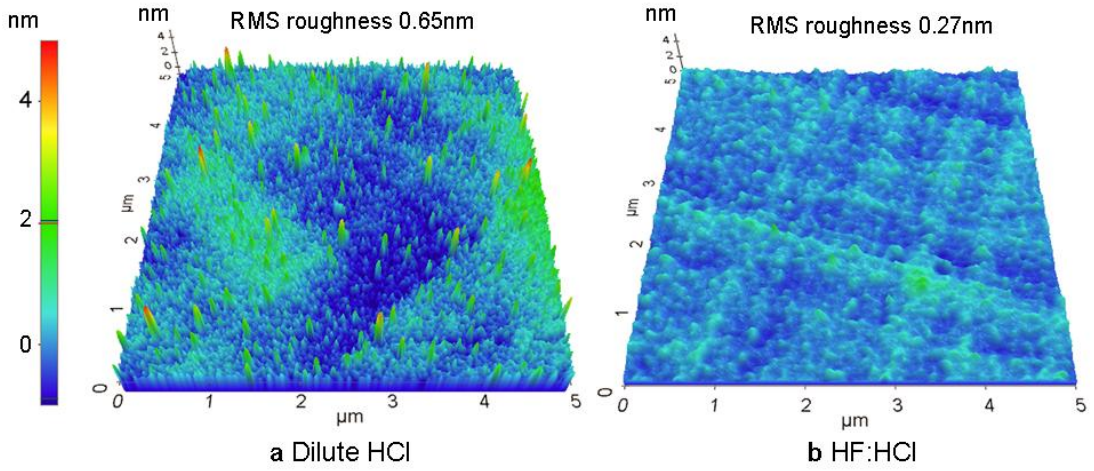


Figure 6.8 AFM analysis of the surface of sample B exposed to CF4 plasma and treated with **a)** dilute HCl and **b)** HF:HCl.

The surface layer of SnO_xF_y can also be removed through a wet chemical treatment with HF:HCl. Here, HF:HCl represents a solution comprising equal parts by volume of concentrated HF(49%) and concentrated HCl(38%). The PES spectra for samples cleaned with HF:HCl do not differ appreciably from the ones shown in

Figure 6.5 for samples treated with dilute HCl (sample B1'). However, AFM analysis of the sample surface after wet chemical treatment brings out the subtle differences between the two methods. **Figure 6.8** compares the 5 μm x 5 μm AFM scan of the sample B1 treated with a) dilute HCl and b) HF:HCl. The reduction in surface roughness after HF:HCl treatment can be attributed to a more effective removal of Sn that accumulates on the surface during the CF_4 etching process. The extremely low RMS surface roughness obtained here is further evidence that the CF_4 dry etch does not damage the GeSn surface.

On the basis of SEM, PES and AFM analyses, the mechanism responsible for the etch selectivity between Ge and $Ge_{1-x}Sn_x$ may now be understood as follows: In a glow discharge, plasma assisted dissociation of CF_4 produces reactive CF_x and F. The F radicals react with germanium atoms spontaneously to form volatile gaseous [**90**] GeF_4, which desorbs from the surface. The presence of Sn atoms in $Ge_{1-x}Sn_x$ results in formation of a thin layer of non volatile tin fluoride (SnF_y) that inhibits further surface reaction. With continued exposure to CF_4 plasma, the GeSn surface becomes Sn-rich as Ge atoms are preferentially removed from the surface.

$$\begin{aligned} \mathrm{Ge} + 4\mathrm{F} &\longrightarrow \mathrm{GeF_4}(g)\uparrow \\ \mathrm{Sn} + 2\mathrm{F} &\longrightarrow \mathrm{SnF_2}(s) \\ \mathrm{Sn} + 4\mathrm{F} &\longrightarrow \mathrm{SnF_4}(s) \end{aligned} \qquad (6.2)$$

During the etching process, plasma ion energy should be minimized to prevent the sputtering of the thin surface passivation layer of tin fluoride and to stop further etching of the underlying $Ge_{1-x}Sn_x$ layer. On the basis of this understanding, it is reasonable to expect the effectiveness of $Ge_{1-x}Sn_x$ as an etch-stop for CF_4 etching to

increase with increasing Sn composition in the alloy. Also, etching in inductively coupled plasma (ICP) systems allows for independent tuning of plasma density and ion energy, unlike the capacitive coupled plasma etching used here. Using ICP etching, it may therefore be possible to further reduce any plasma damage to the GeSn etch-stop layer while achieving a high etch rate for Ge. The dry etch process developed here can also be extended to other group IV materials and their alloy with Sn. Since both Si and Ge are etched in CF_4 plasma due to formation of volatile fluorides [29, 30], it can be speculated that the ternary alloy $Si_yGe_{1-x-y}Sn_x$ possesses similar resistance to CF_4 plasma etch as shown here by GeSn and shows high etch selectivity compared with Si, Ge or Si_yGe_{1-y}.

6.3 Strain-free, direct band gap GeSn

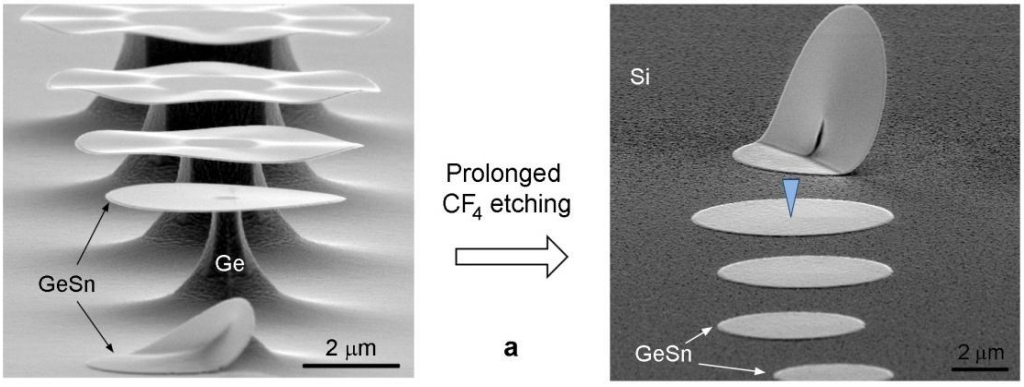


Figure 6.9 Ge buffer underneath the GeSn layer is removed by prolonged etching of the undercut GeSn microdisks in CF_4 plasma. The disks collapse onto the Si substrate and do not show any signs of structural damage. Raman and μPL measurements are performed on the 7 μm disk indicated by the blue arrow.

6.3.1 Raman measurements

In the process flow used to fabricate GeSn microdisks, prolonged etching in CF_4 plasma results in complete removal of the Ge buffer layer causing the GeSn disks to collapse onto the underlying Si substrate as shown in **Figure 6.9**.

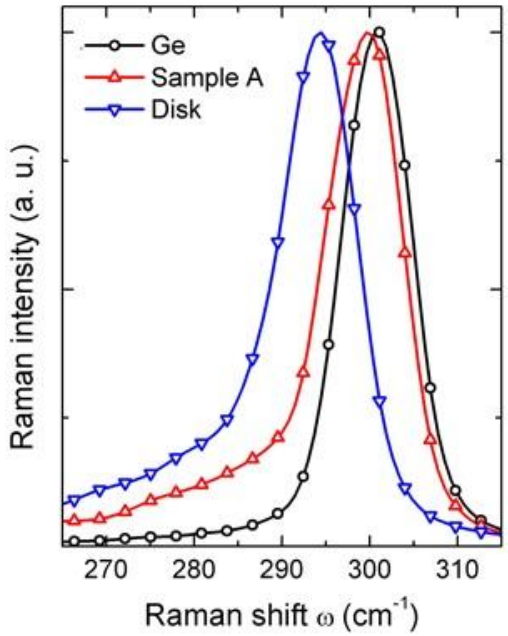


Figure 6.10 Comparison of the Raman spectra of the GeSn disks, sample A and a bulk Ge (001) reference sample.

The disks adhere to the Si substrate only through weak Van der Waals forces and therefore expected to be unstrained. Raman spectroscopy is employed to accurately determine the nature of strain in these disks. Previous Raman studies [**91**,**92**,**93**] have found the frequency of Ge-Ge LO phonon mode in unstrained $Ge_{1-x}Sn_x$ to be linearly dependent on the Sn composition of the alloy:

$$\Delta\omega_{Ge_{1-x}Sn_x} = \omega_{Ge_{1-x}Sn_x} - \omega_{Ge} = ax \tag{6.3}$$

The value of coefficient *a* has been determined to be -83.1 cm^{-1} [**91**], - (82±4) cm^{-1} [**92**] and - (75.4 ± 4.5) cm^{-1} [**93**]. **Figure 6.10** shows the Raman spectrum measured on a 7 μm diameter disk. For the disks, the Raman spectra show an asymmetric peak at a frequency of 294.33 cm^{-1} corresponding to the Ge-Ge LO mode. The Raman spectra as recorded for the reference bulk Ge (001) substrate and the control sample A are also plotted for comparison. The contribution of the Ge buffer to the measured Raman spectra of sample A is expected to be negligible due to the small absorption depth (< 17nm) of 532 nm laser in the GeSn layer. The Ge-Ge LO Raman peak for the disks shows a shift of -6.67 cm^{-1} with respect to bulk Ge. This shift is in close agreement with the value of Raman shift $\Delta\omega$ predicted by equation (6.3) for unstrained $Ge_{1-x}Sn_x$ with 8% Sn, confirming that the disks are strain free. In sample A, the GeSn layer is under compressive strain and the Raman peak is expected to shift to a higher frequency as compared with unstrained GeSn. In such a case, the Raman shift of the Ge-Ge LO mode can be expressed as a function of alloy composition *x* and in-plane biaxial strain ε:

$$\begin{aligned} \Delta\omega^{strained}_{Ge_{1-x}Sn_x} &= \omega^{strained}_{Ge_{1-x}Sn_x} - \omega_{Ge} = ax + b\varepsilon \\ \Delta\omega^{strained}_{Ge_{1-x}Sn_x} &- \Delta\omega_{Ge_{1-x}Sn_x} = b\varepsilon \end{aligned} \tag{6.4}$$

The Raman spectrum for sample A shows a peak at 299.52 cm^{-1} corresponding to a shift of 5.19 cm^{-1} with respect to the strain-free disks. From the XRD measurements shown in **Figure 6.1**, the in-plane biaxial strain ε is calculated as -1.07%, giving a strain induced frequency coefficient of *b* = -485 cm^{-1}. This can be compared with previous experimental results for *b*: - (563 ± 34) cm^{-1} [**92**] and 435 cm^{-}

[1] [**91**]. Also, the FWHM of the Raman peak can be qualitatively correlated to the material quality. In **Figure 6.10** the FWHM for Ge-Ge LO mode in sample A and GeSn disks is found to be similar to the bulk Ge reference sample, indicating a high material quality of GeSn layers both before and after Ge buffer removal.

6.3.2 Micro photoluminescence measurements

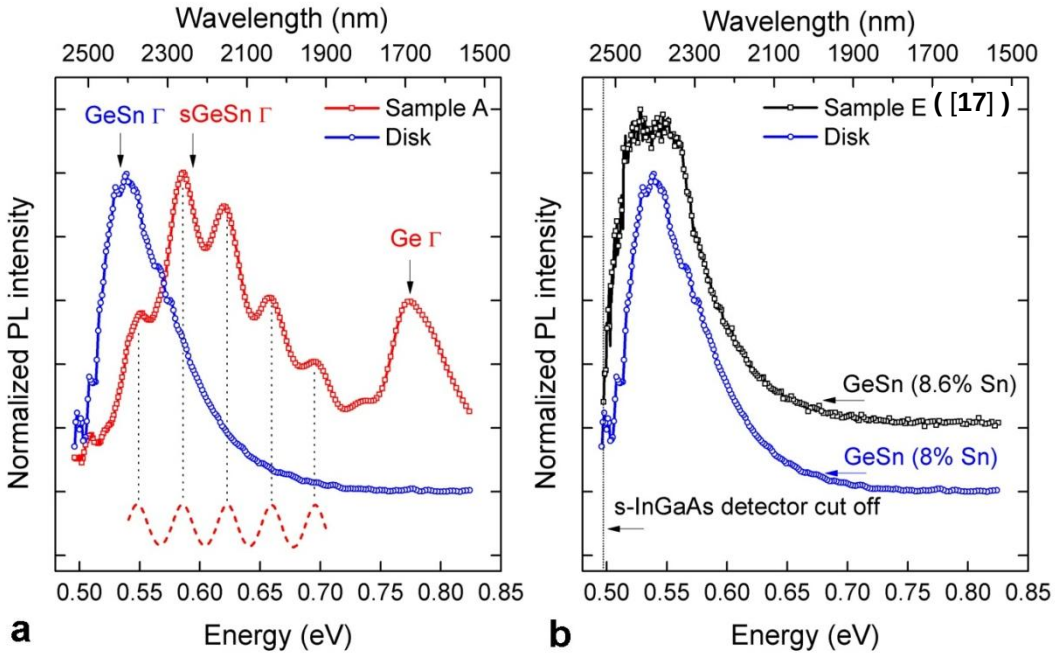


Figure 6.11 (a) Comparison of the μPL spectra of the disk and sample A. The GeSn disks are strain free whereas GeSn in sample A is under compressive strain (sGeSn). **(b)** μPL spectra of the disk is nearly identical to the spectra measured for direct band gap $Ge_{1-x}Sn_x$ (sample E with 8.6% Sn from [**17**]). This confirms that direct band gap is obtained in strain free GeSn disks shown in **Figure 6.9**.

Information regarding the band gap of the strain-free GeSn disks can be extracted through micro photoluminescence measurements (μPL). In **Figure 6.11a**, the

room temperature μPL spectra of sample A and a 7 μm GeSn disk are compared. For sample A, a peak at 0.78 eV corresponding to Ge direct band gap transition is observed. A broader peak at ~0.59 eV can be assigned to band-to-band transitions in the compressively strained GeSn (sGeSn) layer. Since the strain splits the degeneracy of light and heavy hole (LH, HH) valleys, the direct-gap transitions from Γ-LH, Γ-HH and the indirect-gap transitions from L-LH, L-HH are expected to contribute to the peak broadening. Furthermore, the PL spectrum is modulated by the resonances arising due to the Fabry-Perot cavity modes formed between the GeSn/air and Ge/Si interfaces.

In the strain-free disks, a strong and sharp PL peak at 0.54 eV is observed. To first order, the peak PL position serves as a good approximation to the direct band gap energy. The extracted direct band gap of 0.54 eV matches closely with the calculated direct band gap energy of 0.53eV for unstrained GeSn with 8% Sn as shown in **Figure 6.2**. For a more direct comparison, **Figure 6.11b** shows the recorded PL spectrum of 'Sample E' from [**17**]. In this sample, direct band gap $Ge_{1-x}Sn_x$ with 8.6% Sn was grown using low-temperature MBE on lattice-matched InGaAs buffer layer. The MBE-grown sample showed a slight compressive strain (0.22%) causing a broadening of the PL peak and a shift to slightly higher energies. Nevertheless, the close resemblance of the two PL spectra confirms the direct band gap property of the GeSn disks.

6.4 Fabrication of GeSn nanowires

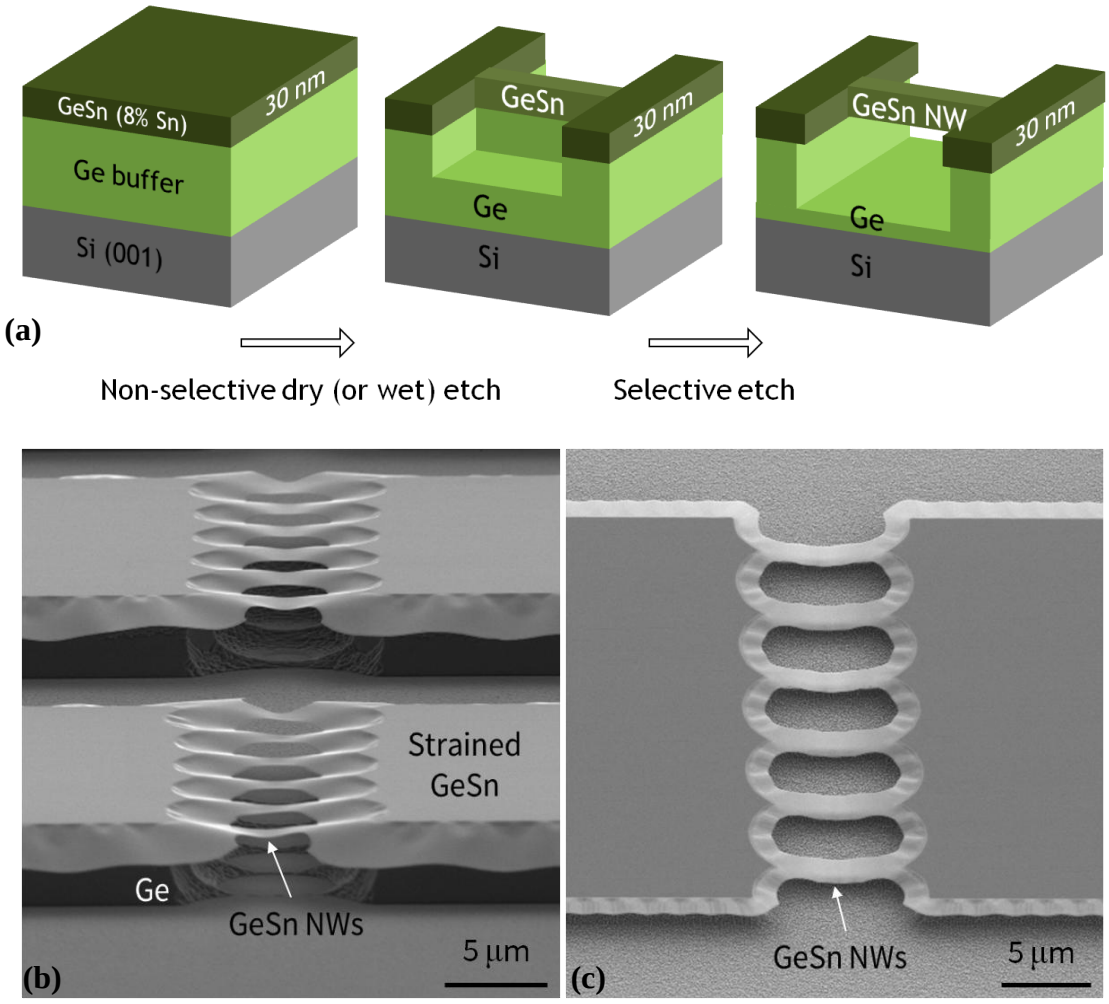


Figure 6.12 (a) Process flow for fabrication of GeSn nanowires (NWs) **(b)** Side-view and **(c)** plan-view of suspended GeSn NWs fabricated on Sample A (**Figure 6.1**).

The process flow used previously to fabricate GeSn microdisk can be extended to enable fabrication of suspended GeSn nanowires. After patterning the GeSn and Ge layers to define a nanowire, the GeSn layer is undercut by removing the underlying Ge buffer layer using the selective etch recipe described above. **Figure 6.12** shows the process flow and the resulting suspended GeSn nanowires. Due to the high selectivity

of etch between Ge and GeSn, the final thickness of the GeSn nanowires is expected to be equal to the initial thickness of the GeSn layer as defined during the epitaxial growth. The nature of strain in the suspended GeSn nanowire is estimated using Raman measurements. **Figure 6.13** shows the normalized Raman spectra mapped along the length of the nanowire. As-patterned, the length of the nanowire is 10 μm. There is ~ 2 μm undercut due to the selective etch, resulting in the total length of the suspended region to be ~ 14μm.

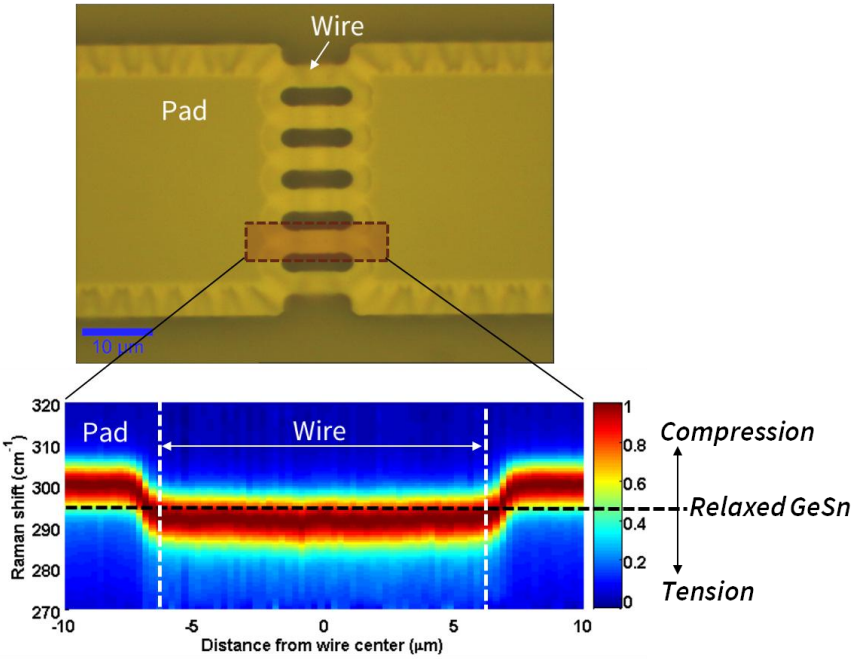


Figure 6.13 Raman spectra mapped along the length of the suspended GeSn nanowire. 'Pad' region is under compressive strain and shows +ve Raman shift compared with relaxed GeSn (8% Sn). Suspended wire shows –ve Raman shift with respect to relaxed GeSn (8% Sn) and hence under tensile strain.

In the 'pad' region, GeSn is compressively strained and shows a Raman peak at the frequency of 299.52 cm^{-1}. As found previously in the case of GeSn disks

(**Figure 6.10**) strain-free, relaxed GeSn with 8% Sn is expected to show peak Raman at frequency of 294.33 cm^{-1}. The suspended portion of the wire shows the Raman peak at 291.4 cm^{-1}. This shift towards smaller frequency as compared with the strain-free GeSn suggests that the suspended portion of the wire is under tensile strain.

The thin nanowires provide an ideal geometry for fabrication of gate-all-around nano-scale MOSFETs using GeSn as the channel material. Furthermore, as discussed previously in chapter 5, the uniaxial tensile strain in these nanowires is expected to enhance the electron mobility.

6.5 Fabrication of germanium-tin-on-insulator substrates

In this section, the selective etch between GeSn and Ge is used to enable fabrication of germanium-on-insulator (GeOI) and germanium-tin-on-insulator (GSOI) substrates. **Figure 6.14** shows the key steps in the process flow. The fabrication process begins with formation of relaxed-Ge buffer on a Si-carrier wafer (donor wafer), followed by deposition of a layer of GeSn and a second layer of Ge using CVD. The top Ge is then passivated using the GeO_x/Al_2O_3 surface passivation scheme detailed in chapter 4. This wafer is directly bonded to a Si handle wafer with thermally grown SiO_2, resulting in the stack shown in **Figure 6.14b**. Prior to bonding, the Si/SiO_2 handle wafer is cleaned using SC-1 solution[6], followed by a 30s clean in 1:50 HF:DI-H_2O solution. After bonding, the composite wafer is furnace-annealed at 300 ºC for 3 hours. There exists a strong adhesion between the SiO_2 and Al_2O_3

[6] SC-1: Standard clean performed with 1:1:5 solution of NH_4OH: H_2O_2: DI-H_2O at 80 ºC for 10 mins.

surfaces due to the following bonding reaction that occurs at the Al_2O_3/SiO_2 interface [**94**]:

$$\text{Al-OH} + \text{Si-OH} \longrightarrow \text{Al-O-Si} + H_2O \qquad (6.5)$$

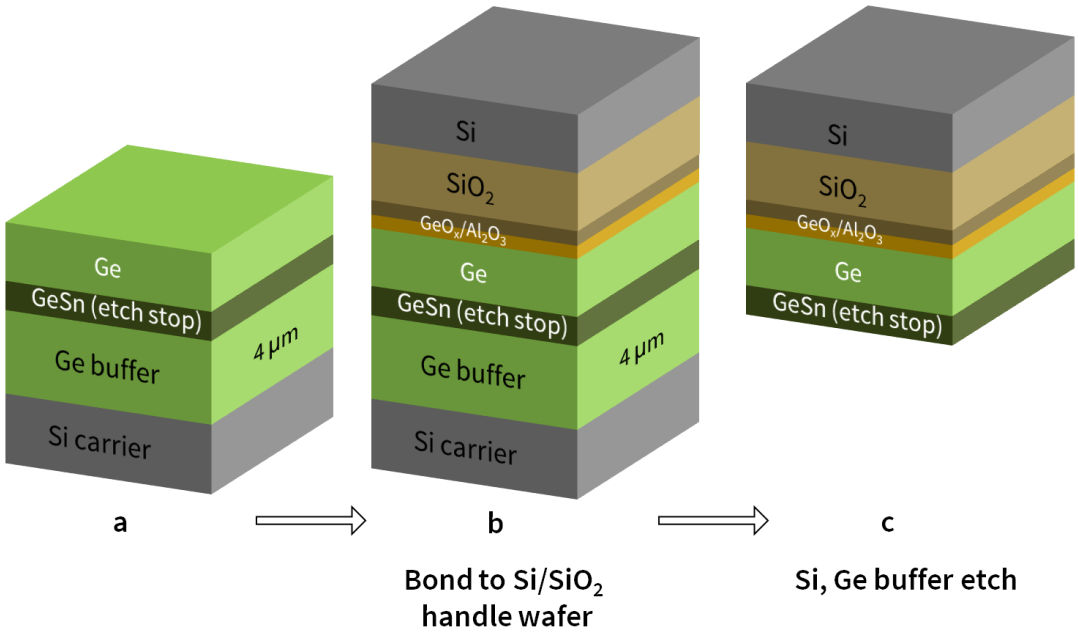


Figure 6.14 Key steps in fabrication of GeOI and GSOI substrates

Next, the Si-carrier (donor wafer) is thinned down to ~30μm using a SF_6-based dry etch. The remaining Si-carrier is etched in tetra-methyl-ammonium-hydroxyl (TMAH) solution. This solution etched Si without affecting the Ge-buffer layer. In principle, the Si donor wafer can be recycled through the use of wafer splitting techniques such as Smart-Cut [**95**] or controlled wafer spalling [**96**]. The Ge-buffer is then thinned using aluminum etchant as done previously in section 6.2.2. The final etch is done using the selective dry etch between Ge and GeSn resulting in the stack shown in **Figure 6.14c**. In the process, the Ge and GeSn layers from the starting wafer are effectively transferred onto the Si/SiO_2 handle wafer.

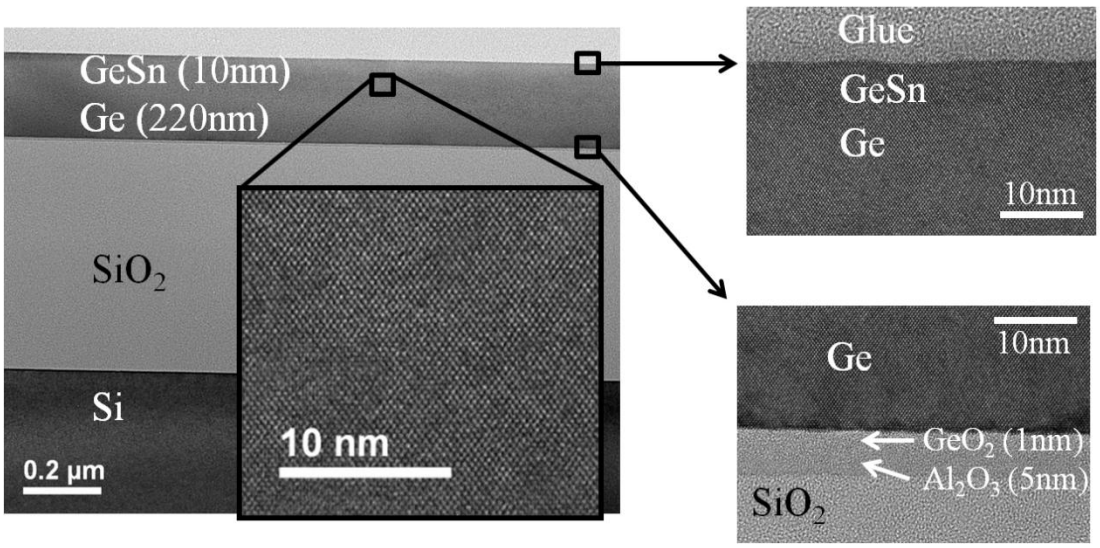


Figure 6.15 TEM cross-sections of **(a)** GSOI with a high resolution inset, **(b)** top and **(c)** bottom interface. Excellent crystal quality, high uniformity of the transferred layers and good interfacial quality are observed.

Figure 6.15 shows the cross-section TEM image of a GSOI substrate fabricated using this process flow. The thickness of the Ge and GeSn layers chosen here is 220 nm and 10 nm, respectively. Note that there is no fundamental constraint on the choice of the material/thickness of the semiconductor layer to be transferred. For simplicity, only a single layer of 220 nm thick Ge is shown here. The present approach is also applicable for transfer of any number of stacked semiconductor layers from the carrier wafer to the Si/SiO_2 handle wafer. From the TEM images, it is clear that the transferred layers retain their high crystal quality. In this particular case, the use of GeO_x helps achieve high quality back interface passivation by reducing the density of electrically active traps at the Ge/Al_2O_3 interface.

Thickness uniformity of the semiconductor layer across the wafer is a key figure of merit for semiconductor-on-insulator substrates. A tight control over the

semiconductor layer thickness variation is necessary in order to reduce the variability in device performance. Due to the high etch selectivity between GeSn and Ge substrates, the thin GeSn layer acts as an effective etch stop during the final etch and results in excellent thickness uniformity of the transferred layers. The thickness uniformity that can be obtained using this method is as good as that of the epitaxial method employed for growth of the GeSn and Ge layers.

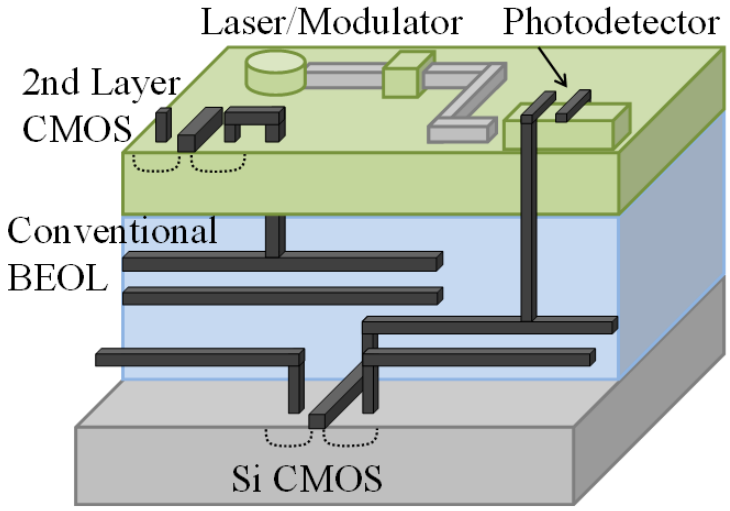


Figure 6.16 GeOI/ GSOI integrated with conventional Si ICs to enable 3-D integration. Ge and/or GeSn as the 2nd layer allows for co-integration of logic and photonic components.

The GSOI substrates fabricated here provide an ideal platform for monolithic 3D integrated circuits (3-D IC). The use of GeSn and Ge overcomes many challenges of monolithic 3D integration, including the need for Si-compatible high-mobility and direct gap materials. Additionally, because of its lower processing temperatures, GeSn and Ge are well suited as material for the stacked layers in heterogeneous 3-D IC, which are expected to achieve higher performance at reduced power and form factors

while allowing for more system functionality. **Figure 6.16** shows a possible application of the GSOI technology. Since the GSOI fabrication is a sub-400 ºC process, it is compatible with the conventional Si back-end-of-the-line (BEOL) processing. In conjunction with mainstream Si-CMOS, the transferred Ge/GeSn layers can then be employed for co-integration of another level of CMOS devices and other Ge and GeSn based photonic components such as a light-emitters (lasers), photo-detectors and modulators.

6.6 Summary

This chapter outlined a dry etch process that allows selective removal of Ge over $Ge_{1-x}Sn_x$ with very high selectivity even for alloy Sn composition as low as 8%. The high etch selectivity was attributed to the formation of thin surface passivation layer of non-volatile SnF_y during the etch process. The dry etch process parameters were tuned to reduce any possible plasma damage to the GeSn layer. Through growth of GeSn thin films on Ge virtual substrates and subsequent removal of the Ge buffer layer using the selective etch process, high-quality, direct band gap GeSn was achieved.

The etch process presented here can facilitate GeSn device fabrication for a wide range of applications. For instance, the GeSn nanowires shown in **Figure 6.12** represent an ideal geometry for fabrication of gate-all-around nanoscale MOSFETs using GeSn as the channel material. The high selectivity of the dry etch process ensures a uniform wire thickness and significantly reduces the process induced variability in device performance. GeSn is shown to be an effective etch stop against

CF_4 plasma etching. This property of GeSn has been capitalized to enable controllable transfer of thin layers of Ge and GeSn to form Ge-on-insulator (Ge-OI) and GeSn-on-insulator (GS-OI) substrates with excellent thickness uniformity. These GS-OI substrates provide an ideal platform for monolithic 3D co-integration of logic and photonic devices. Another salient feature of nanostructure fabrication using the highly selective etch described here is the precise control over the dimensions of the nano-structures, which ensures negligible variability across the entire wafer. Hence, such a semiconductor fabrication process technology is very well suited for high-volume manufacturing.

Chapter 7

Conclusions & Future Work

This thesis undertook the task of exploring GeSn alloys for potential applications in semiconductor device technology. The absence of prior research in the area of GeSn-based devices, allowed this work to adopt a multifaceted approach towards addressing the challenges in developing the GeSn materials technology. Consequently, this thesis spans a fairly diverse range of topics:

In order to facilitate device design and optimization, a model for accurate calculation of the electronic band structure of GeSn was developed. This model was used to evaluate the performance benefits of employing GeSn as a channel for MOSFETs. Concurrently, a sound understanding of the key challenges in GeSn material growth and device processing was developed, and specialized device fabrication processes were designed in order to realize GeSn channel p and n MOSFETs. pMOSFETs that use compressively strained GeSn as channel material were found to show hole mobility enhancements over Ge. An ozone oxidation process was developed for achieving excellent surface passivation of Ge and GeSn.

This knowledge of the electrical properties of GeSn, combined with novel materials growth and processing technique, enabled the design of a FinFET-based

CMOS solution of the 7 nm technology node. Sn, in conjunction with Si and Ge, was shown to be essential in band gap and stress engineering the FinFETs to achieve high on-current, meet the off-current requirements and to continue further device scaling. In addition to the significant changes in the electronic properties of Ge upon alloying with Sn, it was discovered that addition of as little as 8% Sn to Ge dramatically modifies the behavior of the material towards fluorine (F) plasma etching. While Ge was rapidly etched in F plasma, GeSn showed extremely high resistance to F-based plasma etching. This selective etch recipe was used to achieve strain-free direct band gap GeSn, fabricate tensile-strained GeSn nanowires and facilitate fabrication of GeSn-on-insulator substrates. Additionally, the selective etch between Ge and GeSn is foreseen to be of great significance and high impact since it provides a robust technique for fabrication of innovative GeSn-based devices for a wide range of applications such as high-speed transistors for semiconductor logic, Si-compatible photonics and micro-electro-mechanical systems. References [**97**-**107**] are the important publications resulting from this work.

This thesis lays the foundation of further research in Sn-based group IV materials and devices. The direct band gap property of GeSn makes it particularly favorable for tunneling field effect transistors (T-FETs). The method of achieving direct band gap GeSn through selective removal of the Ge buffer layer provides the starting point for fabrication of GeSn T-FETs. Although the focus of this work remained confined to GeSn, exploring the properties and applications of the ternary alloy system – SiGeSn is expected to be a fruitful extension of the ideas and methods presented here.

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