PHYSICS AND TECHNOLOGY OF LOW TEMPERATURE GERMANIUM MOSFETS FOR MONOLITHIC THREE DIMENTIONAL INTEGRATED CIRCUITS

A DISSERTATION

SUBMITTED TO THE DEPARTMENT OF ELECTRICAL ENGINEERING

AND THE COMMITTEE ON GRADUATE STUDIES

OF STANFORD UNIVERSITY

IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF

DOCTOR OF PHILOSOPHY

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June 2009

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Abstract

As the minimum feature size of silicon (Si) CMOS devices shrinks to the nanometer regime, device behavior becomes increasingly complex, due to new physical phenomena at short dimensions and fundamental limitations in material properties are reached. One of the techniques that shows promise to overcome this obstacle is the utilization of monolithic three-dimensional integrated circuits (3D-ICs).

By stacking devices vertically, it is expected that (1) more functionality can fit into a smaller space and (2) the signal delay and power consumption in the interconnect layers will decrease and bandwidth will increase. The major challenge in fabricating monolithic 3D-ICs is the maximum process temperature limit of 400 ºC in the upper layers of CMOS device processing, due to the fact that higher process temperature would destroy the underlying device and interconnect layers.

1. Single crystalline GeOI growth technique at below 360 ºC

First, we have investigated Ni or Au-induced crystallization and lateral crystallization of planar amorphous germanium (α-Ge) on SiO_2 at 360 ºC without the deleterious effects of thermally induced self-nucleation. Subsequently, single crystalline Ge growth has been achieved on SiO_2 by making dimension of α-Ge line smaller than the size of grains formed using Ni and Au-induced lateral crystallization at 360 ºC.

2. Low temperature dopants activation technique in Ge

Second, we have investigated low temperature boron and phosphorus activation in α-Ge using the metal-induced crystallization technique. Eight candidates of metals including Pd, Cu, Ni, Au, Co, Al, Pt, and Ti are used to crystallize α-Ge at low temperatures followed by resistivity measurement, TEM, and XRD analyses, thereby revealing behaviors of the metal-induced dopants activation process where metals react with α-Ge at low temperature. It is found that Co achieves the highest B and P activation ratio in Ge below 360 ^{o}C with slow diffusion rate. The feasibility of low temperature activation technique has been demonstrated for Ge gate electrode in Si P-MOSFET using Schottky Ni (or Co) silicide source/drain.

3. High performance and low temperature Ge CMOS technology

Third, we demonstrate high performance n^{+}/p & p^{+}/n junction diodes and N & P-channel Ge MOSFETs, where Ge is heteroepitaxially grown on a Si substrate at sub 360 ºC and the low temperature gate stack comprises of $Al/Al_2O_3/GeO_2$. Shallow (~100 nm) source/drain junctions with very low series resistivity [5.2×10^{-4} Ω-cm (in

n^+/p junction) and 1.07×10^{-3} Ω-cm (in p^+/n junction) at the lowest point of SRP] and high degree of dopant activation are achieved by Co-induced dopant activation technique. Consequently, high diode and transistor current on/off ratios (~1.1×10^4 & ~1.13×10^3 for N-MOSFETs and ~2.1×10^4 & ~1.09×10^3 for P-MOSFETs) were obtained in these N & P-channel Ge MOSFETs.

These low temperature processes can be utilized to fabricate Ge CMOS devices on upper layers in three-dimensional integrated circuits, where low temperature processing is critical.

Acknowledgements

This dissertation would not have been possible without the help and contributions of many individuals, to whom I am greatly indebt. First of all, I want to express my sincere and deepest gratitude toward my advisor, Prof. Krishna C. Saraswat, for his generous support and insightful guidance throughout the course of my Ph.D research. I especially appreciate his patience, allowing me to take sufficient time to choose a great research topic that eventually became my thesis. It has been a rewarding experience to work with him.

I would like to thank my co-advisor, Prof. Philip Wong, for his kind advice and support. I have learned and benefitted from his vast knowledge and industry research experience at IBM. Despite his busy schedule, he has always given me valuable comments. I want to thank Dr. Pawan Kapur for being both a good mentor and friend. Pawan has provided me with invaluable and unbiased guidance on my research. I also acknowledge the help and guidance offered by Prof. Simon Wong, especially in 3D-ICs project. I am also grateful to Prof. James Harris for agreeing to serve as the chair of my Ph.D dissertation defense committee.

I was very fortunate to interact with Dr. Munehiro Tada from NEC corp., Japan and Dr. Hailin Peng from Prof. Yi Cui group. I would like to thank them both for sharing their broad technical expertise and being my mentors during my Ph.D.

I thank Irene Sweeney and Gail Chun-Creech for their efficient administrative support especially for always getting my PO's and reimbursements in time.

At Stanford, I had the great opportunity to interact with finest scholars in the world. I thank all my colleagues including Dr. Hoon Cho, Dr. Hoyeol Cho, Dr. Jungyup Kim, Dr. Abhijit Pethe, Dr. Ali Okyay, Dr. Tejas Krishnamohan, Hyun-yong, Duygu, Woo-Shik, Dong-Hyun, Kyung Hoae, Gunhan, Raja, Yeul, Shyam, Aneesh, Jason, Arunanshu, Sarves, Crystal, Saroonter, Byungil, Soojin, Hyunjoo, Hyunwoo, Sangbum, Kyeongran, Gaurav, Masaharu, Hopil, Donghun, Erik, Filip, Dan, Jia, Nishant, Yuan, Jialie, and many others.

During my Ph.D course, I have spent a great deal of time in Stanford Nanofabrication Facility (SNF) for my experiments. Without SNF staff's help and their expertise, my Ph.D research results would not have been possible. I thank Cesar, Ed, Elmer, Gary, Jeannie, John, Mahnaz, Mario, Mary, Maurice, Nancy, Peter, Ray, Ted, and Uli.

Without many good friends at Stanford, I would not be able to finish the long and challenging life of becoming a Ph.D. I thank Junyoung, Kwonsoo, Wootae, Ilwoong, Sungyeon, Sanghoon, Taeho, Insun, Youngjae, Sangwon, Jongduk, Jongmin, Hansun, Minjae, Jungho, Sechan, Eunjoon, Wanki, Kwon, Jaeho, Pilsung, Daehyun, and Jinwoo.

There are absolutely no words to express my deepest thanks and love to my wonderful family, my wife (Lin Hur), my two months old son (Ian), and my parents. Their continuous love, sacrifice, support, and encouragement have allowed me to pursue my ambitions.

I dedicate this work to them.

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Chapter 1

Introduction

1.1 Motivation

As the minimum feature size of silicon (Si) CMOS devices shrinks to the nanometer regime, device behavior becomes increasingly complex, due to new physical phenomena at short dimensions and fundamental limitations in material properties are reached. As a result, it is predicted that the scaling speed will become slower than Moore's law in future technology nodes. In addition, the signal delay and power consumption in interconnect layers have become important factors limiting the overall performance of integrated circuits (ICs). One of the techniques that shows promise to overcome this obstacle is the utilization of monolithic three-dimensional integrated circuits (3D-ICs) [1.1]. By stacking devices vertically, it is expected that (1) more functionality can fit into a smaller space and (2) the signal delay and power consumption in the interconnect layers will decrease and the bandwidth will increase. The second argument is based on the fact that the average wire length becomes much shorter in the 3D-ICs, therefore it is plausible that it will result in significantly less signal delay and power consumption, and increase in the bandwidth, ensuring continuation of the Moore's law. In addition, this 3D integration technique also offers two other benefits. First, different functional components such as analog, digital or RF blocks could be combined into a single device [1.2], making SoC (System on a Chip) design a more feasible concept. Second, this 3D integration technique allows large numbers of vertical vias between the layers [1.3], enabling construction of wide bandwidth buses between functional blocks in different layers.

The major challenge in fabricating monolithic 3D-ICs is the maximum process temperature limit of 400 ºC in the upper layers of CMOS device processing, for higher process temperature would destroy the underlying device and interconnect layers. Aluminum (Al) and Copper (Cu) interconnects, being fragile and low dielectric constant (k) materials [1.4-1.5] are very unstable at above 400 ºC. In addition, processes above 400 ºC influence the gate stack (metal gate + high-k gate dielectric) [1.6] and shallow source/drain (S/D) junctions [1.7] of the first level devices in 3D-ICs, altering tightly controlled (or designed) device performance and parameters. Thus, metal induced crystallization (MIC) and metal induced lateral crystallization (MILC) are used in this work with germanium (Ge) to reduce the process temperature to below 400 ºC. Ge, by virtue of its lower melting point (937 ºC) than that of silicon (Si) (1412 ºC), offers lower process temperatures and thus is a highly suitable channel material for monolithic 3D-ICs. On the contrary for Si, the process temperature cannot be reduced to below 500 ºC even with MIC technique [1.8-1.9].

1.2 Thesis organization

Chapter 2 starts with an introduction to 3D-ICs and discusses several previously reported low temperature Ge CMOS processes for monolithic 3D-ICs fabrication. In Chapter 3, theoretical basis for the MIC and MILC processes, a main concept in this dissertation, is explained and experimental data to support the mechanisms is presented. Chapter 4 describes in detail low temperature (≤ 360 ºC) single crystalline germanium on insulator (GeOI) growth technique using the MILC technique. In Chapter 5, metal induced dopant activation (MIDA) process featuring the MIC technique is investigated at a low temperature range between 300 ºC and 450 ºC. The feasibility of MIDA technique is demonstrated for a Ge gate electrode in a Si P-MOSFET using Schottky Ni (or Co) silicide source/drain. Chapter 6 presents high performance N and P-channel Ge MOSFETs fabricated at below 360 ºC with the novel n^+ and p^+ S/D junctions formed by low temperature MIDA process and a metal/high-K dielectric/GeO_2 gate stack. Finally in Chapter 7, the conclusions of this work and recommendations for future work are stated.

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Chapter 2

Realization of monolithic three dimensional integrated circuits (3D-ICs)

There are several types of 3D-ICs differentiated primarily by the degree of vertical interconnectivity. These include 1) package level stacking and connections such as cell-phone memories (limited to peripheral connections), 2) wafer to wafer or die to wafer bonding with through-via holes, and finally 3) monolithic 3D-ICs, which exhibit a bottom-up manufacturing of 3D layers, giving highest (gate-level) vertical interconnectivity potential.

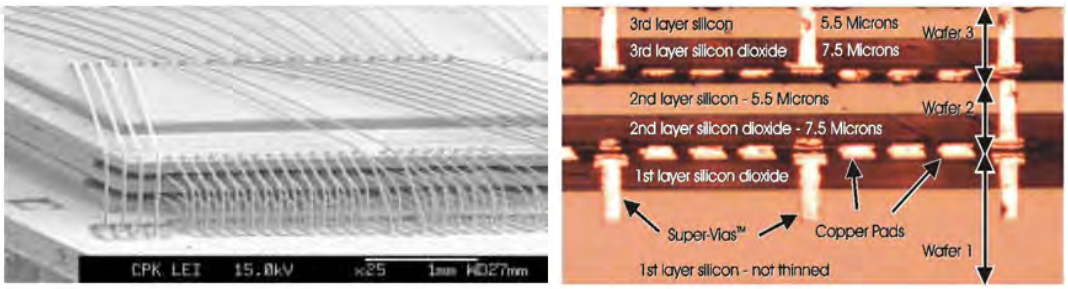

Figure 2.1: (left) 3D packing [2.1] and (right) bonding technology [2.2]

Although monolithic 3D-ICs possess maximum benefits with aspects to speed, power, alignment between layers, and yield [2.3], their fabrication is a challenging feat. It requires low temperature processes preferably under 400 ºC in order to preserve underlying layers. These layers consist of 1) interconnect stacks composed of metals, fragile and porous low dielectric constant (k) materials, and 2) device layers, whose parameters such as junction depths are tightly controlled for performance by limiting the thermal budget. In light of this problem, utilization of Germanium (Ge) as an ideal

substrate for 3D-ICs is being considering as a solution because of its lower melting point than Si, which makes low temperature CMOS processing more feasible.

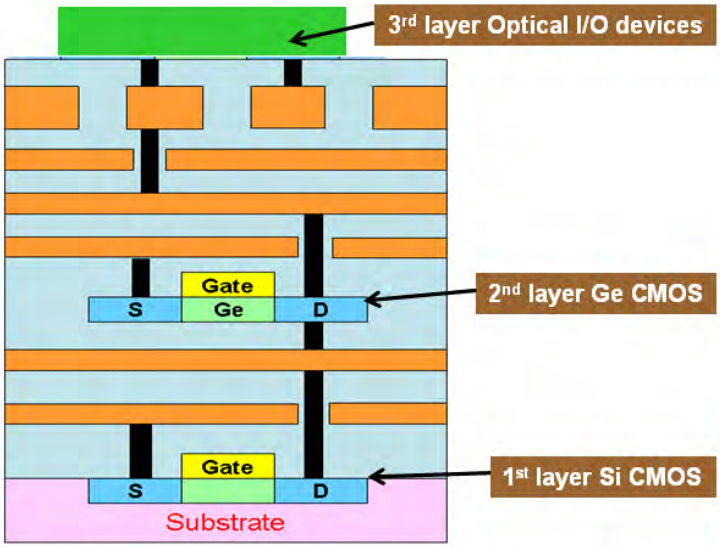

Figure 2.2: Schematic of monolithic 3D-ICs [2.4]

In this chapter, we review some of the current low temperature fabrication approaches to realize Ge MOSFETs for monolithic 3D-ICs in four aspects; (1) channel, (2) source/drain (S/D), (3) gate dielectric for surface passivation, and (4) gate electrode.

2.1 Channel formation

Several techniques are being pursued to obtain germanium on insulator (GeOI), necessary for monolithic 3D-ICs. The most important point, here, is that Ge with imperfect crystal, e.g., polycrystalline structure, degrades transistor performance by 1) reducing the on-current, 2) adversely impacting the subthreshold slope, and 3) increasing leakage current and power dissipation. The adverse impact of grain boundaries on Ge is more severe than Si because of its higher mobility and lower band-gap. Thus, it is imperative to obtain a device-suited single crystalline Ge on silicon dioxide (SiO_2), at a sufficiently low temperature for high performance 3D-ICs. The single crystalline GeOI growth techniques include: rapid melt growth (RMG)

[2.5-2.7] with a continuous wavelength (CW) laser scanning technique [2.8-2.9], fusion bonding process utilizing Smart Cut^{TM} [2.10] and chemical mechanical polishing (CMP) methods [2.11], and metal-induced lateral crystallization (MILC) [2.12-13].

General RMG method employs liquid phase epitaxy (LPE) mechanism and defect blocking technique to make a high quality and ~ 20 μm long single crystalline GeOI structure as shown in Fig. 2.3 and 2.4. In this technique amorphous Ge is deposited on the insulator with a seed window on a Si substrate. The Ge is patterned into stripes and then covered by low-temperature oxide (LTO). The temperature of the wafer is raised up to 940 ºC by rapid thermal annealing (RTA) (melting temperature of Ge : 937 ºC), and the LTO serves as a micro-crucible to hold the liquid Ge. Upon cooling down, liquid phase epitaxy takes place at the a-Ge/c-Si interface and then propagates along the Ge stripe. The defects due to lattice mismatch are necked down near the seed window, and thus the rest of the Ge is high-quality and single-crystalline. This process is compatible with Si-based fabrication with an advantage that the Ge film orientation can be controlled by the Si substrate.

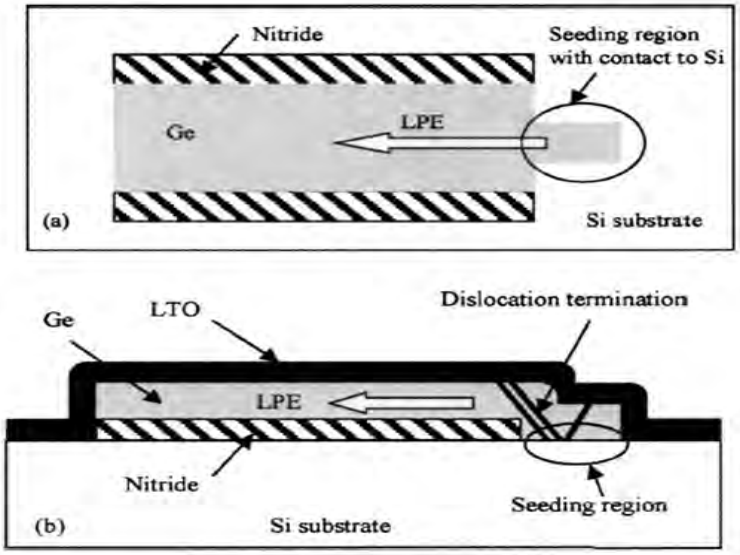

Figure 2.3: (a) Top view and (b) side view of schematics of structures used for Ge RMG process [2.5]

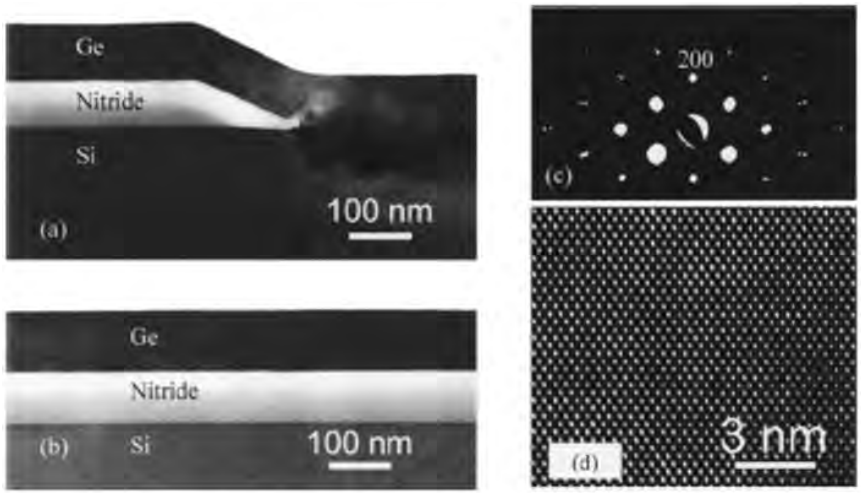

Figure 2.4: Cross sectional TEM images and diffraction pattern taken in GeOI structure formed by the RMG technique [2.5]

However, the RMG method requires high process temperature close to 940 ºC, which is much higher than acceptable for monolithic 3D-ICs application. Therefore, Jia Feng *et al*. [2.14] replaced the RTA step by a CW laser scanning technique (Fig. 2.5) to keep the temperature of bottom interconnect and device layers to below 400 ºC.

After annealing by the scanning CW laser anneal system (frequency-doubled Nd:YAG laser, wavelength = 532 nm, output power = 6 W, beam diameter = 30 um, and scan speed = 20 um/sec), melt growth is guided by the laser over a long distance up to 6 μm and high-quality single crystalline GeOI stripes are obtained. This modified RMG process can be utilized to form Ge channel region of the second layer of devices for monolithic 3D-ICs because the temperature of bottom device and interconnect layers does not exceed 400 ºC while making this GeOI structure.

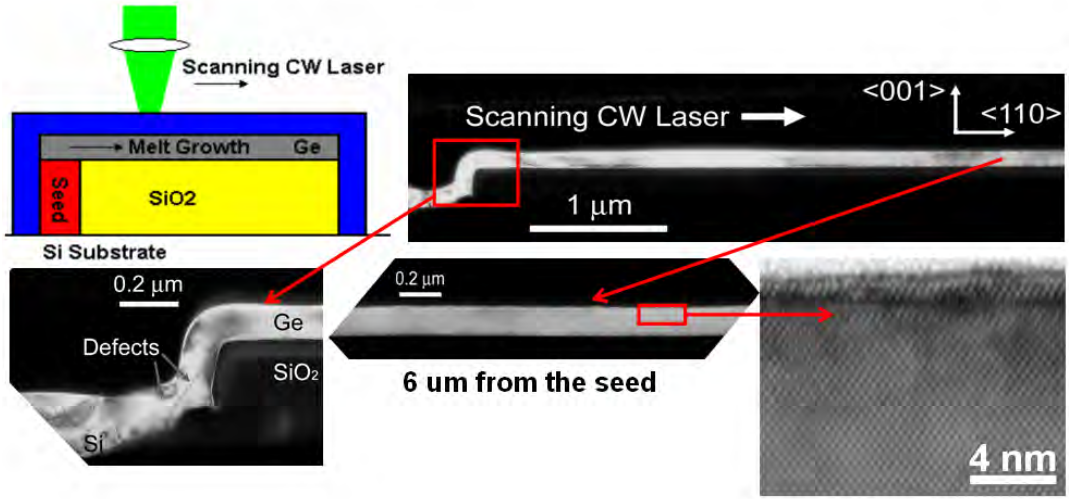

Figure 2.5: Schematic and cross sectional TEM images of GeOI structures formed by the modified RMG process using CW laser scanning technique [2.14]

Another technique used to obtain high quality single crystalline GeOI at below 400 ºC is wafer bonding using CMP and Smart Cut^{TM} methods. Ge is heteroepitaxially grown on Si. This donor wafer is then bonded to another Si wafer having a layer of silicon dioxide (SiO_2) on it. Grinding or CMP and etching methods can be then applied to form the GeOI structure. In such a case, however, one of the two wafers (donor) is completely lost. Ge films with improved quality can be obtained by using Czochralski-grown bulk Ge wafers with zero dislocations instead of heteroepitaxially grown Ge [2.15]. A more efficient way is offered by combining CMP and Smart Cut^{TM} technology [2.11]. The basic process flow includes epitaxial Ge growth on donor Si wafer implanted with hydrogen ion (H^+) which is bonded to acceptor wafer (SiO_2 on Si wafer). After bonding the donor wafer is peeled off at the region where hydrogen was implanted, followed by a CMP step, as shown in Figure 2.6. The final CMP step is necessary to reduce surface roughness occurred near the H^+ implantation layer.

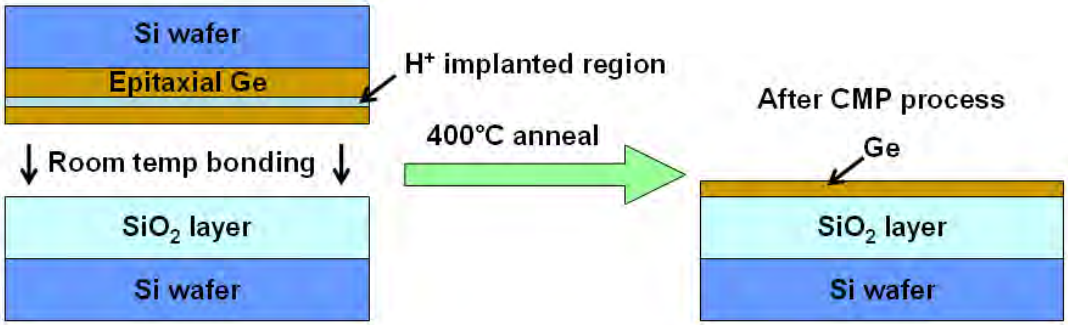

Figure 2.6: Bonding process flow using Smart Cut™ and CMP techniques for GeOI formation

Because this wafer-level GeOI process is performed at around 400 ºC, this technique can be used for monolithic 3D-ICs fabrication.

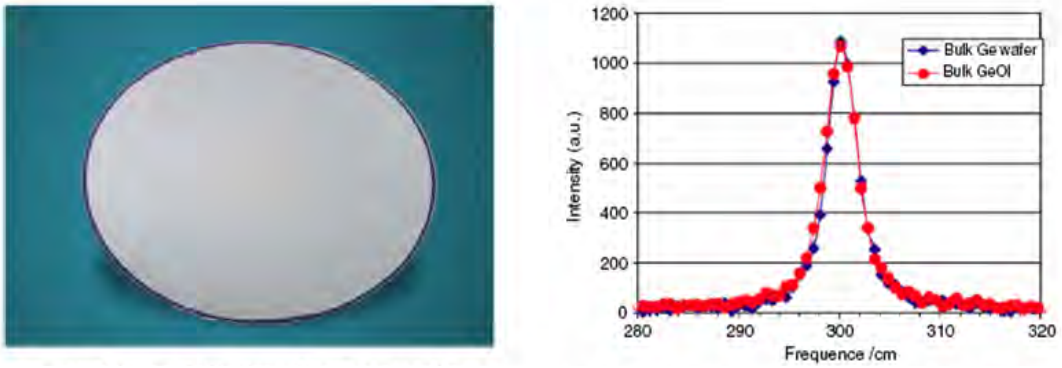

Figure 2.7: (left) a 200 mm GeOI wafer after the bonding process utilizing Smart Cut™ and CMP technique, and (right) Raman spectra taken from bulk Ge donor wafer before bonding and GeOI wafer after bonding process [2.11]

Alternative crystalline GeOI growth process features MILC technique, confining Ge structure dimension (width and thickness) and performed at below 360 ºC where self-nucleation process is non-existent because the competing MILC process is more dominant. In the smaller line dimension, it is possible for a single crystallite to occupy larger volume in the line structure. When the line dimension is smaller than the possible crystallite size, a single Ge crystal can be obtained in the line dimension. Such single crystal GeOI growth in nano-patterned Ge lines using Ni or Au metals is the focus of this work and is demonstrated in Chapter 4.

2.2 Source/drain formation

Another component that we need to consider to realize Ge MOSFETs in monolithic 3D-ICs is low temperature source/drain (S/D) formation. S/D thermal annealing is a strenuous issue in Ge CMOS fabrication for monolithic 3D-ICs because minimum temperatures required for S/D activation are ~ 500 ºC for n^+ and ~ 400 ºC for p^+ S/D [2.16-2.17]. Thus, it is difficult to achieve well-activated S/D below 400 ºC in Ge CMOS fabrication, for it will only result in fractional dopant activation, which degrades the junction quality. This issue is more severe when fabricating the N-channel Ge MOSFET. Up to date reported low temperature S/D formation methods which are acceptable for monolithic 3D-ICs fabrication can be divided into three approaches; (1) dopant activation by laser annealing process [2.18-2.19], (2) Schottky metal-semiconductor (MS) junction formation [2.20], and (3) metal induced dopant activation (MIDA) [2.21-2.22].

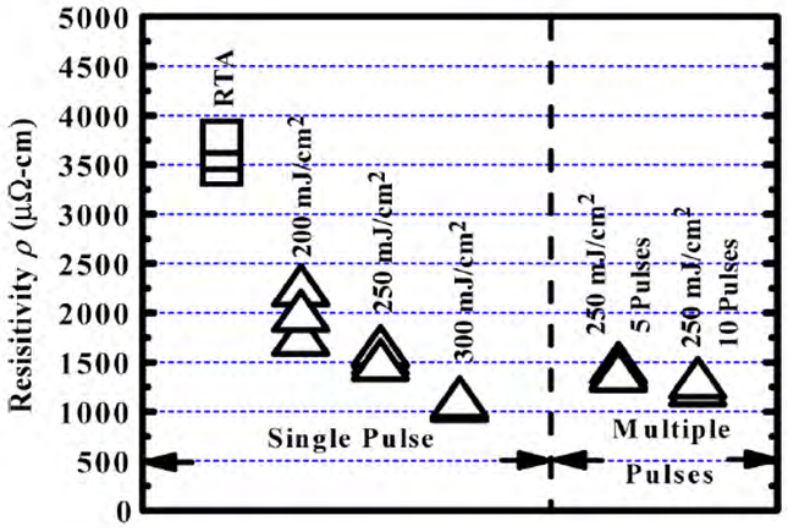

Figure 2.8: Resistivity comparison of S/D junctions activated by RTA and pulsed laser annealing (PLA) processes [2.18]

Very low resistivity has been reported in pulsed laser annealed (PLA) S/D, as compared with S/D activated by RTA process, as shown in Fig. 2.8 [2.18]. As it is

already well known, laser beam works by melting S/D regions locally, regrowing damaged crystals, and finally activating dopants. Because other device regions except S/D are not heated up in this process, this is one of the possible S/D formation techniques that can be used in fabricating monolithic 3D-ICs.

Another candidate to be able to form S/D at below 400 ºC is Schottky MS junction formation technique. As shown in Figure 2.9, because various metals react with Ge at below 400 ºC (Pd at ~170 ºC, Cu at ~220 ºC, Ni at ~220 ºC, Pt at ~310 ºC and Co at 400 ºC) thereby forming germanides with very low resistivity. These germanide/Ge Schottky MS junctions can serve as S/D of the 2nd layer Ge MOSFETs [2.20].

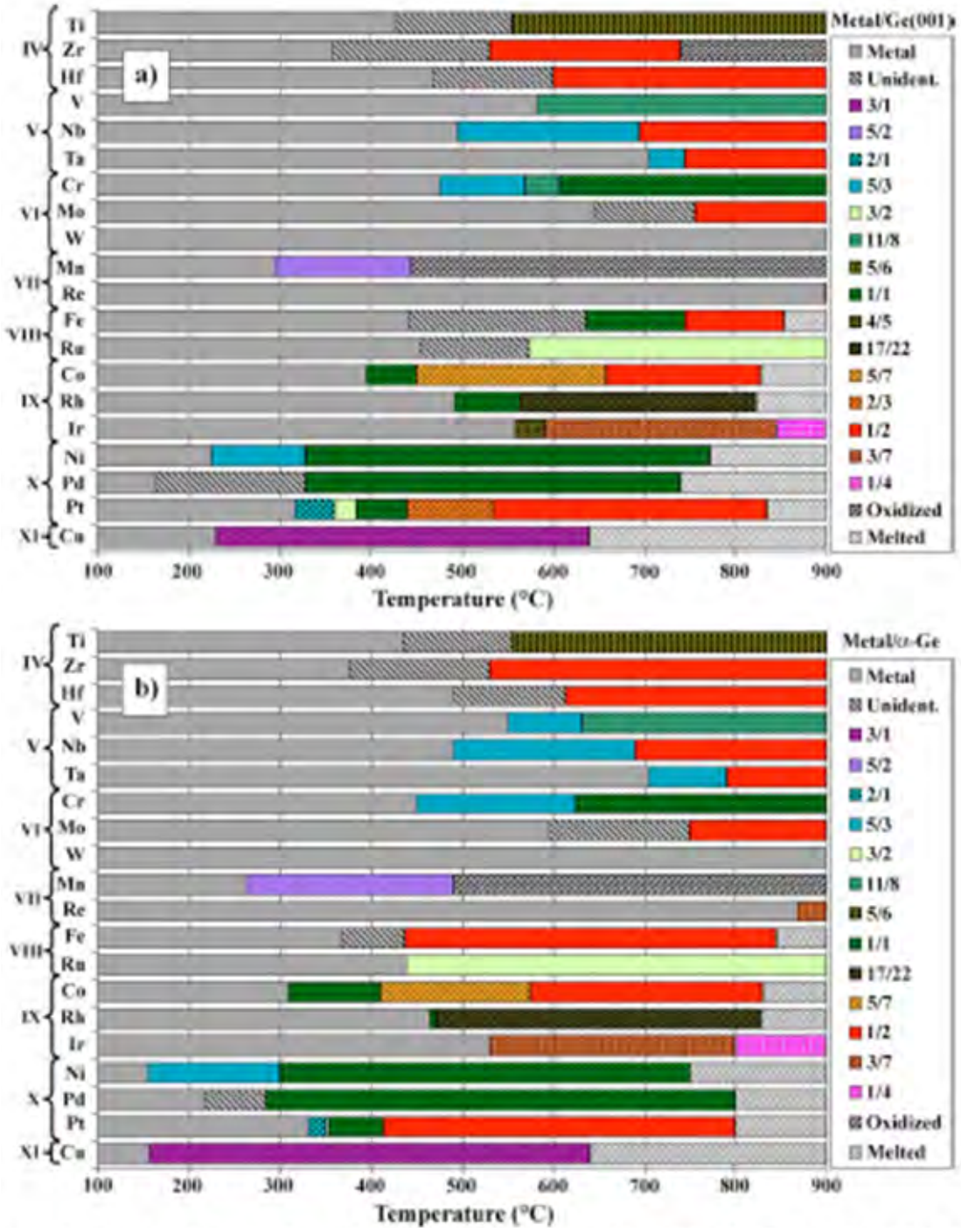

Figure 2.9: Phase sequence of the reaction between 30nm thick transition metals and a 5nm α-Ge deposited on (a) Ge (001) and (b) α -Ge as increasing temperature along 3 ºC/s [2.23]

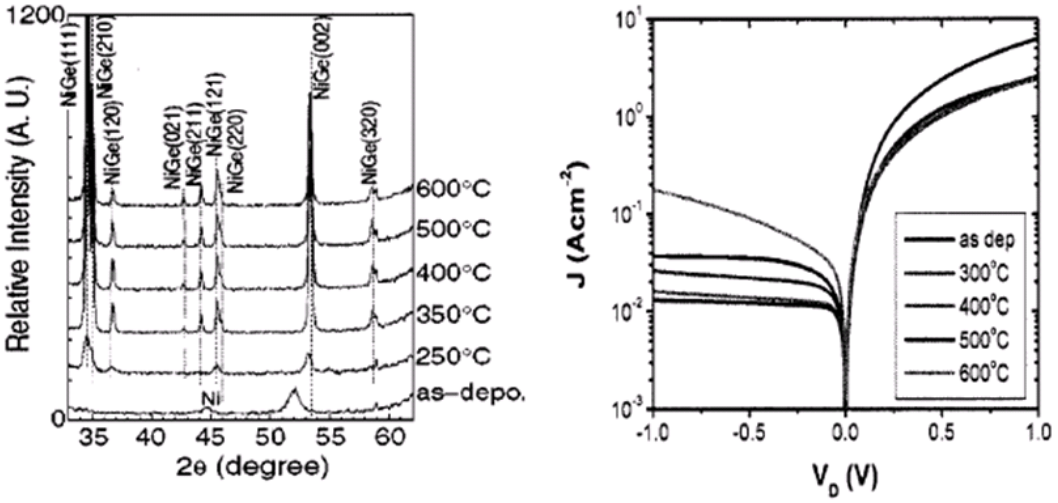

Figure 2.10: XRD profiles and diode I-V characteristics of the NiGe/n-Ge samples annealed at between 300 ºC and 600 ºC [2.20]

As shown in Figure 2.10, a RTA at 400 ºC for 2 minutes is sufficient to form NiGe that provides a suitable Schottky MS junction for S/D of P-channel Ge MOSFETs. Due to its low process temperature (400 ºC), it can be applied for monolithic 3D-ICs fabrication. However, the NiGe obtained at 400 ºC forms an ohmic contact to p-type Ge substrate whereas excellent Schottky MS junction is observed in n-type Ge (Figure 2.11). It is widely known that the work function of NiGe is much closer to the valence band than to the conduction band in Ge because of the Fermi level pinning effect. Other metals like Ti and Co show a similar behavior in p-type Ge, making it difficult to fabricate S/D junctions for N-channel Ge MOSFETs. Inserting ultra thin GeO_x layer between metal and Ge, the Fermi level pinning problem can be relieved due to the suppression of electron wave function penetration from metal to Ge (Figure 2.12). This metal insulator semiconductor (MIS) technique provides Schottky junction in p-type Ge substrate for S/D of N-channel Ge MOSFETs, but a near ohmic contact is again formed in n-type Ge as the previously described germanide/Ge MS junctions. Therefore, it seems difficult to be applied for CMOS compatible process.

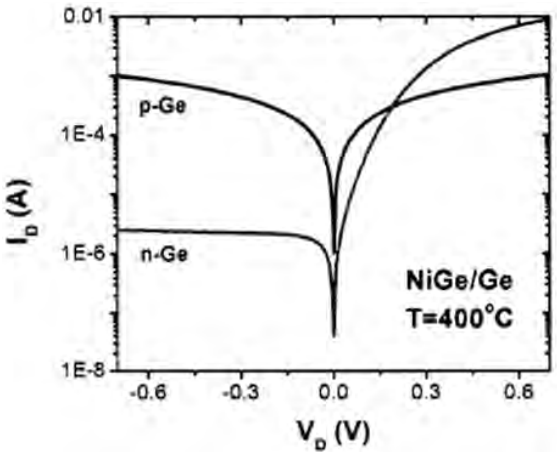

Figure 2.11: Diode I-V characteristics of the NiGe/Ge Schottky junctions formed on p- and n-type Ge substrates at 400 ºC [2.20]

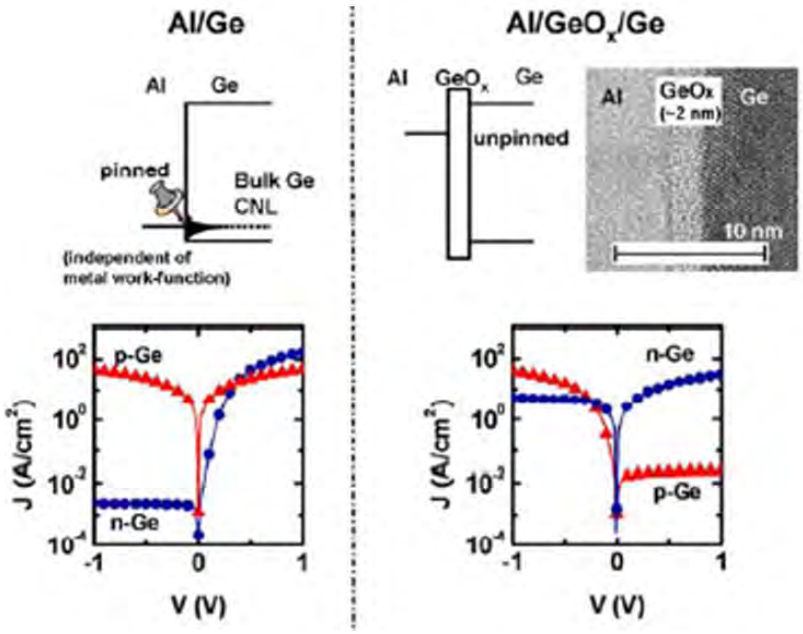

Figure 2.12: Band diagrams, cross sectional TEM image (only Al/GeO_x/Ge), and diode J-V characteristics of Al/Ge and Al/GeO_x/Ge junctions [2.24]

Finally, low temperature MIDA technique featuring metal induced crystallization (MIC) process, to activate S/D at below 400 ºC is introduced in Chapter 5 [2.21-2.22]. Boron and phosphorus atoms in α-Ge film are rearranged and activated at low temperatures (≤ 360 ºC) during MIC process, similar to dopant activation mechanism

by thermal annealing process. Because the MIDA technique successfully activates both n- and p-type dopant atoms at below 400 ºC, it can be used for fabricating Ge CMOS for monolithic 3D-ICs. Additionally, with this MIDA technique, high performance n^+/p & p^+/n junctions and N- & P-channel Ge MOSFETs are demonstrated at below 360 ºC, satisfying the thermal requirement of monolithic 3D-ICs fabrication in Chapter 6.

2.3 Gate dielectric formation and surface passivation techniques

A high-k dielectric can be easily deposited at below 400 ºC, but direct deposition of the high-k dielectric on Ge has exhibited poor electrical characteristics because of high interface trap density (D_{it}). Several high-k materials (HfO_2 [2.25], ZrO_2 [2.26], Al_2O_3 [2.27], and $LaAlO_3$ [2.28]) have been researched for the MOS gate dielectric on Ge, but the carrier mobility in the MOSFETs was degraded. In order to obtain better carrier mobility, usage of an interlayer on the Ge surface for improving the passivation before depositing a high-k dielectric is necessary.

Low temperature ($\leq$ 400 ºC) surface passivation techniques include (1) ozen [2.29] and (2) plasma oxidation [2.31] methods that achieve desirable Ge surface passivation, leading to better CMOS performance. Figure 2.13 shows that by growing GeO_2 via ozone oxidation of Ge and then capping it with HfO_2 or SiO_2 the interface trap density can be significantly reduced [2.29-2.30]. Figure 2.14 shows similar results for plasma oxidation of Ge [2.31]. In both cases 400 ºC oxidation gives best results and hence these techniques can be used for 3D-IC fabrication.

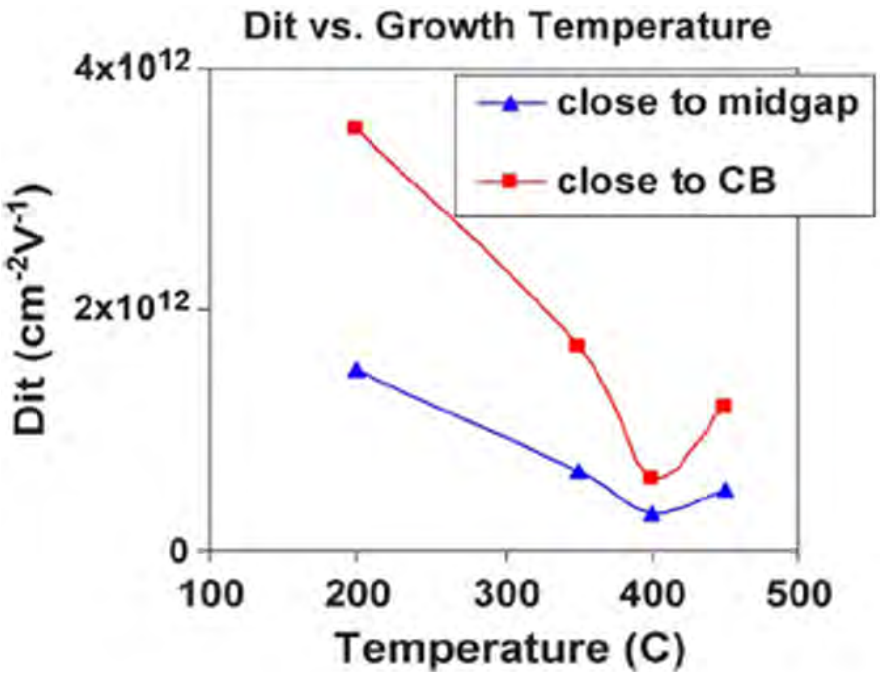

Figure 2.13: interface trap density as a function of the temperature of ozone oxidation of Ge [2.29-2.30]

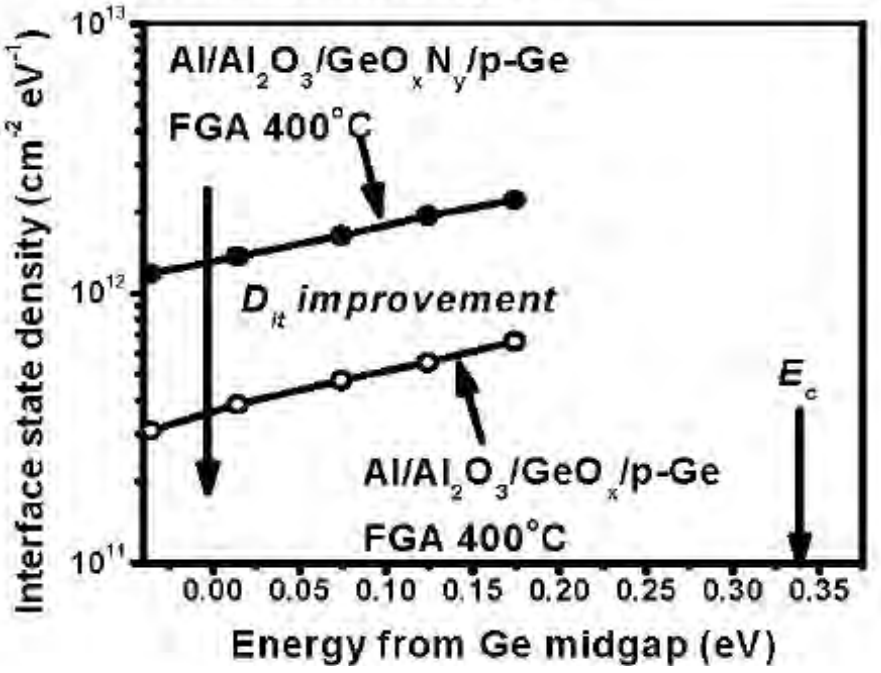

Figure 2.14: interface trap density in Ge bandgap for GeO_xN_y and GeO_x interfacial layer in Ge high-k gate stacks [2.31]

2.4 Gate electrode formation

High-K/metal gate stack is a good low temperature combination for a gate dielectric/electrode formation in monolithic 3D-ICs fabrication. The metal gate electrode can be replaced by a highly doped polycrystalline Ge gate electrode deposited with a diborane treatment method [2.32] at ≤ 310 ºC. Conventionally, low pressure chemical vapor deposition (LPCVD) is used to deposit a thin layer of Si at 500 ºC as a seed for the growth of Ge on SiO_2. Because of the high process temperature required for the Si seed, Ge gate electrode could not be utilized in fabricating monolithic 3D-ICs. By replacing the Si by a boron seed layer deposited by LPCVD from a diborane (B_2H_6) source, the process temperature can be reduced down to 310 ºC [2.32]. The mechanism behind this is that lower B-H bond energy of B_2H_6 (35kJ/mol) compared to the Si-H bonds of SiH_4 (323 kJ/mol) promotes attachment of boron atoms on the SiO_2. Figure 2.1 shows a ross sectional TEM images of poly-Ge film grown with this technique.

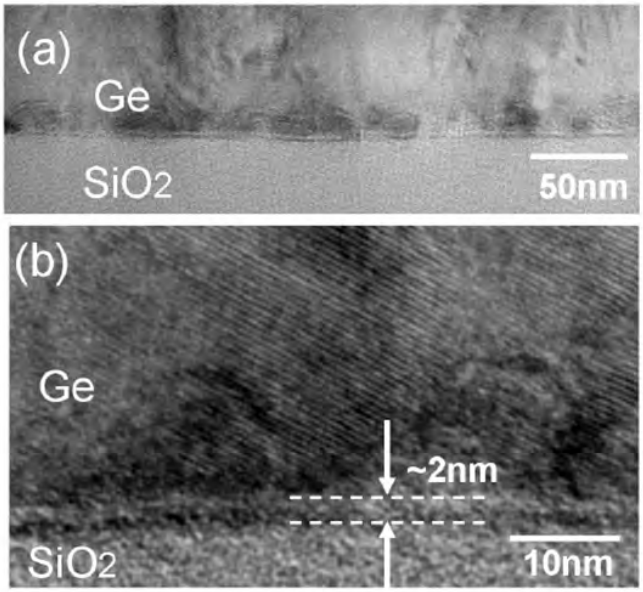

Figure 2.15: Cross sectional TEM images of poly-Ge film deposited at 310 ºC after diborane pretreatment; (a) low and (b) high magnification [2.32]

After depositing the boron seed layer, Ge film can be in-situ doped during the growth with boron and phosphorus using B_2H_6 and PH_3, respectively. As shown in Figure 2.16, very low resistivity (~1mΩ-cm) is observed in p-type Ge gate electrode formed at 310 ºC. This poly-Ge gate electrode fabrication satisfies the thermal requirement (≤ 400 ºC) for monolithic 3D-ICs. In contrast, phosphorus is not sufficiently activated at 310 ºC due to poor crystallization [2.32].

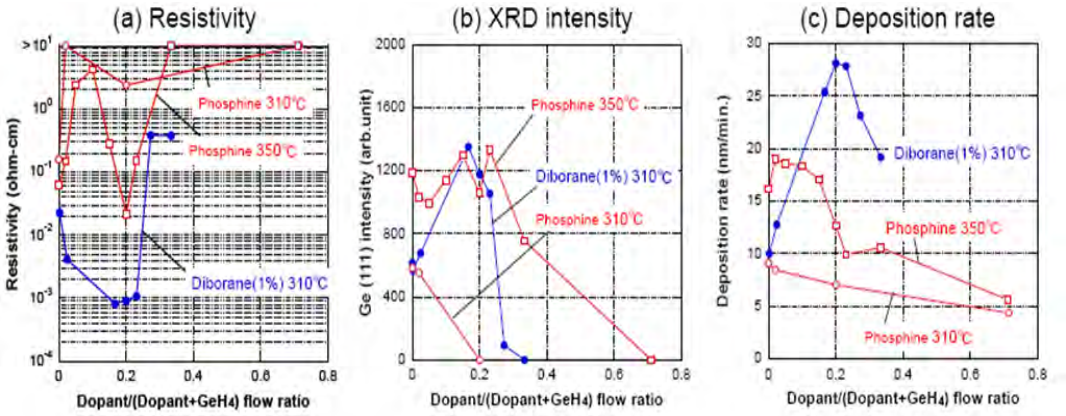

Figure 2.16: (a) Resistivity, (b) XRD intensity, and (c) deposition rate of in-situ doped Ge films as a function of dopants flow ratio [2.32]

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Chapter 3

Metal induced crystallization (MIC) / Metal induced lateral crystallization (MILC) of amorphous germanium

Metal induced crystallization (MIC)/Metal induced lateral crystallization (MILC) are potentially promising approaches to process Ge CMOS at a low temperatures to give minimum impact to the underlying interconnects and device layers. As shown in Figure 3.1 when a sample with α -Ge layer coated with a metal is annealed at a very low temperature where self-nucleation cannot occur, metals vertically and laterally diffuse into the a-Ge layer, crystallizing it in the process. We call the vertical crystal growth "MIC" and the lateral growth "MILC", respectively. When annealing α-Ge thermally without a metal seed, homogeneous nuclei are formed (nucleation process) growing into crystals upon further annealing (crystallization process).

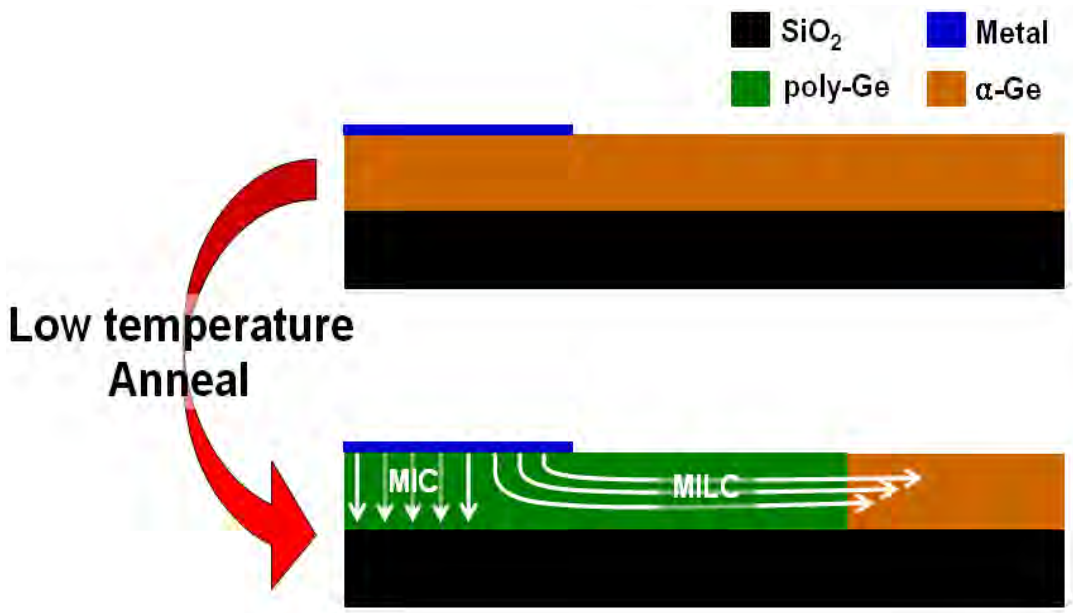

Figure 3.1: Schematic diagram depicting MIC/MILC process

In the MIC/MILC process on the other hand, the existence of metal atoms in α-Ge weakens the bonds in Ge and helps heterogeneous nuclei to be formed at a low temperature where the homogeneous nuclei formation cannot exist. These heterogeneous nuclei then grow into crystals upon further annealing at a low temperature. As a result, this technique dramatically reduces crystallization process temperature, which is a crucial criterion in the fabrication of 3D-ICs. In addition to increasing the grain size, it is important to reduce the number of the heterogeneous nuclei, for grain size depends on the number of nuclei.

MIC/MILC growth is triggered by two kinds of metal groups: (1) Ni-like metals: copper (Cu), palladium (Pd), nickel (Ni), cobalt (Co), platinum (Pt), and titanium (Ti) and (2) Au-like metals: lead (Pb), gold (Au), aluminum (Al), and silver (Ag). Ni-like metals that form germanides with Ge tend to have lower MIC/MILC temperatures than Au-like metals because germanides are normally formed at very low temperatures, compared to eutectic temperatures of the Au-like metals [3.1-3.2]. As shown in Table 3.1, Cu, Pd, Ni, Co, and Pt provide low germanide formation temperatures (Cu_3Ge at 225 ºC, Pd_xGe_y at 251 ºC, PdGe at 340 ºC, NiGe+Ni_5Ge_3 at above 250 ºC, CoGe at 360 ºC, Co_2Ge at 430 ºC, $CoGe_2$+Co_5Ge_7 at above 520 ºC, Pt_3Ge at 300 ºC, Pt_2Ge at

350 ºC, Pt_3Ge_2+PtGe at 375 ºC, PtGe at 390 ºC, and $PtGe_2$ at above 450 ºC). In comparison, the eutectic temperatures of the Au-like metals, such as Pb, Au, Al, and Ag, are 327ºC, 356ºC, 423ºC, and 650ºC, respectively [3.1].

In this chapter, we introduce a comprehensive physical mechanism for predicting MIC/MILC growth rate and experimentally demonstrate self-nucleation/MIC/MILC results of α-Ge with Pd, Cu, Ni, Au, Co, Al, Pt, and Ti. X-ray diffraction (XRD) and transmission electron microscopy (TEM) are used for experimental analysis.

Germanide	Sheet resistance (Ω/□)	T_a (°C)	Germanide	Sheet resistance (Ω/□)	T_a (°C)
Co+CoGe	9.9	360	Pd+Pd_xGe_y	7.3	251
Co_5Ge_7+$CoGe_2$	6.3	520	PdGe	4.4	340
$CoGe_2$	5.5	650	Pt+Pt_5Ge	16	300
Co_2Ge	7.2	430	Pt_2Ge	8.7	350
Cr_5Ge_3	23	480	Pt_3Ge_2+PtGe	6.9	375
Cr_5Ge_3	51	560	PtGe	6.3	390
CrGe	26	670	$PtGe_2$	4.2	450
Cu_3Ge	8.5	225	$PtGe_2$	6.7	720
FeGe or Fe_5Ge_6	26	390	$PtGe_2$	11	807
FeGe or Fe_5Ge_6	28	440	Re_3Ge_7	81	925
$FeGe_2$	14	580	Rh+RhGe	10	440
Hf_xGe_y+Hf	26	470	RhGe	21	480
Hf_xGe_y	24	545	$Rh_{17}Ge_{22}$	32	600
Ir+Ir_4Ge_5	7.0	260	Ru+Ru_2Ge_3	30	560
Ir+Ir_4Ge_5	7.2	460	Ru_2Ge_3	3800	700
Ir_3Ge_7	11	580	Ru_2Ge_3	2800	925
Mn_5Ge_2	180	284	$TaGe_2$	18	780
Mn_5Ge_2	160	320	Ti+Ti_xGe_y	63	480
MnO	710	520	Ti_5Ge_6	58	760
$Mo_{13}Ge_{23}$	18	720	Ti_5Ge_6	120	925
Nb+Nb_5Ge_3	20	600	V+V_xGe_y	18	500
$NbGe_2$	30	680	V_5Ge_3	32	600
Ni+NiGe+Ni_5Ge_3	7.7	250	Zr+Zr_xGe_y	110	360
NiGe+Ni_5Ge_3	8.5	270	Zr+Zr_xGe_y	62	460
NiGe+Ni_5Ge_3	10	285	Zr_xGe_y	110	620
NiGe+Ni_5Ge_3	5.0	315	$ZrGe_2$	85	760
NiGe	3.1	380	$ZrGe_2$+ZrO_2	190	925

Table 3.1: Sheet resistance and formation temperatures of germanides on α-Ge with several metals [3.2]

3.1 Mechanism

Although the exact principle behind MIC/MILC is not yet known, Hayzelden *et al.* made an attempt to explain this MIC/MILC phenomenon with chemical potential difference and its impact on diffusion [3.3]. Germanides and metal atoms respectively act as a medium of MIC/MILC in Ni-like and Au-like metals. As shown in Figure 3.2, Ni-like metals move toward α-Ge because of chemical (or physical) potential difference between c-Ge/NiGe (high potential) and NiGe/α-Ge (low potential) interfaces. The diffused Ni-like metals react with α-Ge to form germanides and the process repeats. The Ge atoms remaining behind attach to the germanide template to form crystalline Ge [3.3-3.4]. Au-like metals also migrate towards α-Ge region at above eutectic temperature, leaving crystalline Ge phase behind [3.1, 3.4-3.5].

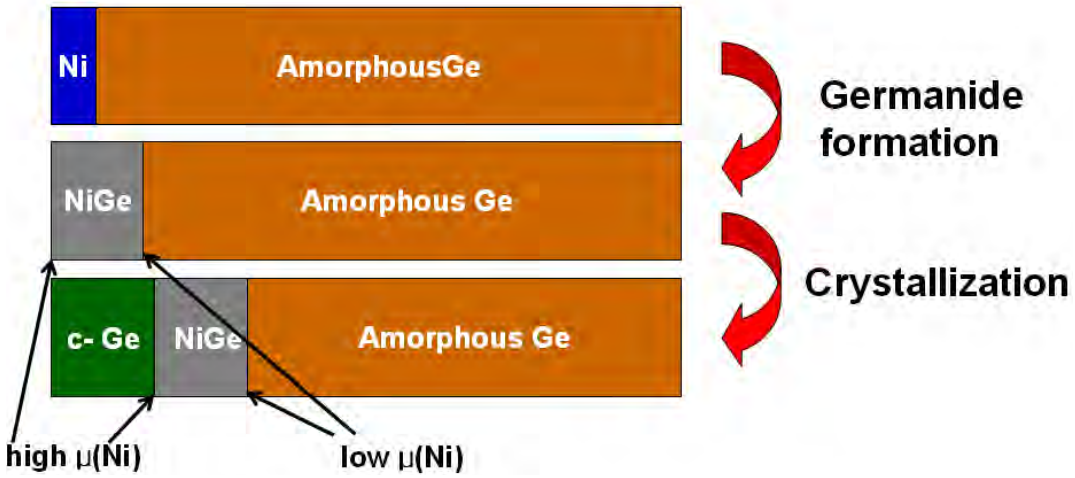

Figure 3.2: Schematic diagram showing 1D MIC/MILC process with Ni

Normally, Ni-like metals are more attractive in the MIC/MILC process because it is possible to control the concentration of metals supplied to the Ge. It is possible to form very thin germanide layer at a low temperature, and then selectively etch unreacted metals leaving the thin germanide layer on the Ge surface. As a result, only low concentration of metals is diffused into the Ge during the MIC/MILC process [3.7].

3.2 Experimental works

In this section, three significant sets of experiments will be described and discussed in turn; (1) Self-nucleation, (2) MIC, and (3) MILC on α-Ge planar structures.

3.2.1 Self-nucleation of α-Ge

A 200nm thick α-Ge film was deposited at 300 ºC in a low pressure chemical vapor deposition (LPCVD) furnace on a 1μm thermally grown SiO_2 film on Si (Figure 3.3). The control samples were used to find self-nucleation temperature by isothermal anneal in a N_2 ambient for 1 hour at 300 ºC, 350 ºC, 360 ºC, 370 ºC, 380 ºC, 390 ºC, 400 ºC, 450 ºC, 500 ºC, and 550 ºC. These samples were characterized using XRD (Cu Kα, λ=1.5408Å) peak intensities, bright field TEM images, and selective area electron diffraction (SAED) patterns (Figure 3.4).

Figure 3.3: Control sample structure to observe self-nucleation

Kanno *et al.* have used the imaginary part of reflective index of isothermally annealed α-Ge [3.8] to report a temperature of ~500 ºC for self-nucleation. Since there is a finite possibility of having small crystals due to self-nucleation forming even below 500 ºC, several different temperatures were investigated (for fixed time of 1 hour) to determine the temperature at which self-nucleation starts.

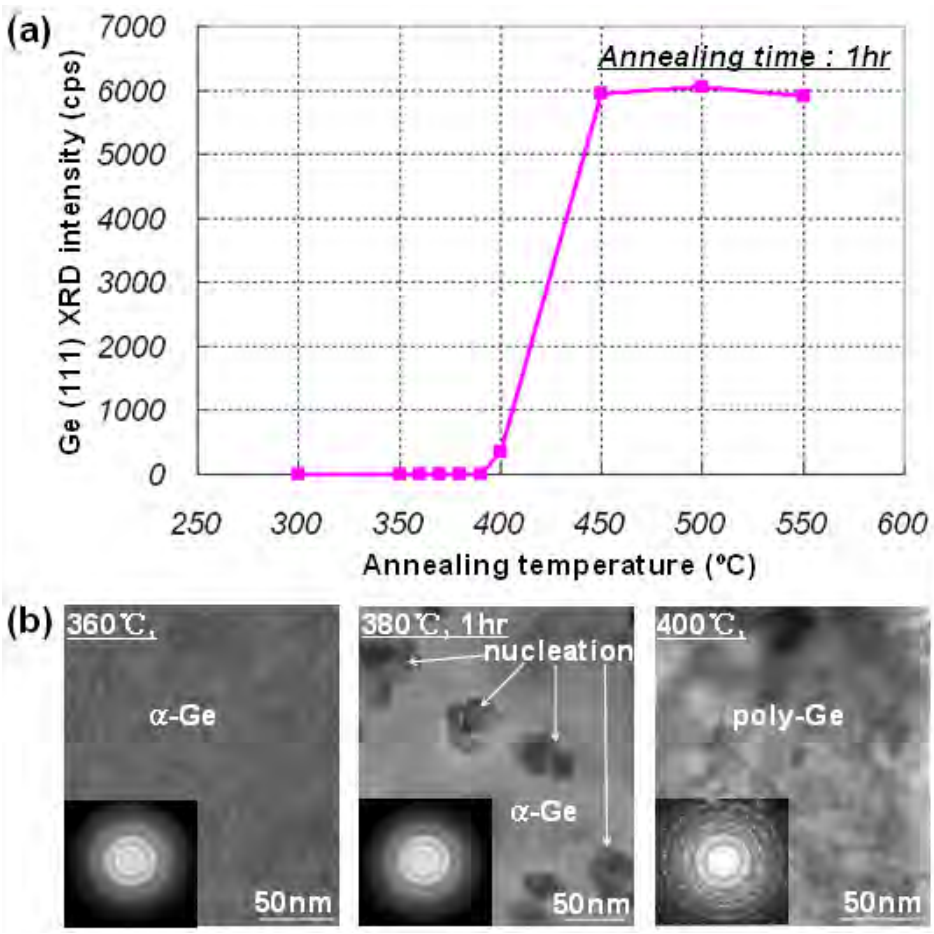

Figure 3.4: Ge (111) XRD peak data, SAED patterns, and bright field TEM images; (a) Ge (111) XRD peak intensities of control samples annealed between 300 ºC and 550 ºC (b) bright field plane view of TEM images and SAED patterns of control samples after annealing for 1 hour at 360 ºC, 380 ºC, and 400 ºC [3.9]

This was achieved using XRD and TEM analysis as shown in Figure 3.4. According to the sheet resistance measurements and XRD analysis, self-nucleation began around 400 ºC. The sheet resistance of the control sample (without metal) annealed at 400 ºC was ~4.5×10^{3} Ω/□ and Ge (111) XRD peak intensity was observed at this temperature, whereas below 390 ºC the sheet resistance was quite high (> 1×10^{7} Ω/□) and no Ge (111) peak intensity was observed. Above 450 ºC, the Ge (111) peak intensity saturated implying that above this temperature the crystal size did not increase. However, our TEM analysis suggested that the temperature at which self-nucleation commences was a bit lower at 380ºC, as shown in Figure 3.4 (b). This

small discrepancy arose because small nucleation spots were not detected by XRD and sheet resistance measurements. TEM studies showed no grains, a few grains (size : 15-20 nm), and many grains (size : 30-40 nm) after annealing for 1 hour at 360 ºC, 380 ºC, and 400 ºC, respectively.

Based on these results, 380 ºC was determined to be the maximum temperature allowed for subsequent MIC/MILC experiments. This is because the scope of the experiment was to achieve crystallization induced only by metals, not by self-nucleation. For the MIC/MILC process, the existence of homogeneous nuclei formed by the self-nucleation can increase total number of nuclei by adding homogeneous nuclei to number of heterogeneous nuclei by the MIC/MILC. As a result, this will effectively decrease the overall grain size.

3.2.2 Metal induced crystallization (MIC) of α-Ge

For MIC samples shown in Figure 3.5, 5nm thick metal films, Pd, Cu, Ni, Au, Co, Al, Pt, and Ti, were deposited on the 200nm thick undoped α-Ge films immediately after removing the native GeO_x with 2% hydrofluoric (HF) acid. In order to investigate reaction temperatures between metals and Ge, undoped MIC samples were isothermally annealed in a N_2 ambient for 1 hour at 300 ºC, 350 ºC, 360 ºC (only for Ni-, Au-, Co-, Pt-, and Ti-MIC processes), 380 ºC (only for Co-, Al-, Pt-, and Ti-MIC processes), 400 ºC, and 450 ºC.

Figure 3.5: Control sample structure to observe the MIC process

Figure 3.6 (b) shows XRD profiles of 200nm thick undoped Ge films crystallized by Co-MIC process at several temperatures. Because the intensities of Ge (111) peaks are the strongest among others, these peaks are used to evaluate the degree of Ge crystallization.

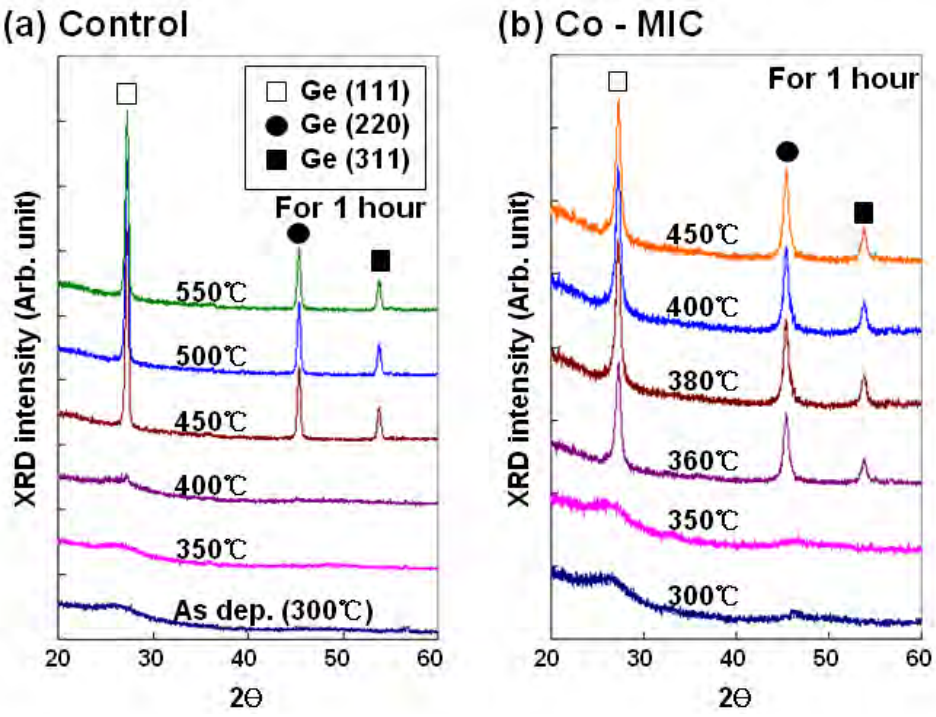

Figure 3.6: XRD profiles of 200nm thick undoped Ge films; (a) control samples As-deposited and annealed for 1 hour at 350 ºC, 400 ºC, 450 ºC, 500 ºC, and 550 ºC and (b) Co-MIC samples annealed for 1 hour at 300 ºC, 350 ºC, 360 ºC, 380 ºC, 400 ºC, and 450 ºC

We did not observe any Ge peaks after annealing Co-MIC samples at below 350 ºC for 1 hour, confirming that there was no crystallization of the Ge film below this temperature. Although Co-MIC process started at 360 ºC, process temperature above 380 ºC was needed to fully crystallize the 200nm thick undoped Ge films. The sample annealed at 360 ºC had a slightly lower Ge (111) peak intensity than samples annealed at above 360 ºC, meaning partial crystallization of the Ge film. Normally, thicker crystallized film provides a higher XRD peak intensity assuming that the size of crystal grains does not change. In fact, the size of crystal grains in every Co-MIC

sample was almost the same (explained in Figure 3.8 in detail). The Ge (111) peak saturates at above 380 ºC, which implies that there was no additional crystal growth with respect to grain size as annealing temperature increases. This is mainly because the large number of heterogeneous nuclei formed by the assistance of Co prevents crystal grains from increasing their size during the Co-MIC process. According to TEM analysis, grain size in Ge films crystallized by Ni-MIC process was around 50 nm. Based on this and full width half maximum (FWHM) data on Ge (111) peaks in Co- and Ni-MIC samples (Figure 3.8), the size of Ge crystal grains after the Co-MIC process is expected to be slightly bigger than 50nm. In general, a small FWHM value indicates a big crystal grain size because there is small number of crystal grains in one x-lay beam spot. Further analysis using FWHM measurements is performed with 200nm thick undoped Ge samples crystallized by the eight metals at the end of this sub-section (Figure 3.8).

In a similar manner, the crystal types of the Ge films are classified (amorphous, partially crystallized, and fully crystallized) after annealing between 300 ºC and 450 ºC for 1 hour with several metals including Pd, Cu, Ni, Au, Co, Al, Pt, and Ti (MIC processes). Pd, Cu, Ni, Co, Pt, and Ti normally form germanides with Ge as transition metals [3.2], and diffuse into Ge layer by further annealing process leading to MIC. As previously explained, Ni-like metals tend to move toward α-Ge region after forming germanides because of their lower chemical potential at the germanides/α-Ge interface than at the germanide/crystallized Ge (c-Ge) [3.3-3.4]. The metals moving forward subsequently react with α-Ge to form new germanides and this process is repeated. The Ge atoms remaining behind attach to the germanide template to form c-Ge. In contrast, Au and Al, being Au-like (eutectic) metals, just diffuse into the Ge layer around their eutectic temperatures (356 ºC for Au and 423 ºC for Al). Because these metals (both Ni and Au-like metals) in Ge layer weaken Ge-Ge bonding energy, the metals induce Ge crystallization at low temperatures.

Gaudet *el al.* also reported MIC phenomenon and temperature dependent phases of germanides on α-Ge substrate with 20 transition metals including metals used in this work (Pd, Cu, Ni, Co, and Pt) [3.2]. Even though we have used a different annealing

method (furnace anneal at a selected temperature) and ambient (in N_2) compared to those of Gaudet *el al.* (thermal ramp at 3 ºC/sec in purified He), our results (Figure 3.7) agree with Gaudet *el al.* in that the transition metals used in this work (such as, Pd, Cu, Ni, Co, and Pt) give rise to significant reduction in the crystallization temperature of α-Ge. In addition, our results also agree with the order in which MIC process begin in these metals according to increase in temperature (Pd→Cu→Ni→Co→Pt).

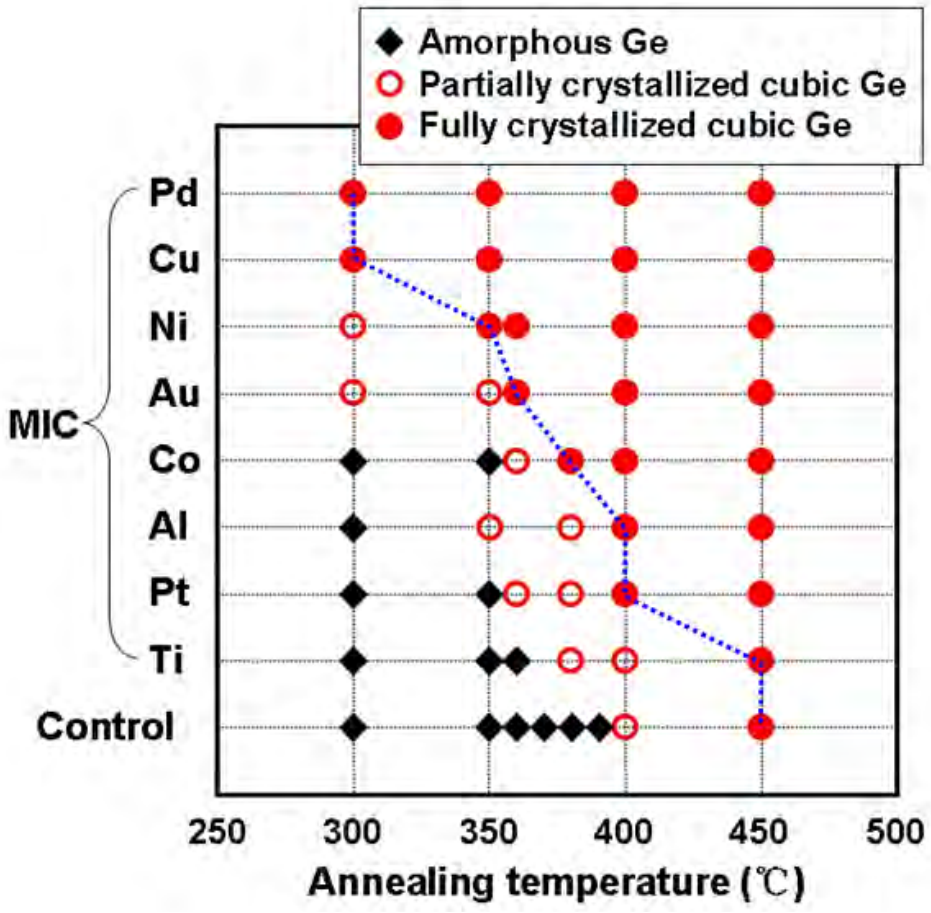

Figure 3.7: Phase diagram describing crystal status of 200nm thick undoped Ge films processed by metal-induced crystallization (MIC) technique with Pd, Cu, Ni, Au, Co, Al, Pt, and Ti for 1 hour at several temperatures between 300 ºC and 450 ºC

Pd- and Cu-MIC processes in α-Ge seem to start below 300 ºC according to XRD analysis which shows the 200 nm thick α -Ge films are fully crystallized after annealing at 300 ºC for 1 hour. Ni- and Au-MIC processes also starts at 300 ºC, but

full crystallization in α-Ge film is achieved at above 350 ºC for Ni and 360 ºC for Au. Thus, given the same temperature, the diffusivity of Pd in Ge is expected to be similar to that of Cu but much higher than those of Ni and Au, although it is difficult to predict exact diffusivities of the metals at these low temperatures due to lack of data. The result in Figure 3.7 is also supported by the fact that Pd and Cu require lower temperatures to form germanides than Ni, Cu_3Ge at 225 ºC, Pd_xGe_y at 251 ºC, PdGe at 340 ºC, and NiGe+Ni_5Ge_3 at above 250 ºC [3.2]. Even though both Ni- and Au-MIC processes partially crystallized the 200 nm thick undoped Ge film at 300 ºC for 1 hour, Ni-MIC process was slightly faster than Au-MIC. By comparing Ge (111) peak intensities in more detail, the Ni-MIC process crystallized ~56 % of the Ge film while Au-MIC process crystallized ~47 % of the film. Au dramatically diffused into the α-Ge film at above its eutectic temperature and eventually crystallized the 200 nm thick α-Ge film at above 360 ºC. Co-MIC process partially starts at 360 ºC (~72 % of the 200 nm undoped Ge film was partially crystallized) and at least 380 ºC was needed to fully crystallize the α-Ge film. Therefore, diffusivity of Co seems to be much lower than that of Pd, Cu, and Ni at the same temperature. Al, the other eutectic metal in this experiment, fully crystallized the 200 nm thick undoped α-Ge film at above 400 ºC, although Al-MIC process began at 350 ºC. Pt and Ti also caused the MIC process on α-Ge films, but the process temperatures were slightly higher than the previous metals, as shown in Figure 3.7. The diffusivities of Pt and Ti in Ge seem to be much lower than those of the previously introduced metals. In addition, Pt and Ti germanides are formed, Pt_3Ge at 300 ºC, Pt_2Ge at 350 ºC, Pt_3Ge_2+PtGe at 375 ºC, PtGe at 390 ºC, $PtGe_2$ at above 450 ºC, and Ti_xGe_y at above 480 ºC [3.2] at slightly higher temperatures than the previously described metals. As a result, Pt- and Ti-MIC processes starts at 360 ºC and 380 ºC, respectively. Fully crystallized 200 nm α-Ge films were obtained at above 400 ºC for the Pt-MIC and at above 450 ºC for the Ti-MIC. Although the control sample was completely crystallized at 450 ºC, α-Ge film with 5 nm Ti is most likely to be crystallized by both self-nucleation and Ti-MIC processes at that temperature, which explains why its FWHM value is different from that of control sample annealed at 450 ºC (Figure 3.8). Based on our thermal budget

for 3D-ICs (≤ 380 ºC) where crystallization effect by self-nucleation (or self-crystallization) process does not exist, five metals (Pd, Cu, Ni, Au, and Co) were selected for metal induced dopant activation (MIDA) experiments described in Chapter 4.

To compare the approximate grain sizes, FWHM data from XRD Ge (111) peaks of all MIC samples were extracted, as shown in Figure 3.8. These FWHM data were extracted from only fully crystallized films because the depth of the partially crystallized Ge films can be smaller than the size of Ge crystal grains obtained by MIC processes. Here, lower FWHM value indicates a larger crystal grain size, and from this we can gain insight in the relative grain sizes of crystallized Ge films.

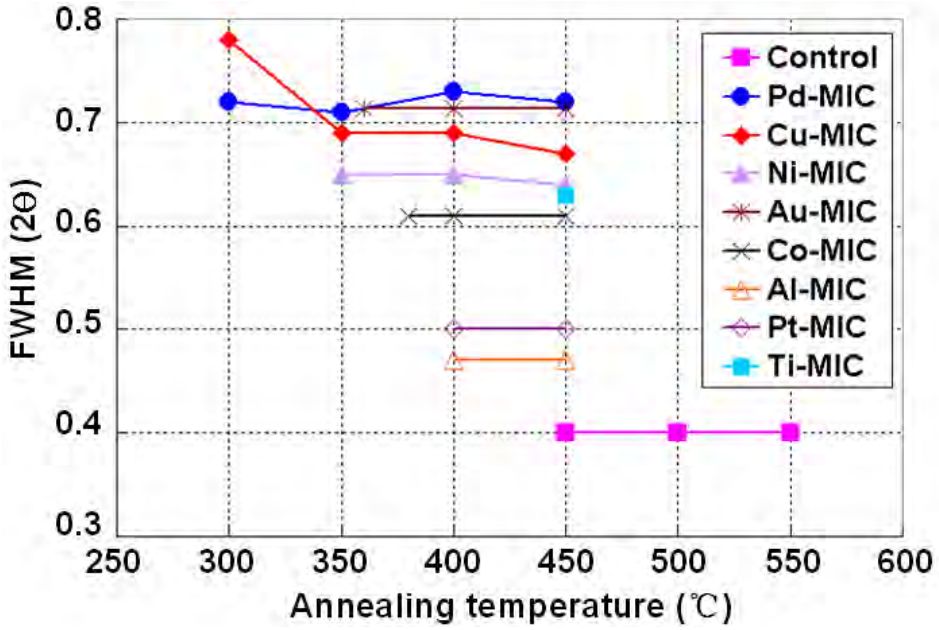

Figure 3.8: Full width half maximum (FWHM) data extracted from Ge (111) peaks of 200nm thick undoped control and MIC samples with 5nm thick metals as a function of annealing temperature

Control sample needed higher crystallization process temperature, but it provided the biggest grain size having the lowest FWHM value (~0.4°). The size of Ge crystal grains in all MIC samples is expected to be smaller than 100nm because grain size of the fully crystallized Ge film at above 450 ºC is known to be around 100 nm by TEM

analysis. Pt- and Al-MIC processes provided almost comparable grain size to the control sample. As already mentioned, the grain size of films crystallized by Ni-MIC was found to be roughly 50 nm, determined by TEM analysis. Thus, it is expected that the size of Ge crystal grains created by the Co-MIC process will be slightly bigger than 50 nm, whereas samples crystallized by the Pd-, Cu-, Ni-, and Au-MIC will have smaller grain sizes than 50 nm. We also observed a decrease of FWHM (increased grain size) between 300 ºC and 350 ºC in the Cu-MIC sample. Except in this case however, the sizes of crystal grains created by the MIC processes were almost independent of the process temperature. This is due to the fact that a number of heterogeneous nuclei formed by the assistance of metals prevented the Ge films from forming larger grains.

3.2.3 Metal induced lateral crystallization (MILC) of α-Ge

After depositing 20 nm thick low temperature oxide (LTO) on a 100 nm α-Ge film, the samples are patterned to form Ge planar structures on the insulating substrate and followed by a 5 nm thick Ni or Au seed deposition using an e-beam evaporator. The deposited Ni or Au is patterned using a lift-off process. The α-Ge planar structure is 5 mm long and 80 μm wide.

Figure 3.9: Control sample structure to observe the MILC process [3.9]

The planar structure samples with 5 nm thick Ni seed are isothermally annealed in a N_2 ambient for 1 hour at 360 ºC, and characterized using TEM. Dendrite-type lateral growths are observed in 5 nm Ni seeded samples at 360 ºC, as shown in Figure 3.10 and the lateral growth length is around 2 μm after annealing at 360 ºC for 1 hour. It is

expected that Ni germanides have favorable precipitate orientations like $NiSi_2$ (<100>, <110>, and <111>) during MILC process [3.3, 3.8]. Since the Ge atoms remaining behind attach to the limited kinds of Ni germanide templates to form crystalline Ge during migration of Ni germanides, there are only a few MILC growth directions causing dendrite-type growth.

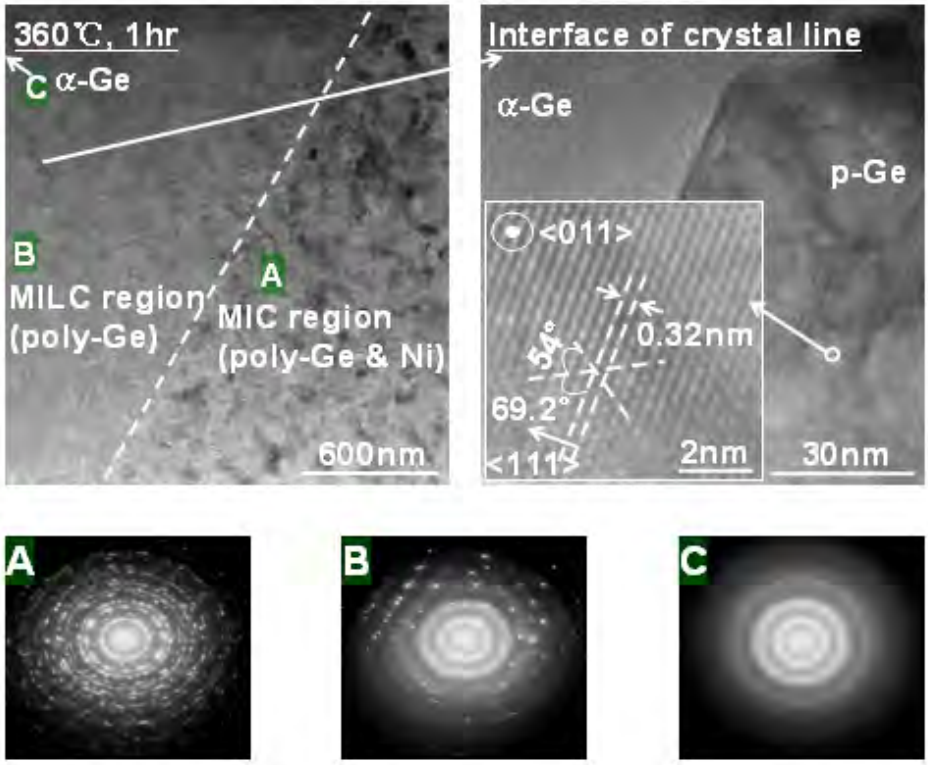

Figure 3.10: Bright field plane view TEM images and SAED patterns of Ni MILC growth on α-Ge planar structure sample after annealing for 1 hour at 360 ºC [3.9]

On the other hand, Au MILC exhibits plane-type growth mechanism because there are no favorable precipitate orientations (Figure 3.11). In the past, Kanno *et al.* have reported that MILC growth rates of a sample with 5nm thick Ni seed are 0.8 μm/hr with 5 hour incubation time and 20 μm/hr with 10 minutes incubation time at 350 ºC and 400 ºC, respectively [3.8]. Our MILC growth rate of ~2 μm/hr at 360 ºC is very reasonable when compared with 0.8 μm/hr at 350 ºC and ~20 μm/hr at 400 ºC. The SAED patterns in Figure 3.10 are taken at MIC (right on the metal seed), MILC (next

to the metal seed), and α-Ge (far away from the metal seed) regions. After high resolution (HR) TEM analysis (axis coming out from the HRTEM image is <011>), the interface between crystal Ge and α-Ge is observed and the growth orientation of the crystal turns out to be parallel to <111> direction, which is one of the favorable directions. The calculated distance between atoms in one direction is around 0.32 nm, yielding a <111> orientation. From the selected direction, the other two directions are found to be at angles of 69.2° and 54°, respectively. The single crystalline Ge in the bright field HRTEM image shows three orientations, <002>, <111>, and <111> if a beam axis of <011> is chosen.

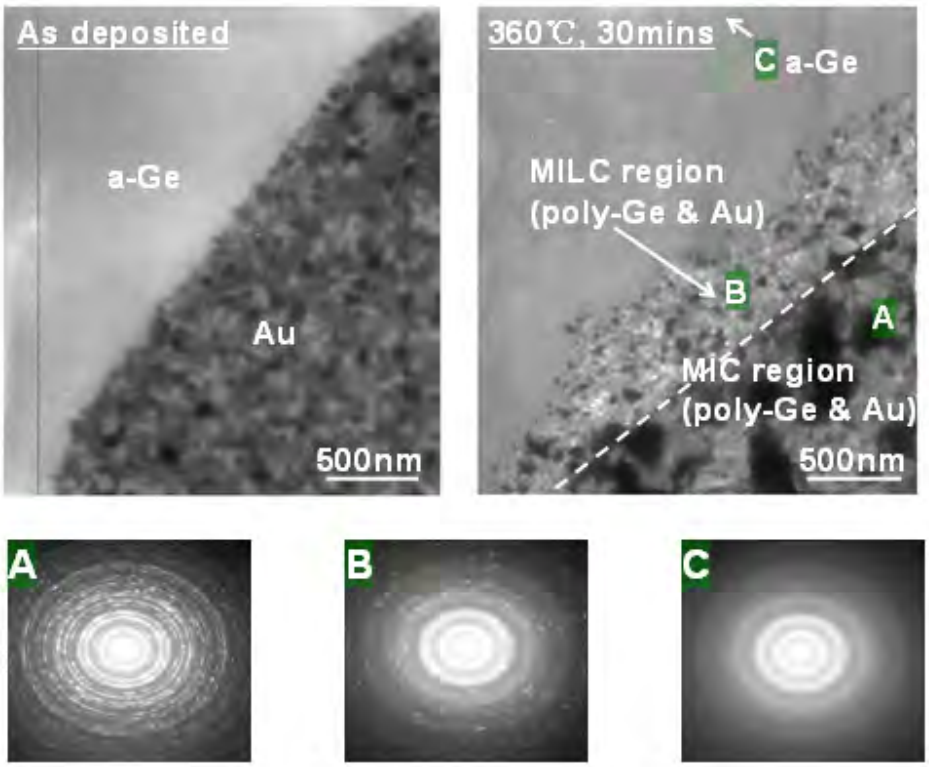

Figure 3.11: Bright field plane view TEM images and SAED patterns of As-deposited α-Ge planar structure sample and Au MILC growth on the sample after annealing for 30 minutes at 360 ºC [3.9]

Planar α-Ge structure sample with 5 nm thick Au seed is annealed in a N_2 ambient for 30 minutes at 360ºC. Figure 3.11 shows bright field plane view TEM images of

As-deposited samples, which are annealed for 30 minutes at 360 ºC, respectively. Roughly 0.543 μm plane-type MILC growth is observed after annealing for 30 minutes at 360 ºC which is slightly higher than Au-Ge eutectic temperature (~356 ºC). Since the self-nucleation of α-Ge occurs at around 380 ºC and the eutectic temperature of Au-Ge is 356 ºC, Au is a viable candidate to obtain single crystalline Ge using MILC growth (Pb with a eutectic temperature of 327 ºC presents another viable candidate). As previously discussed, plane-type MILC growth mechanism is shown in Au MILC because there are no favorable orientations for crystal growth during migration of Au (Figure 3.11). The Ge atoms leaving behind (or diffusing through Au) are crystallized following the crystal orientations of Au, but there are no any limited kinds of growth directions because crystal orientation of Au itself is expected to be random. The SAED patterns in Figure 3.11 are also taken at MIC, MILC, and α-Ge regions similar to the case of Ni MILC.

3.3 Summary

In this chapter, we have systematically investigated self-nucleation, MIC, and MILC processes in α-Ge with TEM and XRD systems. Eight different metals, Pd, Cu, Ni, Au, Co, Al, Pt, and Ti were initially used in the MIC work, but three of them, Al, Pt, and Ti were later excluded because of their high reaction temperatures with Ge that exceeds the thermal budget for fabrication of 3D-ICs where self-nucleation does not affect the MIC/MILC process (≤ 380 ºC). Based on the previous experiment results, these MIC and MILC processes were applied to activate dopant atoms (Chapter 5) and obtain single crystalline GeOI structure (Chapter 4) below 400 ºC.

3.4 References

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Chapter 4

Single crystalline germanium on insulator (GeOI) growth using metal induced lateral crystallization (MILC)

Traditional metal induced lateral crystallization (MILC) [4.1-4.5] results in poly-crystalline film, which degrades transistor performance [4.6] by (1) reducing the on-current, (2) adversely impacting the subthreshold slope, and (3) increasing leakage current and power dissipation. In addition, the impact of grain boundaries on Ge is more severe than Si because of its higher mobility and lower band-gap. Thus, it is imperative to, at least, obtain a device-suited single crystalline Ge on silicon dioxide (SiO_2), at a low temperature for high performance monolithic 3D ICs.

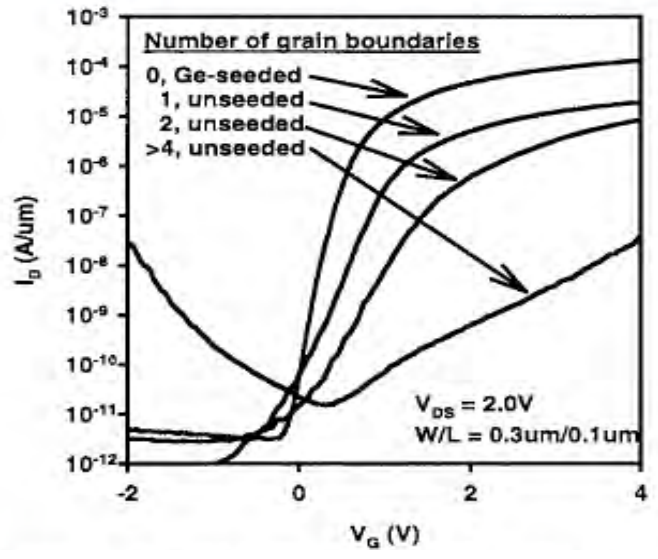

Figure 4.1: Effects of grain boundaries on transistor performance [4.6]

In this chapter, self–nucleation free single crystalline germanium on insulator (GeOI) growth process by using MILC technique and confining line dimension is propsed. As α-Ge film is annealed at a high temperature, small clusters of atoms known as self-nuclei start forming at a random position in the α-Ge flim. Further annealing makes the nuclei to grow into crystals. Because the self-nucleation, occurred at random positions is a competing process to MILC which results in small crystallites, it is important to use this MILC technique at the self-nucleation free temperature region (≤ 380 ºC) for bigger crystallites.

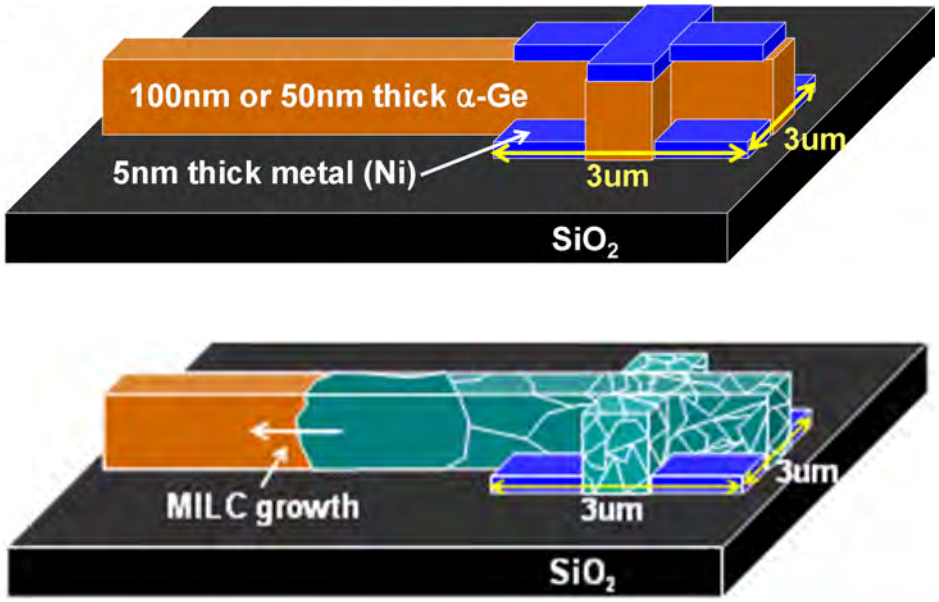

Figure 4.2: Schematic diagram of α-Ge thin line structure to obtain single crystalline GeOI using MILC technique; (a) before annealing and (b) after annealing

Another important aspect for obtaining the single crystal Ge is the dimension (thickness and width) of Ge line structure. In the smaller line dimension, one crystallite occupies the larger volume in the line structure (Figure 4.2). When the line dimension (thickness and width) is smaller than the possible crystallite size, the single crystal Ge can be obtained in the line dimension. This single crystal growth Ge-on-insulator in nano-patterned Ge lines is experimentally demonstrated using Ni and Au.

4.1 Experiment

After depositing 20 nm thick low temperature oxide (LTO) on a 100 nm α-Ge film, the samples were patterned to make line structures on a insulating substrate. The α-Ge thin line structures (Figure 4.3) have several different line widths varying from 550 nm to 900 nm with 50 nm gap. The widths of lines in the left scanning electron microscopy (SEM) image of Figure 4.3 are 550nm (left-side line from the cross pattern) and 500nm (right-side line from the cross pattern).

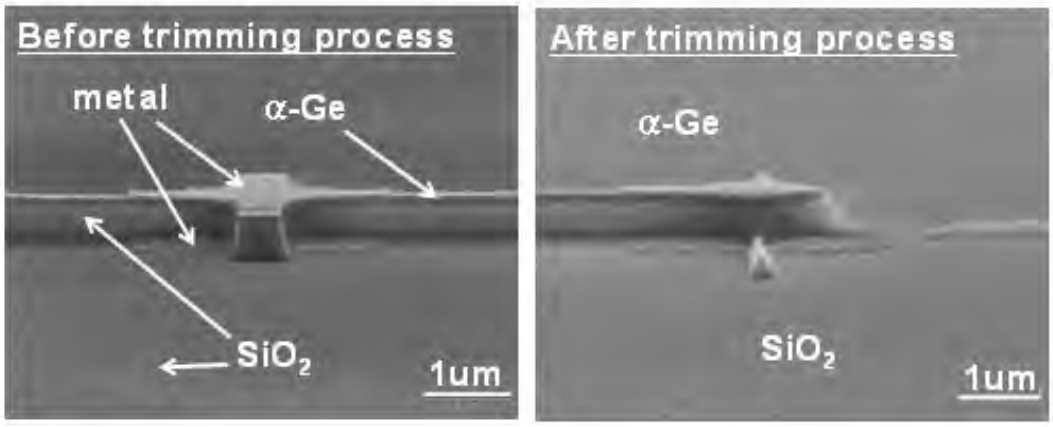

Figure 4.3: Cross view SEM images of the α-Ge thin line structure before and after trimming process [4.7-4.8]

Using these α-Ge line structures/widths, very thin widths were achieved by reducing the dimension of the patterned photo resist lines through isotropic oxygen plasma photo resist trimming process. The samples were subsequently dry-etched down to ~ 0.8 μm depth for a convenient cross-sectional (X) transmission electron microscopy (TEM) analysis. This was in-turn followed by a 5 nm thick Ni or Au seed deposition using an e-beam evaporator. The deposited Ni or Au was patterned using a lift-off process. Figure 4.3 shows side view SEM images of line structures with 5 nm thick Ni seed before and after trimming photo resist.

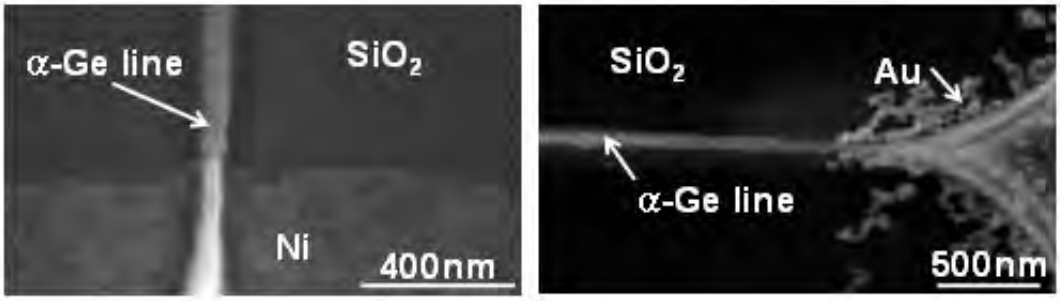

Figure 4.4: Top view SEM images of Ni and Au seeded α-Ge thin line samples [4.7-4.8]

Figure 4.4 shows the top view SEM images of 5 nm thick Ni (left) and Au (right) samples. The isotropic oxygen plasma etch process was done under following conditions; O_2 100 sccm, 500 mT pressure, and 100 W RF power. The measured isotropic etch (or trimming) rate for the photo resist was roughly 40 nm/min. Since width of the lines varies from 550 nm to 900 nm (with 50 nm gap), etching was stopped immediately when one of the lines disappeared, as shown in Figure 4.3. The actual width of the smallest surviving line was 70 nm after the trimming process. 50 nm and 100 nm thick line samples with same width were used to investigate single crystalline Ge growth. The line structure samples are isothermally annealed in a N_2 ambient for 5 hours at 360 ºC based on MILC results of the planar structure samples (Chapter 3). These samples are also analyzed with XTEM images and selective area electron diffraction (SAED) patterns.

4.2 Results and discussion

Ni and Au MILC growth technique was applied to obtain a single crystalline Ge line (100 nm thick and 70 nm wide). The starting material is α-Ge line (Figure 4.2, top) on SiO_2 and the crystallization was done at a low temperature of 360 ºC for 5 hours (Figure 4.2, bottom) thereby, obtaining a 3D-compatible process for creating GeOI virtual substrate. The idea is to achieve a single crystalline Ge by having a grain size larger than the line dimensions, and to propagate a single grain laterally through a narrow α-Ge line. By using TEM and observing no change in sheet resistance, it was

confirmed that no self-nucleation was observed in a control sample even after 5 hours of annealing at 360 °C.

Figure 4.5 shows that ~ 1.33 μm length lateral crystal growth was observed at 360 ºC using Ni MILC. Confining dimension seems to cause the reduction of MILC rate as the MILC rate (~0.27 μm/hr) on this α-Ge line structure is much slower than the rate (~ 2 μm/hr) on the planar structure. The crystallized line sample at 360 ºC, especially the interface between poly and α-Ge was carefully observed in Figure 4.5 using a bright field high resolution (HR) TEM image and SAED patterns. There was clearly a growth competition between several grains to extend the size of the crystals near the Ni MILC seed region (C region in Figure 4.5, poly-Ge SAED pattern). Eventually, one or two selected grains won out and grew to ~ 150 nm length (B region in Figure 4.5, poly-Ge SAED pattern). The grain size grown by Ni MILC was comparable to ~ 70-90 nm, which was slightly smaller than thickness of the α-Ge line. The SAED patterns in Figure 4.5 respectively indicate poly-crystalline and amorphous Ge by MILC and α-Ge regions. The reason why a half of the SAED images were blocked is that special XTEM sample preparation technique was used.

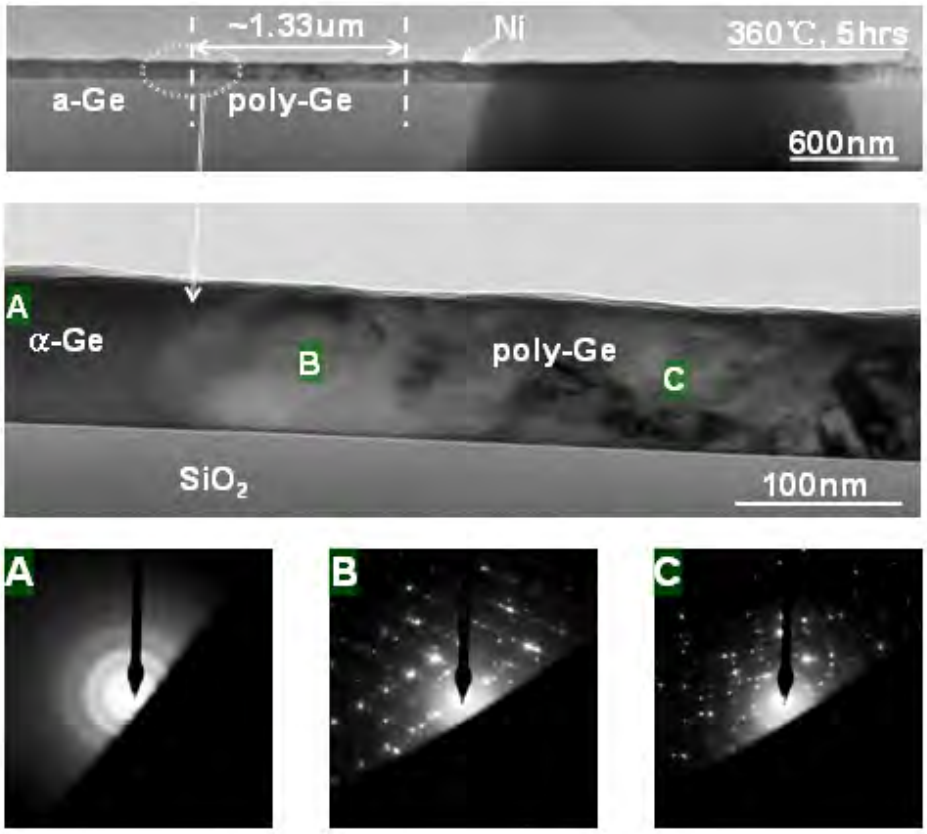

Figure 4.5: Bright field XTEM images and SAED patterns of Ni MILC growth on 100 nm thick and 70 nm wide α-Ge line sample after annealing for 5 hours at 360 ºC [4.7-4.8]

The α-Ge line structures with 5 nm Au seed were also annealed for 5 hours at 360 ºC. In this case (Figure 4.6) fully single crystal line was not obtained, as the grain size (~ 90 nm) was smaller than the line dimensions (100 nm thick and 70 nm wide) like the previous Ni MILC experiment. At the region near Au seed, several small grains existed just as the case of Ni MILC. However, a grain with only ~ 90 nm size was seen to grow as the time went by. Figure 4.6 exhibits ~ 0.472 μm lateral growth by Au MILC after annealing for 5 hours at 360 ºC, yielding a growth rate of ~ 0.09 μm/hr which is slower than the rate (~ 1.09 μm/hr) of Au MILC on planar structure. The reason why MILC growth speed reduced as dimension scaled down is becuase small dimension size prevented metals or germanides from diffusing through the structure when the diffusion direction was toward to the surface of lines.

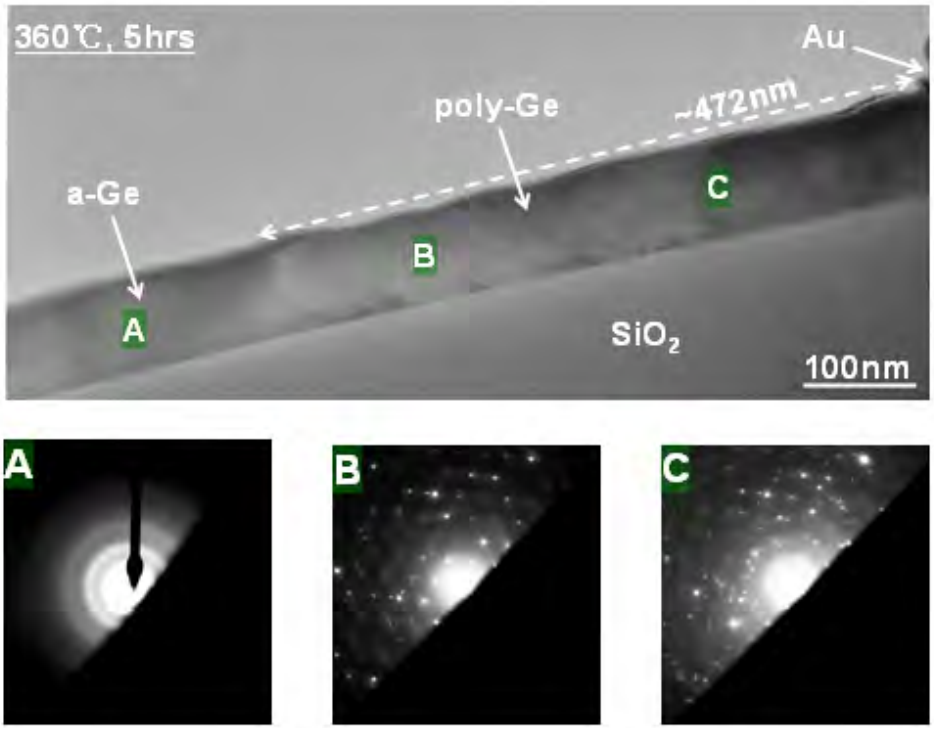

Figure 4.6: Bright field XTEM images and SAED patterns of Au MILC growth on 100 nm thick and 70 nm wide α-Ge line sample after annealing for 5 hours at 360 ºC [4.8]

In a subsequent experiment, Ni seed is selected (as smaller grain sizes were observed than Au MILC) and α-Ge line thickness is reduced to only 50 nm, in order to increase probability to obtain a fully single crystallized Ge line (as the grain sizes in the previous Ni MILC experiment were ~ 70-90 nm which was larger than the width of line structure). Figure 4.7 shows the bright field HRTEM images of the interface between single-Ge and α-Ge in this sample. Fully single crystal Ge regions with roughly 150 nm length were obtained after annealing for 5 hours at 360 ºC.

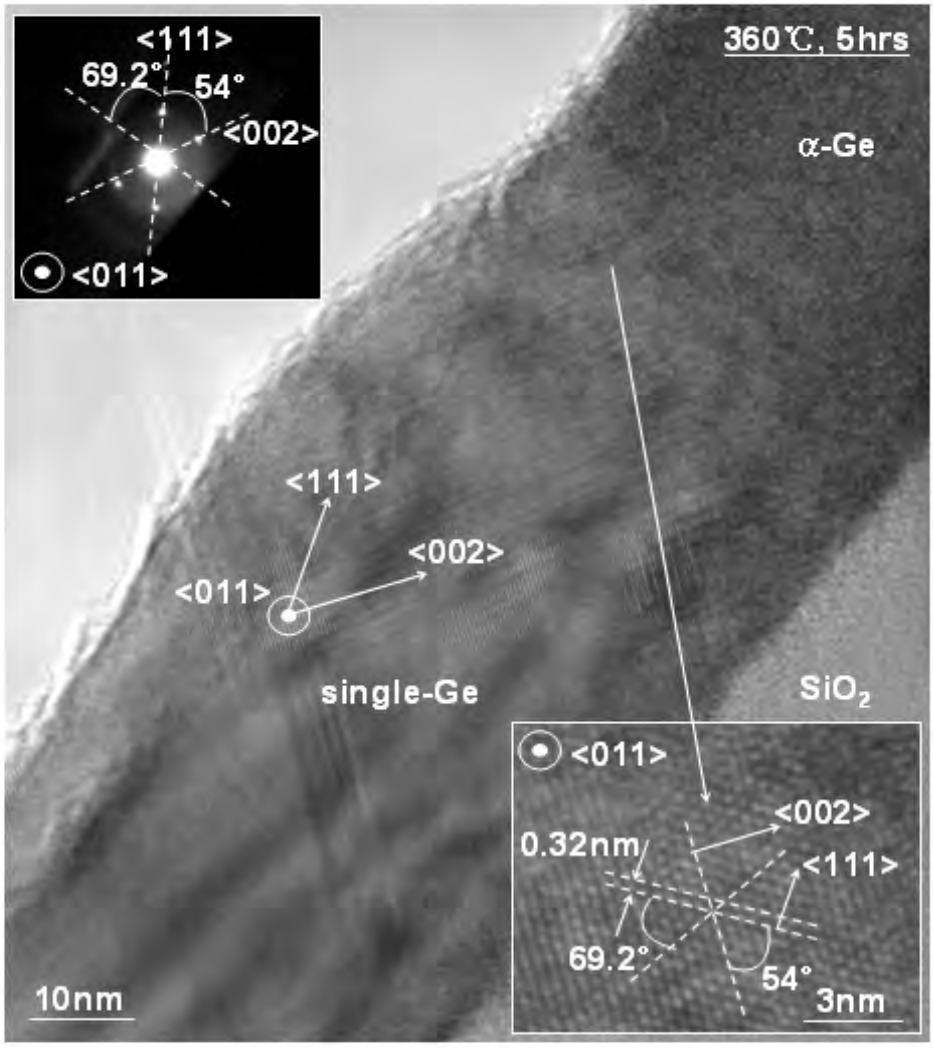

Figure 4.7: Bright field XTEM, HR XTEM images, and SAED patterns of Ni MILC growth on 50 nm thick and 70 nm wide α-Ge line sample after annealing for 5 hours at 360 ºC [4.7-4.8]

Further, the Ni MILC growth rate (~ 0.05 μm/hr) on 50 nm thick and 70 nm wide α-Ge line was found to be lower than the one on the 100 nm α-Ge line thickness with 70 nm width (~ 0.27 μm/hr with 5 nm Ni and ~ 0.09 μm/hr with 5 nm Au), as shown in Table 4.1. Decreasing line dimension causes reduction of MILC growth rate, as seen in sample #1 #2, and #3 (for Ni MILC) and in sample #4 and #5 (for Au MILC). In addition, the rate of Au MILC growth is roughly two and three times slower in

plane (sample #1 and #4) and 100nm thick line (sample #2 and #5) structures, respectively, than Ni MILC at the same condition.

Sample No.	1	2	3	4	5
Metal	5nm Ni			5nm Au	
Structure	Plane	Line	Line	Plane	Line
Thickness (nm)	100	100	50	100	100
Width (nm)	–	70	70	–	70
Lateral crystal growth rate (μm/h)	2.00	0.27	0.05	1.09	0.09

Table 4.1: Summary table; MILC growth rates on α-Ge planar and thin line structure samples with 5 nm thick Ni or Au seed at 360 ºC [4.8]

4.3 Summary

Single crystal growth process on nano-scale (50 nm thick and 70 nm wide using Ni MILC) α-Ge line on insulating substrate at a very low temperature (360 ºC) has been demonstrated. Although single crystal result in our work was obtained at ~ 360 ºC (which is closed to the maximum self-nucleation free MILC temperature, 380 ºC), it is possible to achieve single crystal growth by Ni MILC at below 360 ºC by increasing the annealing time. Pd and Cu are also good candidates for MILC at the self-nucleation free temperature range (≤ 380 ºC), since these metals have (1) very low sintering temperatures needed to form germanide with Ge [4.9] and (2) very high diffusivity in Ge [4.10]. Ge crystallized by Au is expected to yield a higher carrier lifetime, thus a lower leakage current, than Ge crystallized by Ni because Au traps are farther away from the intrinsic energy level in Ge than the Ni traps [4.11]. Despite of higher crystallization temperature (356 ~ 360 ºC) than Ni MILC, Au is another viable candidate to obtain single crystal Ge using MILC growth technique because of its better trap location in Ge energy band. The obtained single crystal Ge by Au MILC and Ni MILC can be used as the channel region for the upper layer devices for 3D ICs, as well as for high performance thin film transistors (TFTs).

4.4 References

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Chapter 5

Low temperature metal induced dopant activation (MIDA) using metal induced crystallization (MIC) technique

A critical aspect currently plaguing the integration of the second (or higher) level devices for 3D-ICs is the lack of dopant (boron = B and phosphorus = P) activation techniques at below 400 ºC. In general, the dopant activation in amorphous (α)-Ge occurs in conjunction with crystallization of α-Ge, where dopants are rearranged and activated (Figure 5.1). It was previously mentioned that α-Ge self-nucleation process started at around 380 ºC and crystallization process was completed at above 450 ºC with 1 hour annealing. Also, dopant activation process for gate, source, and drain formations should be performed at above 450 ºC for complete dopant activation, where fully crystallized Ge film has maximized crystal grains size. However, this annealing temperature (450 ºC) is still too high for second (or higher) level device fabrication in 3D-ICs.

In this chapter, 3D-ICs compatible, low temperature dopant activation process in Ge is introduced, featuring metal-induced crystallization (MIC) technique. In the past, Joshi *et al.* [5.1-5.2] and Lee *et al.* [5.3] demonstrated low temperature activation of dopants in α-Si using the MIC technique with nickel (Ni). However, the processing temperature was at 500 ºC, which does not satisfy the thermal requirement (≤ 400 ºC) for monolithic 3D-ICs. Here, MIC technique for Ge is utilized in order to decrease the dopant activation temperature down to 400 ºC (or less). Using resistivity measurement, transmission electron microscopy (TEM), and x-ray diffraction (XRD) measurement,

the mechanism of the low temperature dopant activation process is investigated on α-Ge by MIC technique, named metal-induced dopant activation (MIDA). In order to avoid dopant activation effect by self-nucleation (or self-crystallization) process occurring at ≥ 380 ºC, maximum temperature limit is restricted from 400 ºC to 360 ºC.

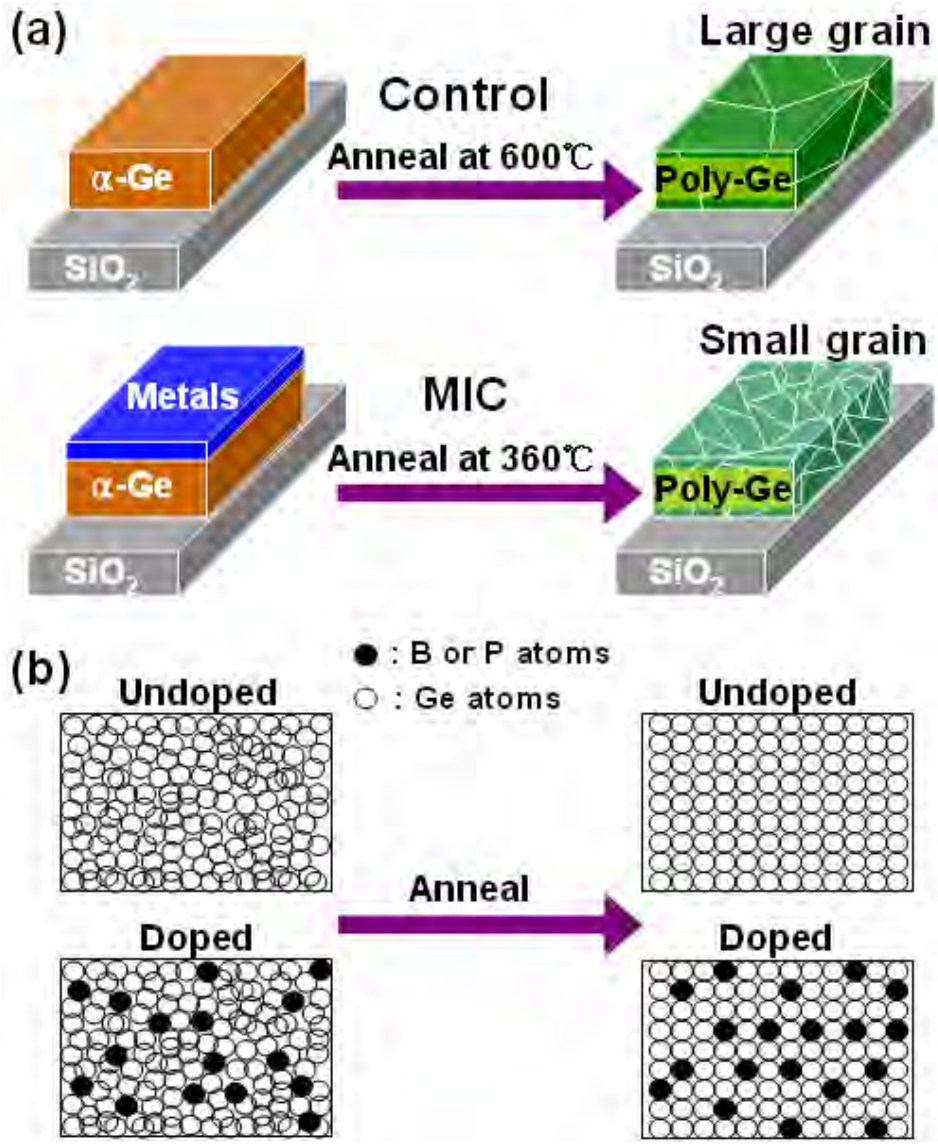

Figure 5.1: Schematics describing (a) relative size of Ge crystal grains and (b) B, P, and Ge atoms in the grains of control and MIC samples before and after the annealing processes (at 600 ºC for control samples and at 360 ºC for MIC samples)

As shown in Figure 5.1, B and P atoms in α-Ge film are rearranged and activated at low temperatures (≤ 360 ºC) during the MIC process, similar to dopant activation mechanism by thermal annealing process. Figure 5.1 describes (a) relative size of Ge crystal grains and (b) B, P, and Ge atoms of control and MIC samples before and after the annealing processes.

5.1 Experiment

100 nm and 200 nm thick α-Ge films are deposited at 300 ºC in a low pressure chemical vapor deposition (LPCVD) furnace on a thermally grown silicon dioxide (SiO_2) film located above a Si wafer. Three types of α-Ge films, p-type, n-type each implanted with B ($^{49}BF_2$, 40 keV, 4e15 cm^{-2}) and P (P_{31}, 90 keV, 4e15 cm^{-2}) ions, and undoped samples were prepared to investigate the dopant activation process. Both undoped and doped control samples were annealed for 1 minute at 600 ºC for the purpose of resistivity measurement and XRD analysis. Five metal candidates (Pd, Cu, Ni, Au, and Co) based on our desired temperature range (≤ 360 ºC) where dopant activation by self-nucleation (or self-crystallization) process ceases to exist as mentioned on Chapter 3 are pre-selected for this experiment. The selected metals (5 nm) were then deposited on 100 nm & 200 nm thick undoped and doped Ge films, and the samples were isothermally annealed in a N_2 ambient at 360 ºC for 1 hour (1.5 or 3 hours for Co) in order to confirm dopant activation by MIC process. The annealed samples were then analyzed by resistivity measurement and XRD systems.

5.2 Results and discussion

Before migrating from the MIC to this MIDA experiment, there are two points that are worth mentioning; (1) Co-MIC process fully crystallizes 200 nm thick α-Ge film at 360 ºC when the annealing time is increased up to 3 hours (Figure 5.2) and (2) size of Ge crystal grains obtained by the MIC processes is independent on the doping type of Ge films (Figure 5.3).

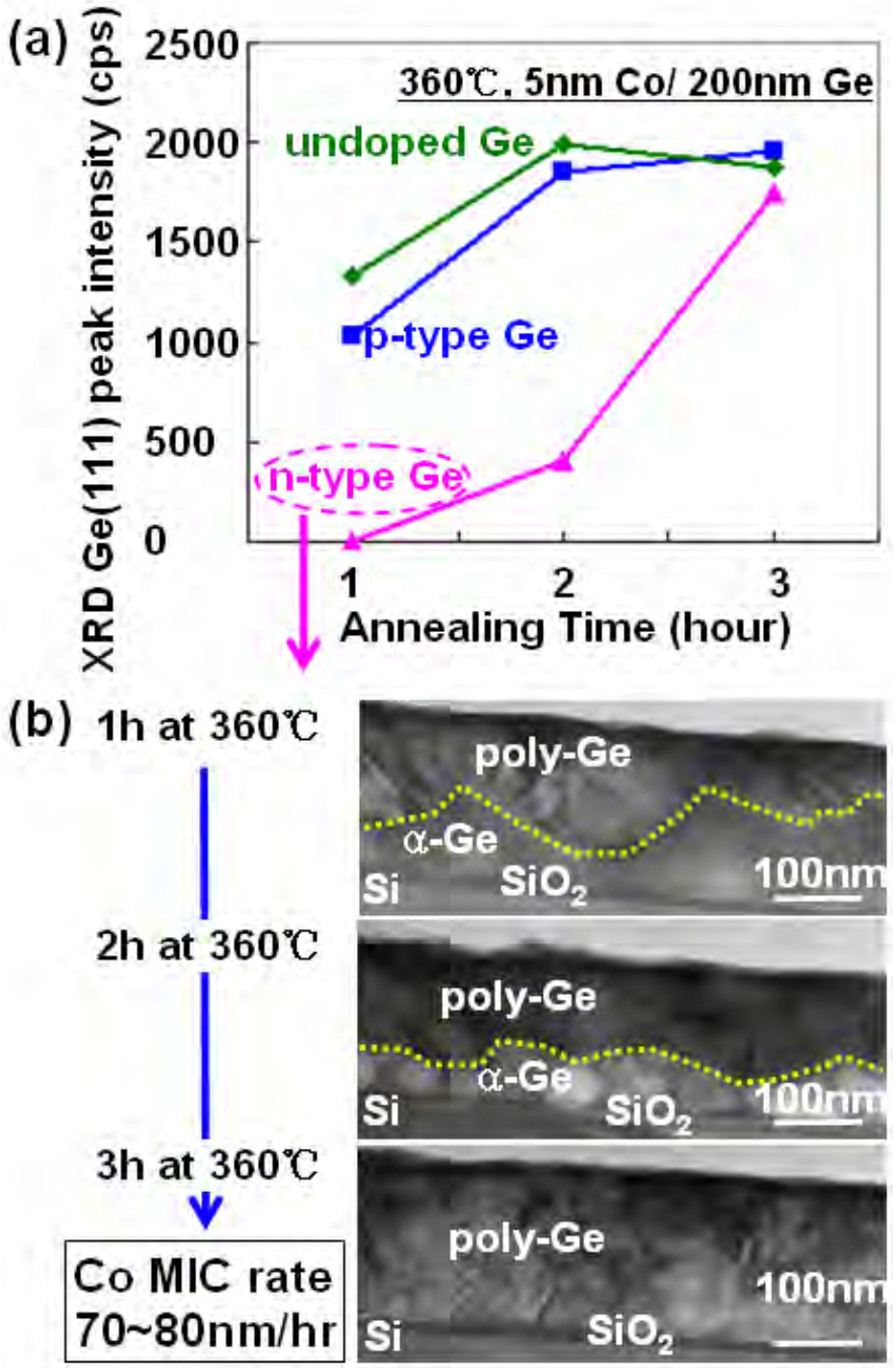

Figure 5.2: (a) XRD Ge (111) peak intensities of three types (p-type (B doped), n-type (P doped), and undoped) of the 200 nm thick Ge films (with 5 nm Co) as a function of annealing time at 360 ºC (b) cross sectional bright field TEM images of 200 nm thick n-type Ge films with 5 nm Co annealed at 360 ºC for 1, 2, and 3 hours [5.4]

Figure 5.2 shows the XRD Ge (111) peak intensity as a function of annealing time in the three types of Ge films (p-type , n-type, and undoped). Because a higher XRD peak intensity is measured in Ge films with a thicker crystallized region on the assumption that grain size is not changed, Co-MIC speed (or rate) can roughly be estimated from these graphs. As a result, 200 nm thick n-type α-Ge film was found to be crystallized with a Co diffusion rate of ~ 70-80 nm/h, shown in Figure 5.2 (b). Although Co diffusion rates (≥ 100 nm/hr) in p-type and undoped Ge films were faster than n-type Ge, a slightly lower Co diffusion rate was also observed in p-type compared undoped Ge films (Figure 5.2). Thus, the existence of dopants in α-Ge seems to suppress the diffusion of Co and consequently the Co-MIC process. The same diffusion behavior depending on dopants was previously reported with Cu in Ge by Hall *et al* [5.5]. The Ge (111) peaks in Co-MIC samples increased and saturated (full crystallization) after annealing for 2 hours (undoped and p-type α-Ge) and 3 hours (n-type α-Ge).

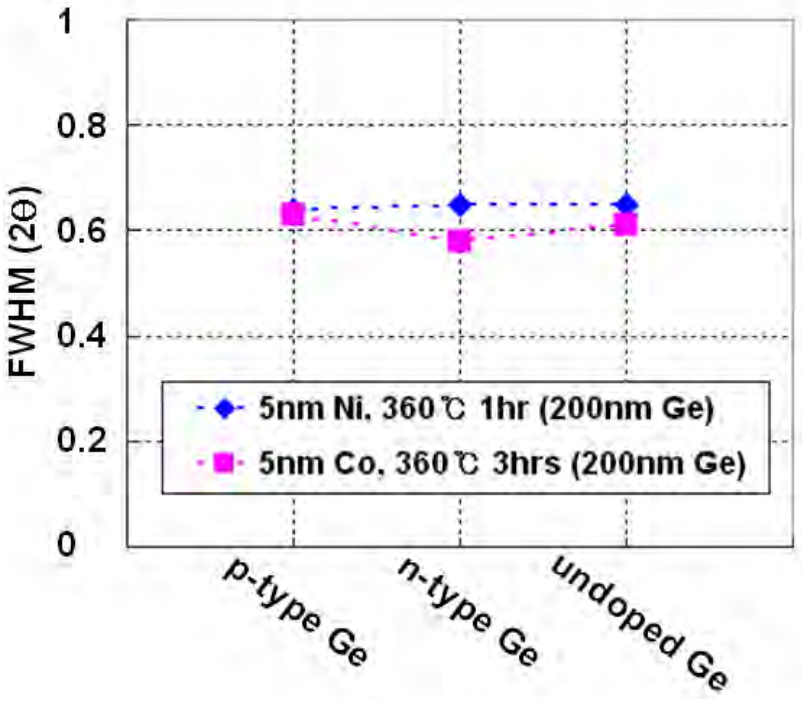

Figure 5.3: FWHM data extracted from Ge (111) peaks of three types of 200 nm thick Ge samples annealed at 360 ºC (Ni-MIC) for 1 hour with 5 nm Ni and (Co-MIC) for 3 hours with 5 nm Co

Next, FWHM data obtained from the three types of Ge films crystallized by Ni- and Co-MIC processes at 360 ºC are investigated, in order to confirm the independency of crystal grain size to the Ge films type (Figure 5.3). Looking at the results, it is observed that FWHM values are almost same in both Ni- and Co-MIC samples. Although, there is a ± 1.5 % difference in Co-MIC samples, it can be neglected considering the measurement or process variation. Therefore, Ge crystal grains size formed by MIC processes is rather independent on the types of the Ge films, even though MIC speed (or rate) depends on the film type.

Based on the previous experimental results (Chapter 3), MIC process was again applied to crystallize 100 nm thick three types of α-Ge films, activating dopants (B and P) in the films by depositing five selected metals (5nm each) reacting with α-Ge below 360 ºC. All MIC samples except Co-MIC were annealed in N_2 ambient for 1 hour at 360 ºC, and 2 hours annealing process was done for Co-MIC samples. Then, resistivities and FWHM data were measured from the MIC samples (Figure 5.4).

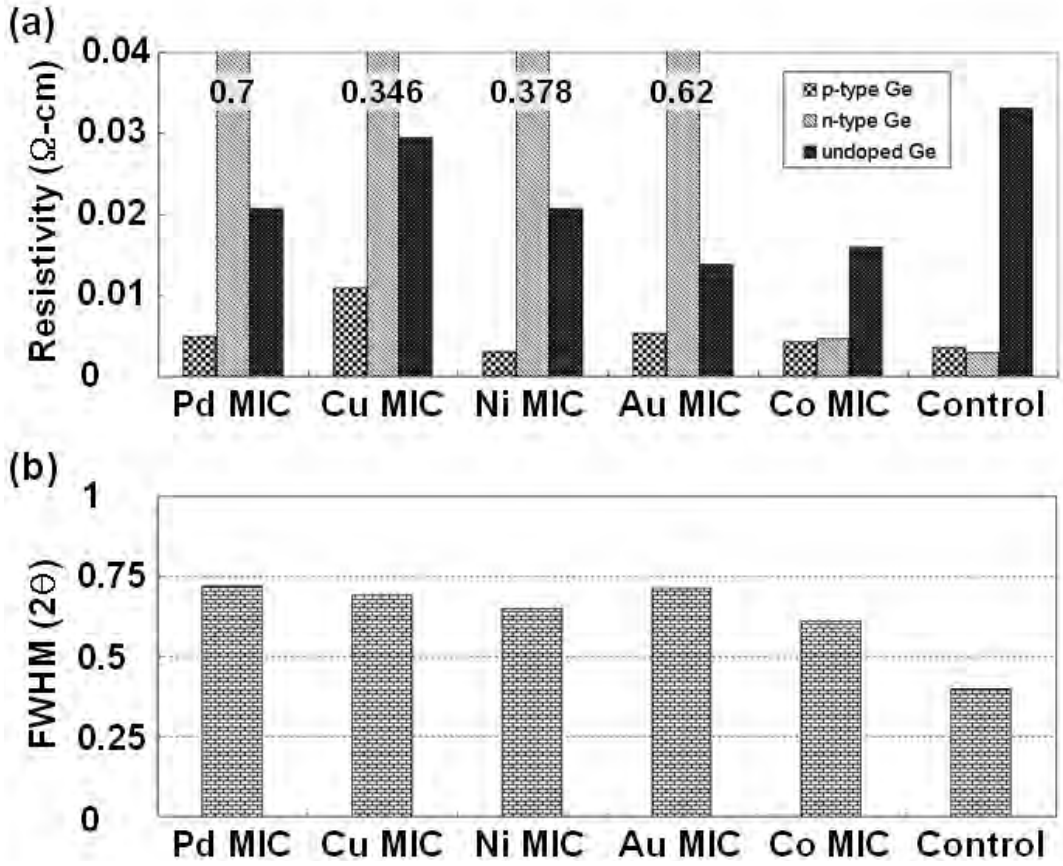

Figure 5.4: (a) Resistivity (Ω-cm) and (b) FWHM data extracted from Ge (111) peaks of 100 nm thick p-type (B doped), n-type (P doped), and undoped Ge films processed by MIC technique with 5nm Pd, Cu, Ni, Au, and Co for 1 hour (2 hours for Co) at 360 ºC and thermally annealed for 1 minute at 600 ºC

Results show that undoped Ge films crystallized by the MIC process have lower resistivities than the control sample, although the MIC samples are expected to have smaller Ge crystal grains size inferred by higher FWHM values. This result is opposite to the fact that poly-crystalline film having smaller crystal grains has a higher film resistivity. This unusual property seems to be a result of metals contributing to a slight reduction in the resistivity. We suggest two possible explanations regarding to this resistivity reduction effect; (1) role of metals as dopants in Ge, and (2) conduction between metals through grain boundary of poly-crystalline Ge. Because solubility of metals in undoped Ge is normally low (~ 10^{15} cm^{-3}), the second explanation is more likely in the case of undoped Ge. However, for doped Ge films, both possibilities need

to be considered, for the solubility of metals in Ge increases up to ~ 10^{19} cm^{-3} (in case of Cu) as dopant concentration increases [5.5].

Full p-type dopant (B) activation through MIC processes in Ge were achieved at 360 ºC, validated by comparing p-type Ge films crystallized by MIC processes to undoped Ge films. Almost all metals tend to work as acceptor-like traps in Ge indicating that these metal traps are not normally effective in p-type Ge films. As shown in Figure 5.5, this is because the metal traps are located above the Fermi level (E_F). These p-type Ge films activated by the MIC processes (except Ni-MIC) have higher resistivities than the p-type control Ge film despite the resistivity reduction effect by metals. Therefore, for these samples the amount of dopants atoms activated by the MIC processes is expected to be lower than the control sample. This agrees with the fact that the MIC samples have smaller Ge crystal grains size because the dopant facilitation probability increases with larger crystal grain formation. Even though Ni-MIC process showed similar resistivity to that of the p-type Ge control film, this Ni-MIC process seems to have a lower amount of activated dopants than the control sample considering the resistivity reduction effect by Ni. However, it is difficult to extract an exact concentration of dopants activated by the MIC processes because the mobility of the poly-crystallized Ge films is not known. This poly-crystalline Ge film mobility depends on the size of Ge crystal grains obtained by the MIC processes and metal impurities mobility in the Ge films.

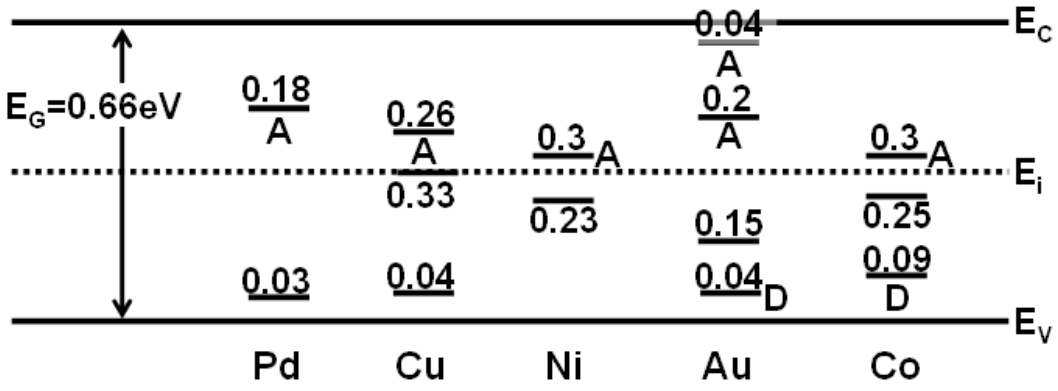

Figure 5.5: Ionization energies for various metal impurities in Ge; Pd, Cu, Ni, Au, and Co [5.6]

Only Co-MIC process succeeded in activating n-type dopant (P) atoms at 360 ºC. We predict that it is because of the compensation process between P atoms and metal atoms working as acceptor-like traps. Pd, Cu, and Ni serve wholly as acceptor-like traps in Ge, but Au and Co can additionally work as another donor-like trap as well as three (for Au) and two (for Co) acceptor-like traps (Figure 5.5). Thus, it is expected that the number of acceptor-like metal (except Co) traps is comparable to the amount of P atoms activated by Pd-, Cu-, Ni-, and Au-MIC processes. However, concentration of the Co traps serving as acceptors is expected to be lower than the number of P atoms facilitated by the Co-MIC process. Two possible explanations to this are (1) Co additionally has one trap serving as donors giving less possibility to work as acceptor-like trpas and (2) Co MIC process activates more dopant (P) atoms due to its bigger grain size, comparing with the other metals.

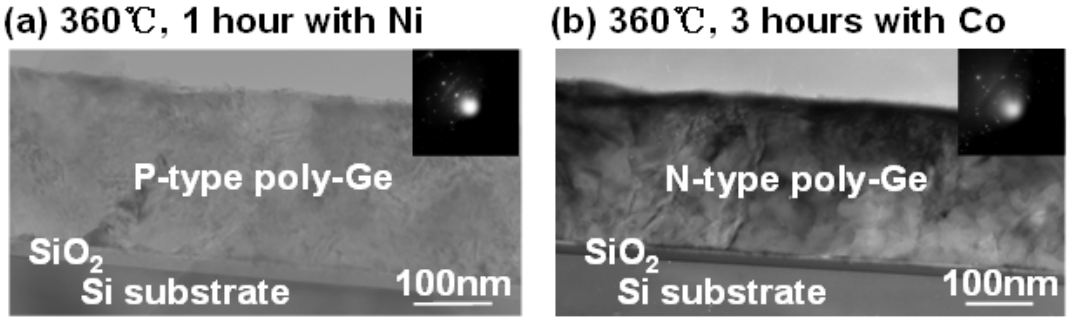

Figure 5.6: Cross sectional TEM images and selective area diffraction patterns; (a) boron-doped Ge film with 5nm Ni annealed at 360 ºC for 1 h, and (b) phosphorus-doped Ge films with 5nm Co annealed at 360 ºC for 3 h, respectively

The low temperature dopant activation technique featuring the Ni and Co-MIC process was demonstrated for a Ge electrode in a Si P-MOSFET using Schottky Ni (or Co) silicide S/D and 20 nm thick gate dielectric (SiO_2) on n-type Si substrate. Ni was selected for the activation of B atoms (p-type) and Co for the activation of P atoms (n-type). Ni and Co silicides were, respectively, used for S/D of the Si P-MOSFETs with p- and n-type Ge gate electrodes because the S/D formation was achieved together with the dopant activation process of a gate electrode at the same time. TEM images in

Figure 5.6 clearly show p- and n-type poly-crystalline Ge gate electrodes crystallized by Ni (Figure 5.6 (a)) and Co (Figure 5.6 (d)) MIC process, respectively.

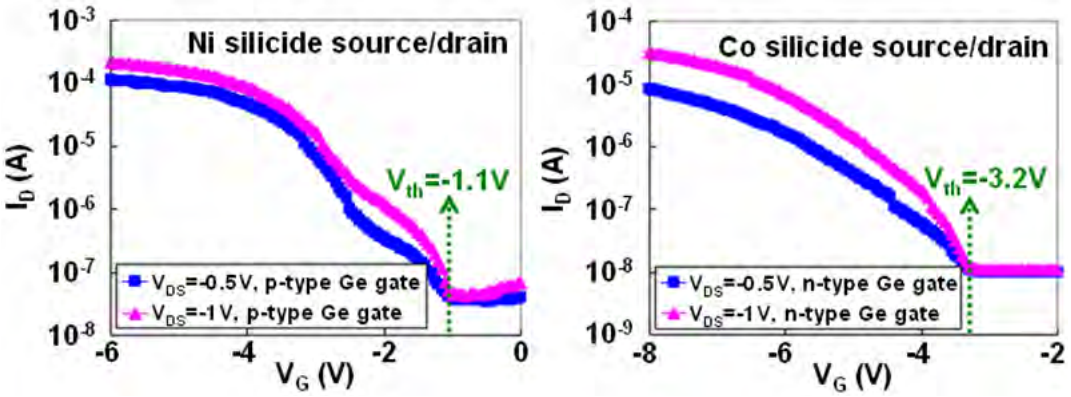

Figure 5.7: I_D-V_G characteristics of p-channel Si MOSFETs with (left) p-type & (right) n-type Ge gate electrodes activated by Ni (and Co) MIC and (left) Ni & (right) Co silicides source/drain formed at 360 ºC

This difference of threshold voltage (V_{th}) is shown in the I_D-V_G characteristics of Si P-MOSFETs with the p- and n-type Ge gate electrodes activated at 360 ºC using Ni and Co, indicating that different dopant (B and P) atoms were successfully activated (Figure 5.7). The Si P-MOSFET with a p-type Ge gate electrode activated by Ni MIC process turns on at around V_{GS}=-1.1V, whereas the Si transistor having a n-type Ge gate electrode by Co MIC process has a turn-on voltage at -3.2V.

5.3 Summary

We have demonstrated 3D-ICs compatible, low temperature (at 360 ºC) dopants activation process in α-Ge featuring the MIC technique. Based on the previous experiment results (Chapter 3), MIC process was applied to crystallize three types (p-type, n-type, undoped) of α-Ge films and ultimately achieve dopant activation in the films. Among the selected metals, Co not only crystallized the α-Ge films at 360 ºC, but it also facilitated B and P atoms in the films. The remaining metals, such as, Pd, Cu, Ni, and Au, only succeeded activating p-type dopant (B) atoms at below 360 ºC

due to compensation problem between n-type dopant (P) atoms and metals. This technique is also promising for integrating Ge transistors at low temperatures (≤ 400 ºC) required by 3D-IC fabrication.

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Chapter 6

Low temperature and high performance germanium CMOS technology with novel source/drain by metal induced dopant activation and metal/high-k/GeO_2 gate stack

Ge CMOS fabrication can be technically separated into two parts; (1) a gate stack and (2) source/drain (S/D) fabrication. Based on several gate stack techniques (channel surface passivation, gate dielectric, and gate electrode) reported to date (refer to Chapter 2), it is not a difficult task to form a gate stack for Ge CMOS at ≤ 400 ºC. Because carrier mobility depends on interface trap density, it is critical to perform ozen [6.1] and plasma oxidation [6.2] methods at ≤ 400 ºC to achieve desirable Ge surface passivation that leads to high Ge CMOS performance. High-K/metal gate stack is a good low temperature combination for a gate dielectric/electrode formation. The metal gate electrode can be replaced by a highly doped poly Ge gate electrode deposited with a diboron treatment technique [6.3] at ≤ 310 ºC. However, S/D annealing has been a challenging issue in Ge CMOS fabrication for monolithic 3D-ICs because the minimum S/D activation temperatures are ~500 ºC for n^+ and ~400 ºC for p^+ S/D [6.4-6.5]. It is difficult to achieve well activated S/D at ≤ 400 ºC in the Ge CMOS fabrication, because low temperature processing will only result in minor dopant activation, which degrades the junction quality. This issue is more severe when fabricating the N-channel Ge MOSFET.

In this chapter, a high performance N and P-channel Ge MOSFETs fabricated below 360 ºC (for N-MOSFET) and 380 ºC (for P-MOSFET) with the novel n^+ and p^+

S/D junctions formed by metal induced dopant activation (MIDA) technique introduced in the Chapter 5 and metal/high-K/GeO_2 gate stack are introduced. This low temperature Ge MOSFET process can be utilized to integrate high performance Ge CMOS devices above interconnect layers for monolithic 3D-ICs without exceeding 400 ºC.

6.1 Experiment

MIDA technique was exploited to form S/D junctions in both N- and P-channel Ge MOSFETs at below 400 ºC for monolithic 3D-ICs application. Combining with a $GeO_2/Al_2O_3/Al$ gate stacking technique, whole process temperature for these MOSFETs fabrication was kept under 400 ºC.

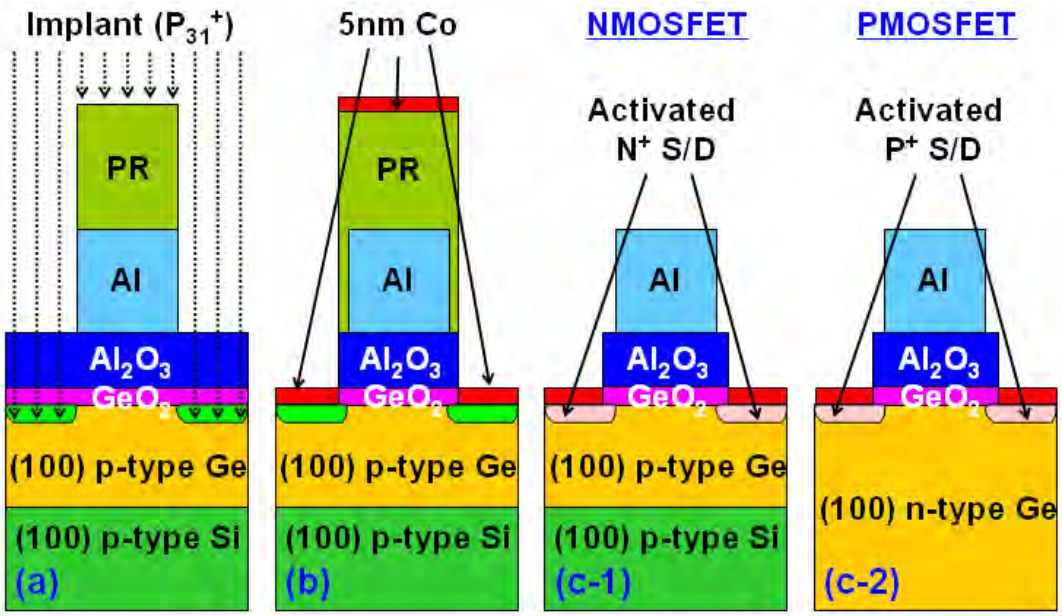

Figure 6.1: N and P-channel Ge MOSFETs fabrication flow with the novel n^+ and p^+ S/D junctions formed by MIDA technique and metal/high-K/GeO_2 gate stack

As shown in Figure 6.1, about 2.3 μm thick single crystalline Ge (undoped Ge; slightly p-type: ~ 5×10^{14} cm^{-3}) film was heteroepitaxially grown on p-type (5×10^{16} cm^{-3}) Si substrate [6.6] for N-channel Ge MOSFET. Light n-type (Sb: ~1×10^{14} cm^{-3}) bulk

Ge wafer was used for P-channel Ge MOSFET. Ge surface was passivated with a GeO_2 interfacial layer, grown by the ozen oxidation method [6.1]. Then, Al_2O_3 layer was deposited at 350 ºC without vacuum break by atomic layer deposition (ALD) system. 200 nm thick aluminum (Al) was sputtered on the Al_2O_3 and was patterned (and wet-etched) to define the gate region (L_G = 100 μm). After implanting phosphorus (P_{31}^+, 18 KeV, and 4×10^{15} cm^{-2}) and boron (BF_2, 20 KeV, and 4×10^{15} cm^{-2}) ions in the n^+ and p^+ S/D regions, photo-resist (PR) was striped in PRX127 at 40 ºC for 20 minutes. Al gate electrode was then covered with 1μm thick patterned PR that is larger by 100 nm in size than the gate, followed by Al_2O_3 wet-etch process in 2 % hydrofluoric acid (HF) for 10 seconds. A 5 nm thick Co film, which successfully activated P and B atoms in Chapter 5, was subsequently deposited over the whole area, and lift-off process was performed to remove the Co film outside of the S/D regions. In order to characterize n^+/p junction activated by MIDA technique, n^+/p junction diode samples are prepared and those were annealed at 360 ºC for 1 and 10 minutes in a rapid thermal annealing (RTA) system. In addition, n^+/p junction control sample without Co film was created by annealing for 1 minute at 600 ºC. The N- and P-MOSFET samples were then respectively annealed at 360 ºC and 380 ºC for 1 minute in a RTA system. Finally, spreading resistance profile (SRP) and secondary ion mass spectrometry (SIMS) analyses on the n^+/p and p^+/n S/D junctions was done, along with I-V characteristic measurements of the junction diodes and the Ge MOSFETs. It should be noted that in the junction diode I-V measurements, the wafer itself acts as a large resistance since measurement was done using top and substrate as contacts. Split C-V measurement was used to extract mobility of inversion carriers in the MOSFET [6.7].

6.2 Results and discussion

The n^+/p junction diode formed on the epi-Ge by MIC technique after annealing for 1 minute at 360 ºC shows the best diode characteristic, the highest on/off ratio (Figure 6.2). For this work, because the control junction diode was not optimized in terms of on/off ratio by varying annealing temperature and time, it is meaningless to

compare the current on/off ratio of this control junction diode to that of other n^+/p junction diodes formed by the MIC process at 360 ºC. Higher forward current densities (~6× in 10 minutes at 360 ºC, and ~3× in 1 minute at 360 ºC annealed samples, compared with the control diode) were obtained by MIC technique with Co, in spite of a low temperature process (360 ºC). Our n^+/p junction diode activated at 360 ºC has a better current on/off ratio (~ 1.1×10^4) than that (~ 2×10^3) of conventional n^+/p junction diode optimized at 500 ºC by Shang *et al* [6.4]. However, the current on/off ratio of the n^+/p junction degraded as annealing time was increased to 10 minutes at 360 ºC (~ $1.1\times10^4 \rightarrow$ ~ 3.7×10^2). Because Co working as recombination centers in Ge was used to induce crystallization and dopant activation at a low temperature, the diode reverse (off) current density was slightly higher than that of the optimized conventional junction diodes. However, high forward/reverse (on/off) current ratio was achieved by increased forward (on) current density in the junctions formed by MIDA technique.

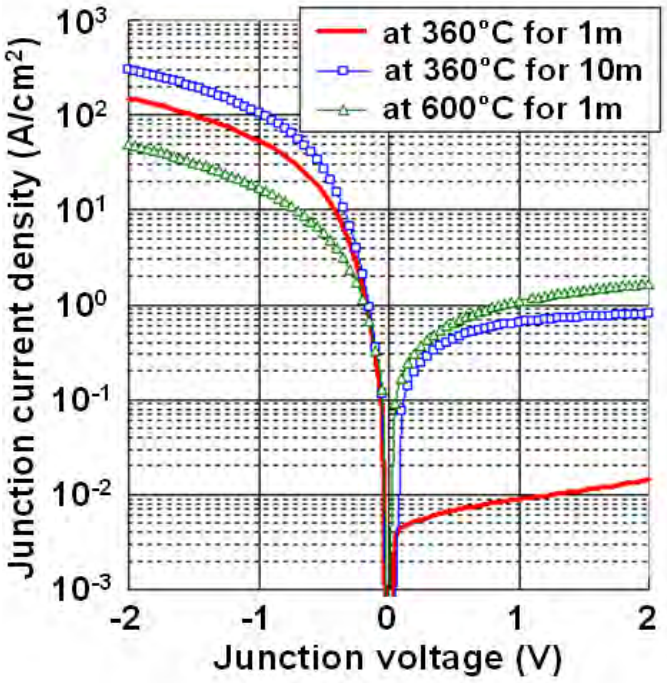

Figure 6.2: n+/p junction current density (A/cm^2) of diodes annealed at 360 ºC for 1 & 10 minutes with Co and at 600 ºC for 1 minute without Co

Figure 6.3 shows SRP and SIMS analyses of the n^+/p junction formed (a) at 360 ºC for 1 minute, (b) at 360 ºC for 10 minutes, and (c) at 600 ºC for 1 minute. As shown in Figure 6.3 (a) and (b), Co diffused into the junction at 360 ºC, triggering the MIC process to re-crystallize the n^+ region and activate P atoms in the region. Higher forward current densities at 360 ºC are the results of a shallower junction depth (~ 100 nm) achieved by Co MIC process compared to the control sample. This is because the low temperature process reduces the diffusion rate of P atoms (shown in SIMS profiles of P atoms in Figure 6.3). In addition, low resistivities of 5.2×10^{-4} Ω-cm and 2.2×10^{-4} Ω-cm (corresponding to 6.3×10^{19} cm^{-3} and 2.7×10^{20} cm^{-3} phosphorus doped Ge) were measured at the surface region of the n^+/p junction in Figure 6.3 (a) and (b) because Co by itself reduces resistivity by forming Co germanide layer as well as activating P atoms after diffusion. As mentioned earlier, the maximum current on/off ratio (~ 1.1×10^4) was achieved after annealing at 360 ºC for 1 minute. In this given condition, much smaller number of active Co recombination centers in Ge is located at the junction region (around 100 nm deep from the surface). The concentrations of Co are about 10^{17} cm^{-3} and 10^{18} cm^{-3} at the 100 nm depth in the samples annealed at 360 ºC for 1 and 10 minutes, respectively.

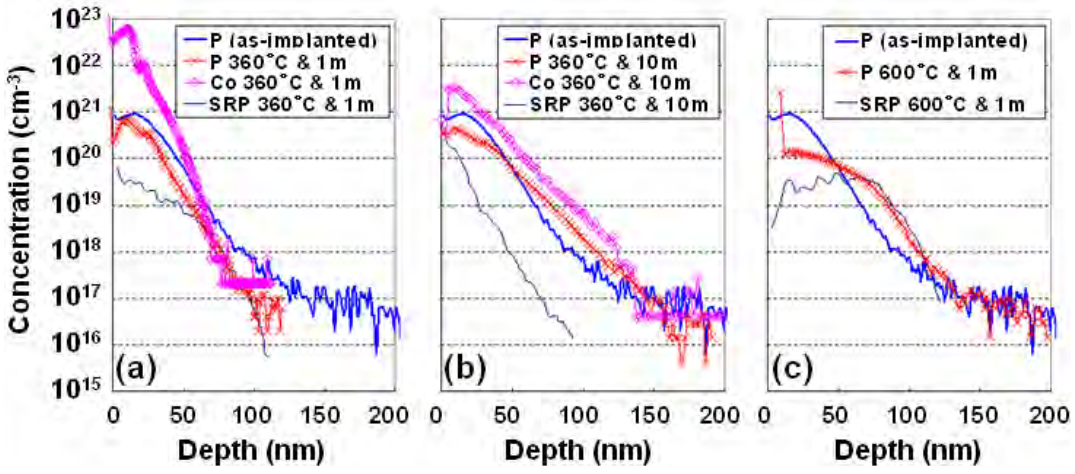

Figure 6.3: Spreading Resistance Profile (SRP) and Secondary Mass Ion Spectrometry (SIMS) of phosphorus and Co in n^+/p junctions annealed (a) & (b) at 360 ºC for 1 & 10 minutes with Co and (c) at 600 ºC for 1 minute without Co

Additionally, it seems that the P atoms diffused slightly after the Co MIC process. Although it is difficult to observe diffusion after annealing for 1 minute at 360 ºC, the diffusion effect was clearly seen in the samples with 10 minute anneal, shown in Figure 6.3 (b). We conclude that Co MIC process also enhanced the diffusion of P atoms which is, however, much slower than that of a normal dopant activation process because of low process temperature. Out-diffusion of P atoms during the activation process was observed not at 360 ºC but at 600 ºC because P atoms were piled up in the unreacted Co layers that are removed in hydrochlorine acid (HCl).

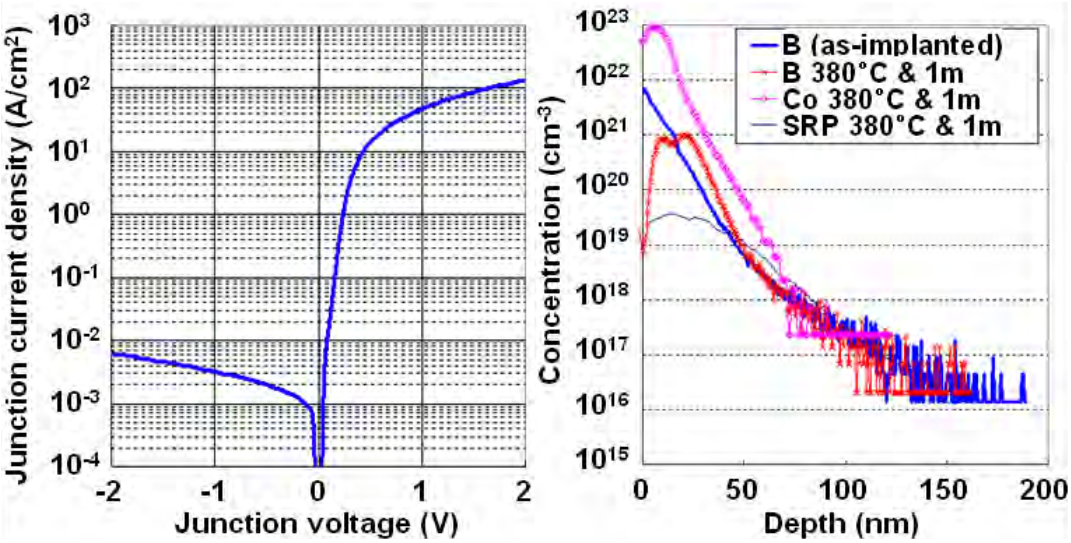

Figure 6.4: (a) diode junction current density (A/cm^2) and (b) SRP & SIMS of boron and Co in the p$^+$/n junction diode annealed at 380 ºC for 1 minute with Co

With the same technique (Co MIDA), the p$^+$/n junction diode was formed on the bulk-Ge substrate after annealing for 1 minute at 380 ºC, and current on/off ratio was measured (Figure 6.4). Our p$^+$/n junction diode has a similar current on/off ratio (~ 1.21×10^4 at |V|=±2V) than that of conventional junction diode optimized at high temperatures, although it was formed by a low temperature process. As the previous n$^+$/p junction, very small amount of active Co recombination centers are located only at the junction interface regions (around 100 nm deep from the surface). The concentrations of Co was about 10^{17} cm^{-3} or less at 100 nm depth in the p$^+$/n sample

annealed at 380 ºC for 1 minute. Besides, we could not observe any segregation effect because B atoms were also piled up in the unreacted Co layer etched finally by HCl.

Figure 6.5 and 6.6 respectively show I_D (μA/μm)-V_G (V) and I_D (μA/μm)-V_D (V) characteristics of N & P-channel Ge MOSFETs fabricated below 360 ºC and 380 ºC with novel S/D junctions formed by Co MIDA technique and GeO_2/Al_2O_3/Al gate stack. The N and P-channel Ge MOSFETs demonstrated a reasonable I_{on}/I_{off} ratio (~1.13×10^3 and ~1.09×10^3, respectively) and fairly high I_{on} per width (~1.4 μA/um and ~1.17 μA/um, respectively) despite being a long channel transistor (L_G = 100 μm). With this Co MIDA technique low I_{on} problem of N-channel Ge MOSFETs due low solubility [6.8] and fast diffusivity [6.9] of n-type dopants in Ge is greatly improved. In Figure 6.5 (a), threshold voltage of the N-channel MOSFET abnormally increased as drain voltage biased from 0.1V to 1.1V, but the P-channel MOSFET did not show any shift of threshold voltage. The interface between Ge surface and gate dielectric (GeO_2+Al_2O_3), not perfectly optimized, seems to trap electron carriers more likely than holes subsequently increasing the threshold voltage of the N-channel MOSFET. In addition, much higher source current (I_S) was observed in the turn-off mode of N-channel MOSFET than P-MOSFET. Measured gate leakage currents were negligibly small compared to source/drain/substrate currents ($I_S/I_D/I_{SUB}$). Thus, it can be concluded that much higher current flows in the N-MOSFET from drain to source thru the interface between hetroepitaxially grown Ge film and Si substrate, where defects by lattice mismatch is dominant, even though the transistor were turned off by sufficiently low gate voltage. On the contrary, the P-MOSFET fabricated on bulk-Ge having almost perfect crystal quality, very low I_S was observed.

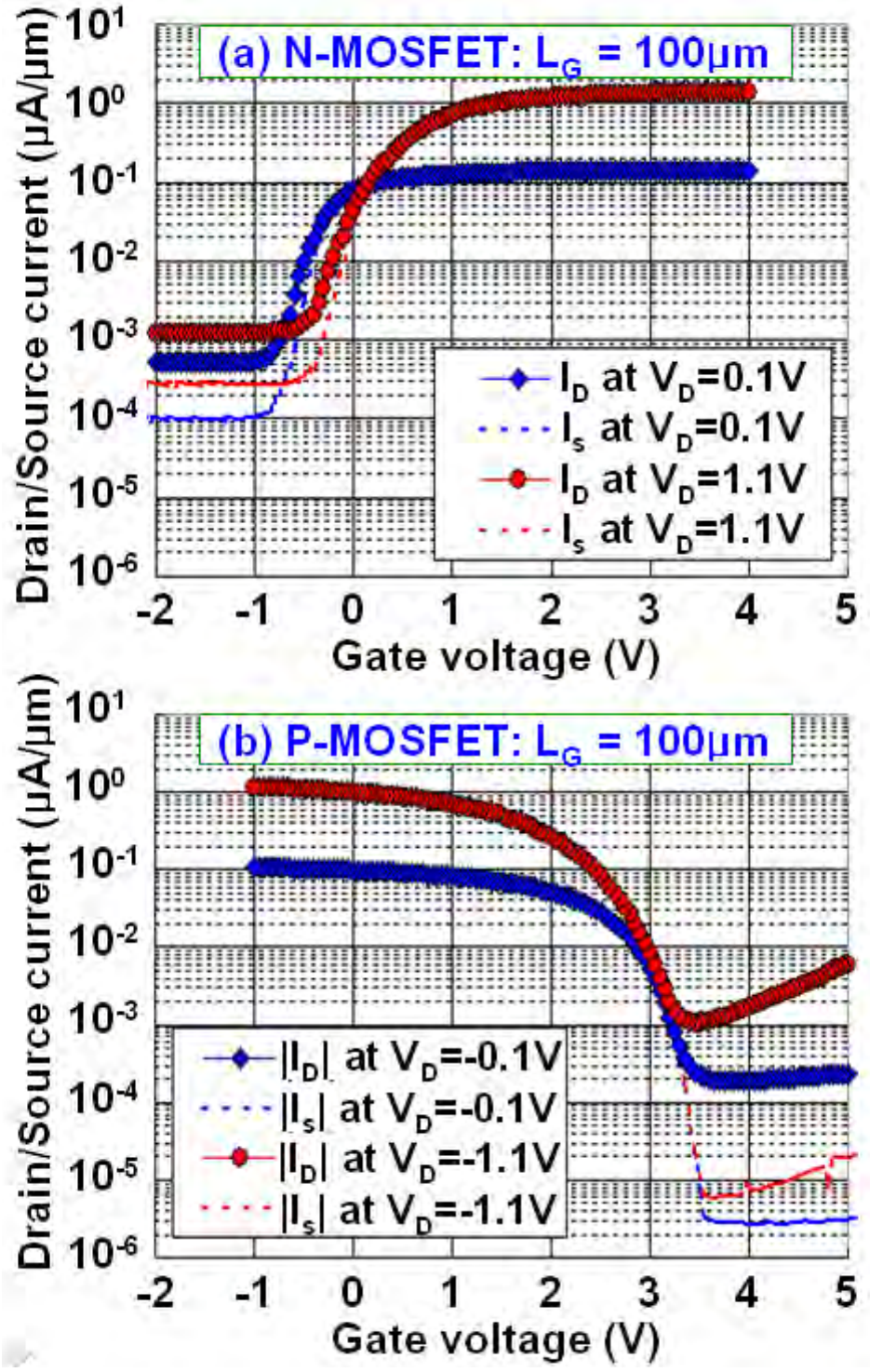

Figure 6.5: I_D I_S (uA/um)-V_G (V) characteristics of N-&P-channel Ge MOSFETs (L_G=100um) at $|V_{DS}|$=0.1 and 1.1V

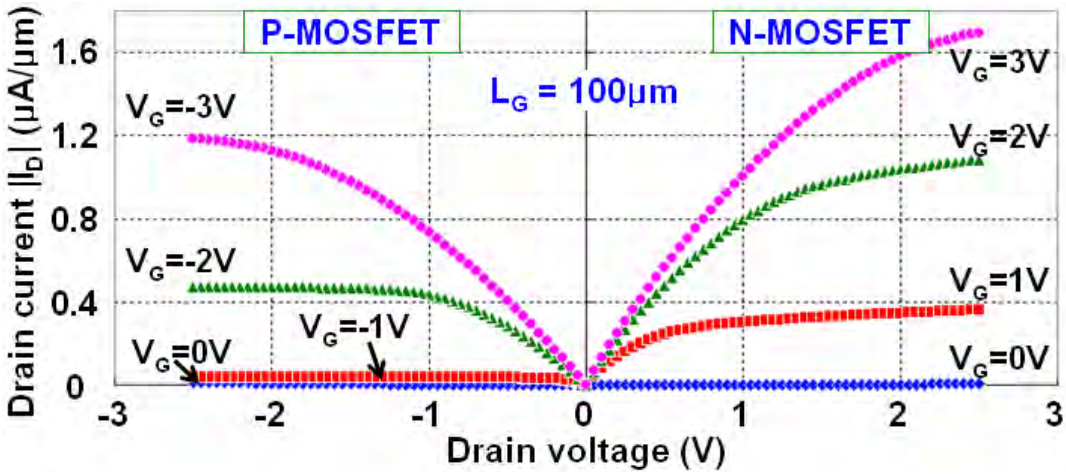

Figure 6.6: I_D (uA/um)-V_D (V) characteristics for N-&P-channel Ge MOSFETs (L_G=100um)

Although the surface passivation process was not optimized in this work, the measured N-channel Ge MOSFET electron mobility (Figure 6.7) was slightly lower than the highest reported on (100) Ge mobility to-date even when compared to a high temperature process (GeO_xN_y) [6.10]. Hole mobility in P-channel Ge MOSFET was similar to the highest reported.

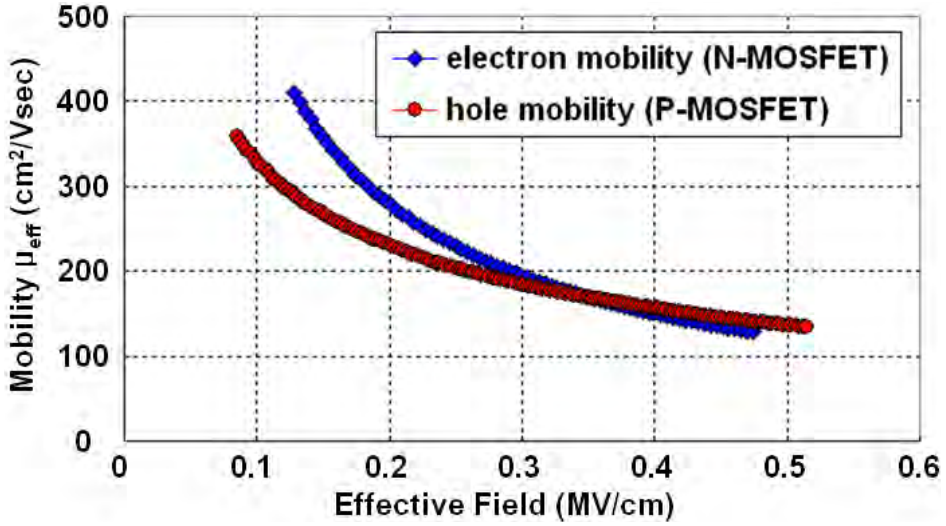

Figure 6.7: Electron and hole mobility (cm^2/Vsec) as a function of effective field (MV/cm) in N-&P-channel Ge n-MOSFETs

6.3 Summary

Ge n^+/p & p^+/n junction diodes and N & P-channel MOSFETs with an $Al/Al_2O_3/GeO_2$ gate stack and novel S/D junctions formed at below 360 ºC and 380 ºC using Co MIDA technique has been demonstrated and analyzed. Excellent diode and transistor on/off ratios were obtained in N & P-channel Ge MOSFETs. Especially, high series resistivity problem in the S/D region of Ge N-MOSFETs was improved, suggested by high I_{on} current (~1.4 μA/μm at L_G = 100 μm). This low temperature Ge CMOS process is promising for integrating Ge transistors at below 400 ºC required by monolithic 3D-ICs fabrication.

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Chapter 7

Conclusion

In this dissertation, low temperature Ge CMOS processes based on MIC/MILC technique for monolithic 3D-ICs application have been discussed in detail. Main contributions of this work are described below.

7.1 Contributions

In this section, three significant sets of experiments will be described and discussed in turn; (1) Self-nucleation, (2) MIC, and (3) MILC on α-Ge planar structures.

7.1.1 MIC/MILC of α-Ge

1. Self-nucleation (or crystallization) of α-Ge was extensively investigated with TEM and XRD systems, in order to find the optimal temperature range (≤ 380 ºC) where MIC/MILC process was not overshadowed by the self-nucleation.
2. With eight metals, Pd, Cu, Ni, Au, Co, Al, Pt, and Ti, MIC process was investigated and analyzed in detail as a function of annealing temperature between 300 ºC and 450 ºC on α-Ge. Five metals,Pd, Cu, Ni, Au, and Co that do not exceed our thermal budget (≤ 380 ºC) in MIC process were selected for the subsequent experiments.
3. Ni and Au MILC growth at 360 ºC was analyzed on plane α-Ge films by TEM, and their Ge crystal grain size was confirmed by high resolution TEM analysis.

7.1.2 Single crystalline GeOI growth using MILC

1. Single crystal growth process was demonstrated on nano-scale (50 nm thick and 70 nm wide) α-Ge line on an insulating substrate at a very low temperature (360 ºC) using Ni and Au MILC technique.

2. It was confirmed that MILC growth rate was related to the dimension (thickness and width) of α-Ge line as well as the kind of metal.

7.1.3 Low temperature MIDA process using MIC technique

1. Relationship between the kind of dopant atoms in α-Ge and MIC growth rate (and grain size of crystals formed by the MIC) was established.

2. With the previously chosen five metals, MIDA process was investigated and analyzed to understand the mechanisms by performing resistivitiy measurements and XRD analysis.

7.1.4 Low temperature and high performance Ge CMOS with novel S/D by MIDA and a metal/high-k/GeO_2 gate stack

1. High performance Ge n^+/p & p^+/n junction diodes and N & P-channel MOSFETs with an $Al/Al_2O_3/GeO_2$ gate stack and novel S/D junctions formed at below 360 ºC using Co MIDA technique was demonstrated and analyzed.

2. High series resistivity problem in the S/D region of Ge N-MOSFETs was improved, indicated by high I_{on} current (~1.4 μA/μm at L_G = 100 μm).

7.2 Recommendations for future work

In this dissertation, several low temperature Ge CMOS processes based on the MIC/MILC technique were developed and studied to fabricate Ge MOSFETs on top of the interconnect layers at below 400 ºC for monolithic 3D-ICs. However, a lot of work still needs to be done in order to improve the Ge MOSFETs' performance. In the case of low temperature (≤ 360 ºC) single crystalline GeOI growth process using the

MILC technique described in Chapter 4, additional analysis (e.g. SMIS) on the concentration of metals left in the single crystalline Ge region after MILC process is required, in order to utilize the Ge film for the channel region of the upper layer Ge MOSFETs. Keeping the lowest concentration of metals in the crystallized Ge region is the most important point to improve transistor performance while reducing leakage current density and increasing mobility.

In Chapter 5, MIDA process featuring the MIC technique was systematically investigated with the selected 5 nm thick metals (Pd, Cu, Ni, Au, and Co) reacting with Ge well at our thermal budget ($\leq$ 380 ºC). However, high concentration of metals incorporated in the Ge films during this MIDA process affects the dopant activation process by increasing number of heterogeneous nuclei, which decreases the grain size, finally reducing dopant activation rate. Besides, the existence of metal traps in Ge decreases the number of activated dopant atoms by compensation while increasing the leakage current density by working as recombination centers in Ge junctions. Here, several ways of reducing the supplied metal concentration during this MIDA process is suggested to avoid the above negative effects; (1) two step MIC process, (2) implantation of metal ions, and (3) MIDA using MILC (not MIC). First, doped α-Ge samples with a thin metal cap are annealed at around 300 ºC to form very thin (a few monolayer) germanide layer, and then, after selectively etching unreacted metal, it is annealed again at 360 ºC to crystallize the doped α-Ge region. As a result, metal concentration will be dramatically reduced. Second, we can control the concentration of metals by implanting metal ions needed for MIDA process. Finally, grain size and dopant activation rate can be increased by applying MILC technique for MIDA process, because it will cause much less metals that can laterally diffuse (concept of flux).

Another interesting extension of this dissertation would be to fabricate Ge MOSFETs using low temperature Ge CMOS processes (introduced in Chapter 6) on the GeOI structure formed by MILC process (Chapter 4). Overall, these improvements can be proved promising for realization of monolithic 3D-ICs.

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