NANO-SCALE ZIRCONIA AND HAFNIA DIELECTRICS GROWN BY ATOMIC LAYER DEPOSITION: CRYSTALLINITY, INTERFACE STRUCTURES AND ELECTRICAL PROPERTIES

A DISSERTATION
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Abstract

With the continued scaling of high speed transistors, leakage current densities across the SiO_2 gate dielectric have increased enormously through direct tunneling. Presently, metal oxides having higher dielectric constants than SiO_2 are being investigated to reduce the leakage current by increasing the physical thickness of the dielectric. Many possible techniques exist for depositing high-κ gate dielectrics. Atomic layer deposition (ALD) has drawn attention as a method for preparing ultrathin metal oxide layers with excellent electrical characteristics and near-perfect film conformality due to the layer-by-layer nature of the deposition mechanism.

For this research, an ALD system using $ZrCl_4$/$HfCl_4$ and H_2O was built and optimized. The microstructural and electrical properties of ALD-ZrO_2 and HfO_2 grown on SiO_2/Si substrates were investigated and compared using various characterization tools. In particular, the crystallization kinetics of amorphous ALD-HfO_2 films were studied using *in-situ* annealing experiments in a TEM. The effect of crystallization on the electrical properties of ALD-HfO_2 was also investigated using various *in-situ* and *ex-situ* post-deposition anneals. Our results revealed that crystallization had little effect on the magnitude of the gate leakage current or on the conduction mechanisms.

Building upon the results for each metal oxide separately, more advanced investigations were made. Several nanolaminate structures using ZrO_2 and HfO_2 with different sequences and layer thicknesses were characterized. The effects of the starting microstructure on the microstructural evolution of nanolaminate stacks were studied. Additionally, a promising new approach for engineering the thickness of the SiO_2-based interface layer between the metal oxide and silicon substrate *after* deposition of the metal oxide layer was suggested. Through experimental measurements and thermodynamic

analysis, it is shown that a Ti overlayer, which exhibits a very high oxygen solubility, can effectively getter oxygen from the interface layer, thus decomposing SiO_2 and reducing the interface layer thickness in a controllable fashion.

As one of several possible applications, ALD-ZrO_2 and HfO_2 gate dielectric films were deposited on Ge (001) substrates with different surface passivations. After extensive characterization using various microstructural, electrical, and chemical analyses, excellent MOS electrical properties of high-κ gate dielectrics on Ge were successfully demonstrated with optimized surface nitridation of the Ge substrates.

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Chapter 1

Introduction to High-κ Gate Dielectrics

1.1 Introduction

After invention of the discrete bipolar transistor in 1947, [1] the Si-based microelectronics industry rapidly expanded for decades with the advent of complementary metal-oxide-semiconductor (CMOS) integrated circuit technology in the early 1960's.[2] Among many developed device concepts, the field effect transistor (FET), based on the metal-oxide-semiconductor (MOS) capacitor has dominated the microelectronics market. It has enabled dramatic increases in device performance and the "scalability" needed to reduce the device dimensions. The basic active MOSFET device is composed of a source and drain used to inject and receive the charge carriers flowing through channel region under the MOS gate stack, which controls the on/off-state of the channel current flow. In silicon-based MOSFET technology, amorphous silicon dioxide (SiO_2) is used as the gate dielectric material and offers several key advantages in CMOS processing. These include thermodynamic stability of the dielectric layer in contact with Si, superior dielectric integrity, manufacturing process compatibility, and a low density of electrical charges in properly prepared SiO_2/Si interfaces. By thermal oxidation of Si to grow SiO_2 on the Si channel, excellent electrical properties can be reproducibly obtained; fixed charge and interface state densities are on the order of 10^{10} /cm^2 and the hard-breakdown field is ~ 15 MV/cm.

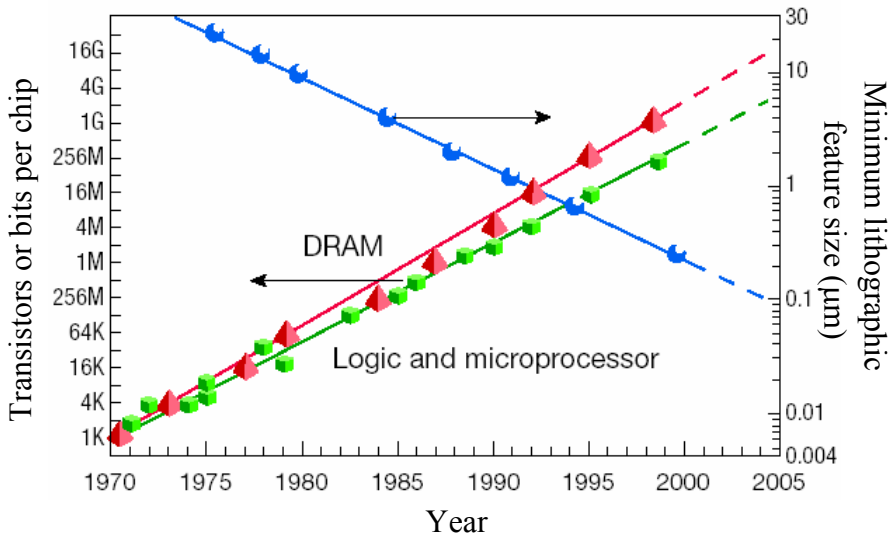

Figure 1.1: Schematic illustrating the increase in device density as the minimum lithographic feature size is reduced. Device density for both DRAM and logic devices is shown.[3]

Commensurate with the electronics industry's demand for greater integrated circuit functionality and performance at a lower cost, transistor and feature size scaling have enabled microprocessor performance to increase exponentially as evidenced by transistor density and microprocessor clock frequency doubling every two years (Moore's law, see Figure 1.1[3]). This rapid shrinking of the transistor feature size also forced the channel length and gate dielectric thickness to decrease accordingly. The improved performance of the transistor associated with device scaling can be understood by considering the theoretical operation of two-dimensional MOSFET devices. The saturated maximum drain current ($I_{D,sat}$) can be expressed using the gradual channel approximation as follows:[4]

$$I_{D,sat} = \frac{W}{L}\mu C_{inv}\frac{(V_G - V_T)^2}{2} \qquad \text{Equation (1.1)}$$

where W is the width of the transistor channel, L is the channel length, μ is the channel carrier mobility, C_{inv} is the capacitance density of the gate stack with the carrier concentrations in the channel inverted, V_G is the voltage applied to the transistor gate, and V_T is the threshold voltage. The $(V_G\text{-}V_T)$ term is limited due to reliability issues, which

can result in an undesirable, high electric field across the gate stack. Additionally, V_T cannot be reduced below 200 mV, a voltage range that is similar to statistical fluctuation in thermal energy ($kT \sim 25$ mV at room temperature). Therefore, reduction of the channel length, increase of the carrier mobility, and increase of the gate stack capacitance are the changes being pursued to increase the saturation channel current.

In order to increase the carrier mobility in the channel region, several channel-engineering technologies, such as strained Si/Si-Ge[5] are emerging and being incorporated into the CMOS processing. In the case of increasing the gate capacitance, the gate capacitance density of a simple parallel plate capacitor can be expressed as

$$C_{gate} = \frac{\kappa \varepsilon_o}{t} \qquad \text{Equation (1.2)}$$

where κ is the dielectric constant of the material, ε_o is the permittivity of free space, and t is the physical thickness of the dielectric. Thus, increase of the gate capacitance density and the corresponding improvement in device performance can be achieved by either decreasing the physical thickness or increasing the dielectric constant of the dielectric.

1.2 Limitation of SiO_2-based gate dielectrics

Silicon dioxide has been used as the primary gate dielectric material in CMOS FET devices since 1957 due to its superior material and electrical properties.[6] While the desire to enhance device speed continues to drive the dielectric thickness downward, it has been demonstrated, both experimentally[7] and theoretically,[8] that a minimum of about 0.7 nm of SiO_2 is required to obtain the bulk properties of the oxide. Furthermore, several research groups have reported that scaling of CMOS structures with SiO_2 gate oxides thinner than 1 ~ 1.2 nm results in no further gains in transistor drain current and thus the practical limit of the SiO_2 thickness is slightly larger than 0.7 nm.[9,10,11] As the lateral dimensions of MOS transistors decrease and higher switching speeds are required, scaling laws prescribe that the SiO_2 gate dielectric thickness must be decreased to less

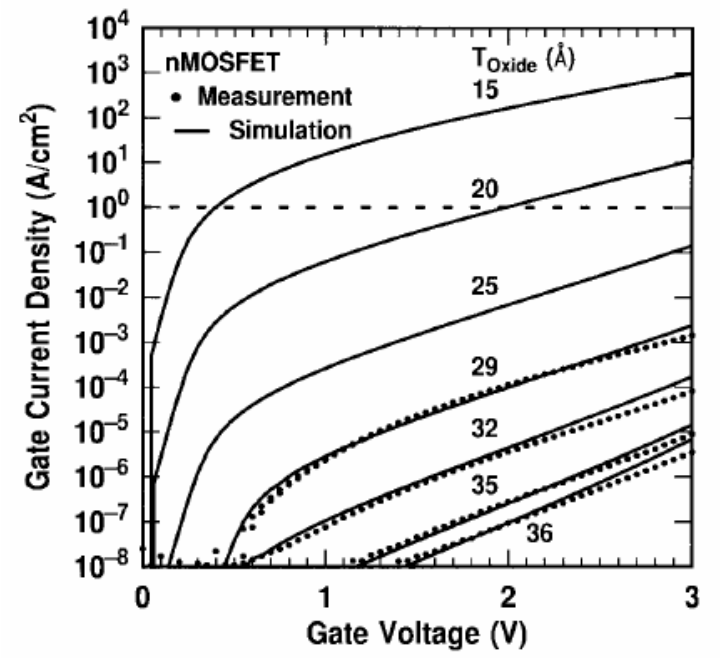

Figure 1.2: Measured and simulated I_g-V_g characteristics under inversion conditions for different SiO_2 thicknesses. The dotted line indicates the 1 A/cm^2 limit for leakage current discussed in the text.[12]

than 1.5 nm for a 0.1 μm channel length device. However, with the reduction of the SiO_2 thickness, the leakage current across the gate dielectric increases enormously through direct tunneling and cannot meet the maximum allowable leakage current density (~ 1 A/cm^2) for optimal transistor operation as shown in Figure 1.2.[12] As a result, high leakage current may decrease device reliability and also increase the stand-by power consumption, especially important for low-power applications.

Another problem with ultra-thin SiO_2 gate dielectrics is the boron penetration across the SiO_2 into the channel region in PMOS devices using P^+ polysilicon as a gate electrode. With the continued decrease in SiO_2 dielectric thickness, a significant amount of boron diffusion can cause a shift of the threshold voltage and also instability in gate dielectric reliability.[13] The use of doped-polysilicon gate electrodes on ultra-thin SiO_2 gate dielectric causes another significant problem: carrier depletion of the gate electrode. Due to the solubility limit of each dopant and the boron diffusion phenomena, a

significant increase of the electrical dielectric thickness under inversion occurs due to the poly-gate depletion. When the increase in the effective insulator thickness resulting from local carrier depletion in the electrode approaches the thickness of the SiO_2 dielectric itself, poly-depletion can no longer be ignored.[14]

In order to overcome these drawbacks and to extend the scalability of the SiO_2 gate dielectric, several chemical and structural modifications have been investigated in the last decade, such as oxynitride and oxide/nitride stacks. The addition of nitrogen to SiO_2 can provide strong Si-N bonds at either the SiO_2/Si or the poly-Si/SiO_2 interface, depending on the nitridation technique. This can enhance the dielectric reliability and prevent boron diffusion.[15,16] Although SiO_2 chemically modified with nitrogen can increase the dielectric constant and extend the scaling of the gate dielectric slightly, the maximum amount of nitrogen incorporation is significantly limited by degradation in the channel mobility and an increase in the concentration of N-related structural defects in the SiO_2 amorphous network.[17] According to the most recent industry roadmaps, oxynitride and oxide/nitride stack dielectrics represent only near-term solutions for scaling the gate stack capacitance of CMOS transistors.[18]

1.3 Consideration for high-κ gate dielectrics

Faced with these limitations on SiO_2-based gate dielectrics, another way of increasing the gate capacitance density and the physical thickness of the dielectric is to introduce new materials having higher dielectric constants. Since the 1990's, many materials have come under consideration as potential replacements to SiO_2. Figure 1.3 is a schematic diagram of a typical gate stack with high-κ dielectric which also summarizes the possible problems with introduction of new materials into the gate stack. In this section, a number of important thermodynamic and material property considerations important for integration of high-κ dielectric materials in MOS devices are discussed.

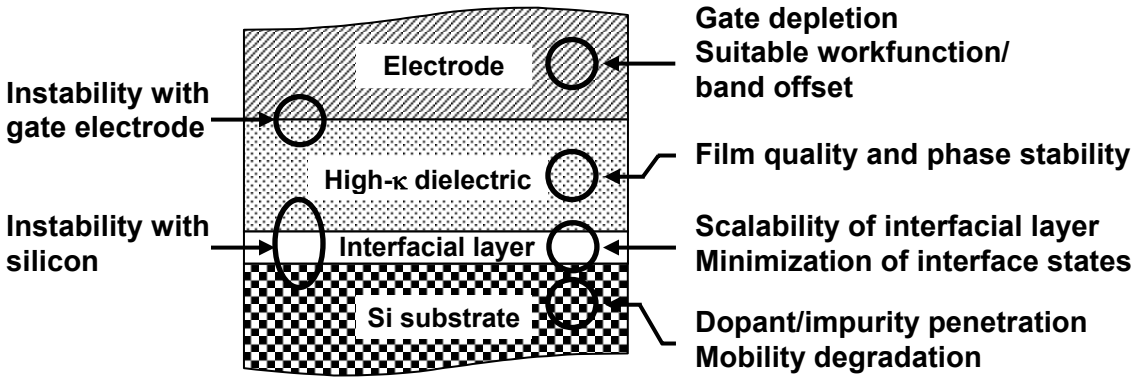

Figure 1.3: Potential problems with a high-κ gate stack.

1.3.1 Thermodynamic stability on Si

One of the most important criteria for the selection of high-κ dielectrics applicable to the conventional Si-based transistor is the thermodynamic stability of the dielectric layer with respect to solid state reaction with the Si substrates during the high temperature processing that is required for dopant activation and deposition of layers after the gate dielectric formation. Many high-κ dielectrics, such as TiO_2, Ta_2O_5, and $(Ba,Sr)TiO_3$, have been investigated in dynamic random access memory (DRAM) research. However, all of these materials are thermodynamically unstable in contact with Si at typical device processing temperatures (~ 1000°C).[3] In order to identify promising alternative high-κ gate dielectrics of the myriad metal oxide systems possible, Hubbard *et al.*[19] performed a systematic thermodynamic analysis of various metal oxide systems in contact with Si substrate at 1000 K. They considered the phase stability of metal-silicon-oxygen (M-Si-O) systems based on the available Gibbs free energy data of several key reactions (Figure 1.4). This phase diagram contains Si, oxygen, the metal under consideration, and all the oxide and silicide phases possible from a reaction of the elemental constituents (Figure 1.4 is constructed based on an assumption of negligible solid solubility of the components in the phases shown).

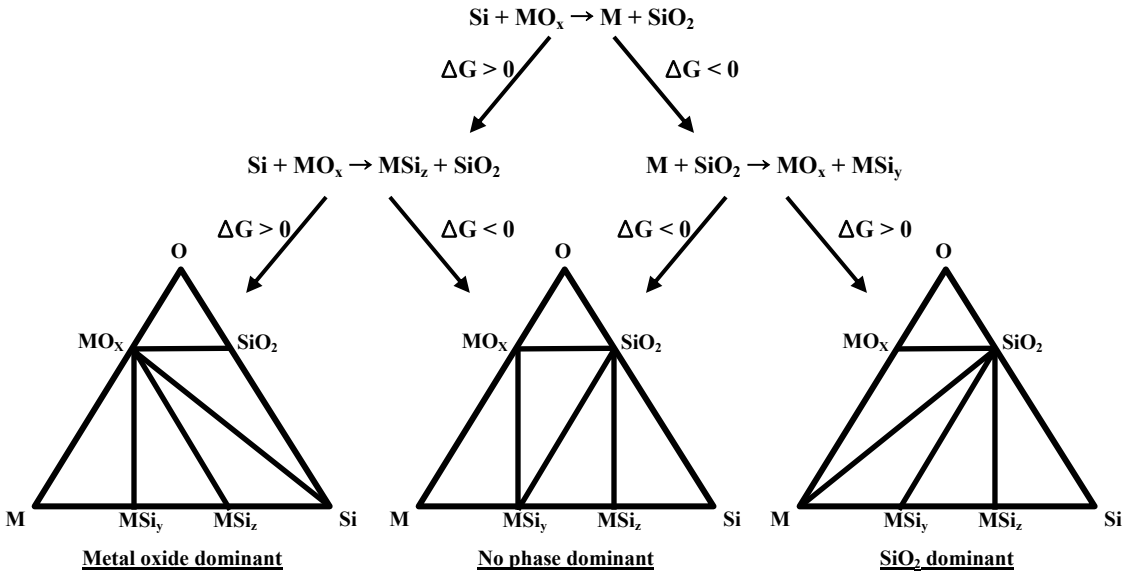

Figure 1.4: A reaction flowchart demonstrating how two reactions can be used to determine which of the three types of phase diagrams a particular M-Si-O system is described by if the system contains no ternary phases (MSi_xO_y) and only binary (MO_x) phases.[19]

Although several practical factors, such as the effects of the phase and the microstructure on the thermodynamic data, kinetic limitations within the surrounding environment, and the deposition ambient are not considered, this theoretical analysis can provide a basic guideline to rule out the unsuitable metal oxide systems. Considering the available thermodynamic data, the thermodynamic stability of binary oxides in contact with silicon is graphically summarized in the periodic table as shown in Figure 1.5.[20] Elements which have no binary oxide (MO_x) that is stable in contact with silicon are hatched in the table after following the several key criteria shown in Figure 1.5. Other elements in the table have the possibility of thermal stability with respect to solid state reaction with silicon, although the limited thermodynamic data considered, especially for metal silicates, is insufficient to definitely conclude stability.

Although the thermodynamic analysis suggests the possibility of a thermally stable high-κ gate stack without any interfacial layer for several metal oxide systems, in practice, the interfacial oxide is often unavoidable during the metal oxide deposition due

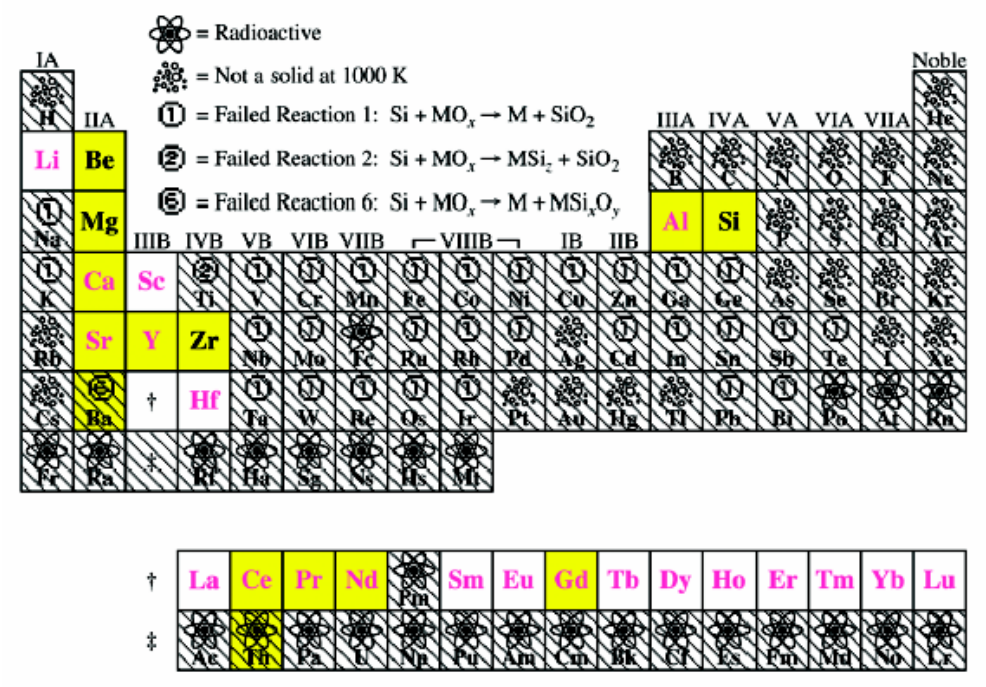

Figure 1.5: Summary of which elements M have an oxide (MO_x) that may be thermodynamically stable in contact with silicon at 1000 K.[20]

to an oxygen-rich ambient in order to achieve the correct metal-to-oxygen stoichiometry. Also, it may be preferable to have a stable interfacial oxide to improve the interfacial characteristics between Si and high-κ dielectric. Because capacitances in series add in reciprocal fashion, the dielectric properties of the interfacial layer can dominate the characteristics of the entire gate stack, thus limiting the scaling benefits of incorporating a high-κ layer in the device.

1.3.2 Permittivity and band offsets

The primary criterion for choosing a new gate dielectric as a replacement for SiO_2 (κ=3.9) for the future transistors is clearly its permittivity. Shannon[21] used a method involving the Clausius-Mossotti equation for calculating ionic polarizabilities as a means to make predictions of permittivities for many dielectrics. Although a good agreement

has been found with some experimentally measured values, there are also many discrepancies which are mainly attributed to the effect of film thickness, deposition methods, and different phases present in the dielectrics. Therefore, experimental measurement of the dielectric constants of thin metal oxide films is crucial, particularly for dielectric layers thinner than ~ 5 nm.

Another important factor to be considered for dielectric selection is the bandgap and the corresponding band offsets with the Si substrate. These offsets are directly related to the leakage current density across the dielectric film. As discussed above, the main advantage of using high-κ gate dielectrics is the reduction of the leakage current by increasing the physical thickness while maintaining the same gate capacitance density. The various leakage current mechanisms in thin dielectrics are mainly or partially dependent upon the band offsets to Si, with the smallest band offset dictating the major injected carrier type. At least 1 eV of band offset for both electrons and holes is required to have a sufficiently low leakage current for future CMOS devices. Robertson[22] calculated and compared these band offsets for various metal oxide systems using tight

Material	**Dielectric Constant**	**Bandgap, E_G (eV)**	**Conduction band offset to Si, ΔE_C (eV)**	**Crystal structure**
SiO_2	3.9	9	3.5	Amorphous
Si_3N_4	7	5.3	2.4	Amorphous
Al_2O_3	9	8.8	2.8	Amorphous
Y_2O_3	15	6	2.3	Cubic
La_2O_3	30	6	2.3	Hexagonal, cubic
Ta_2O_5	26	4.4	0.3	Orthorhombic
TiO_2	80	3.05	0	Tetragonal (rutile, anatase)
HfO_2	25	6	1.5	Monoclinic, tetragonal
ZrO_2	25	5.8	1.4	Monoclinic, tetragonal
$ZrSiO_4$ $HfSiO_4$	15	6	1.5	Amorphous

Table 1.1: Calculated dielectric constants, conduction band offsets, and typical crystal structures for several high-κ gate dielectric candidates.[22]

binding calculations and the theory of Schottky barrier heights. The calculated bandgaps and the conduction band offsets of various promising high-κ candidates are compared in Table 1.1. Because the valance band offsets for holes are always > 1 eV for most high-κ dielectrics, only the conduction band offsets are tabulated. The table indicates that very high dielectric constant materials tend to have small bandgaps.[20] Among the possible high-κ gate dielectric candidates, Ta_2O_5 and TiO_2 can be ruled out due to the expected high leakage current density resulting from their small band offsets. Other metal oxide systems, such as ZrO_2, HfO_2, silicates, Y_2O_3, and La_2O_3, are quite promising considering both the permittivity and conduction band offset.

1.3.3 Process compatibility and mobility

Even if all the electrical and thermodynamic properties of high-κ dielectric requirements are met, there remains a significant hurdle to integrate any new gate dielectric into the standard Si-based CMOS processing. Among these integration criteria, the thermal stability of the dielectric during the process used to deposit doped polysilicon gate electrodes is the primary concern. The use of Si-based gate electrode is preferred due to the accurate controllability of the workfunction of the gate electrode using n- or p-type dopants and also the compatibility with the rest of the fabrication processes. Recently, many researchers have investigated the thermal stability of ZrO_2 gate dielectrics with typical low pressure chemical vapor deposited (LPCVD) polysilicon and found a significant reduction of ZrO_2 forming a detrimental silicide under the reducing conditions provided by these CVD precursors and carrier gases (i.e., silane/disilane and H_2).[23,24] Although HfO_2 shows better thermal stability with respect to deposition of the overlying polysilicon electrode, its electrical properties are also degraded, particularly after the high temperature dopant activation anneal (1025°C).[25] On the other hand, silicates[26,27] and Al_2O_3[28,29] having lower dielectric constant often show excellent thermal stability in contact with polysilicon electrodes after typical CMOS fabrication processing. Another major integration problem with the polysilicon gate electrode is the boron

penetration phenomenon in PMOS devices. Much higher boron diffusion through high-κ dielectrics than across SiO_2 has been consistently reported in various metal oxide systems, such as ZrO_2,[30] HfO_2,[31] Al_2O_3,[32] and Hf-silicates,[33] during high temperature annealing (> 950°C). From the standpoint of eliminating the thermal instability and impurity diffusion, it is desirable to replace the conventional polysilicon electrode with metal electrodes having suitable workfunctions for both NMOS and PMOS. However, this requires a new transistor structure, such as the double gate planar transistor[34] or the vertical replacement gate transistor,[35] in order to minimize the high temperature thermal processing (e.g. dopant activation) required after gate stack formation. In spite of the process complexity and the increased cost of new transistor schemes, adopting metal gate electrode will eventually alleviate the thermal stability issue for high-κ dielectrics and also minimize gate depletion effects.

From a device perspective, another problem with introducing high-κ dielectrics into Si-based transistor is carrier mobility degradation in the channel. Significant

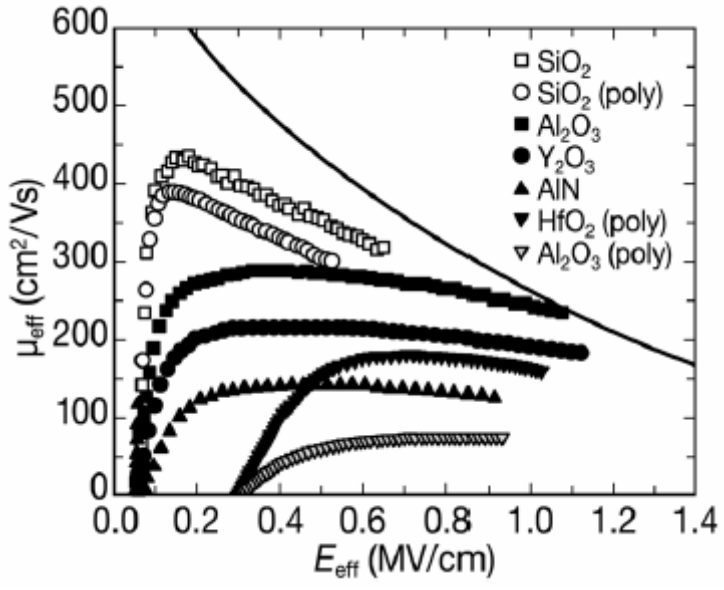

Figure 1.6: The effective mobility versus electric field for transistors with different gate dielectrics in comparison with the universal mobility curve. Unless specifically stated otherwise, aluminum was used as the gate electrode.[37]

degradation in mobility compared to the MOS transistor universal mobility model[36] has been reported by many researchers for many metal oxide gate dielectric systems independent of the film deposition methods, as shown in Figure 1.6.[37] Yamacuchi *et al.*[38], investigating an Hf-silicate dielectric system, attributed this to the additional Coulombic scattering caused by the local fluctuation of the dielectric constant which is generated by the crystallized portion of the high-κ dielectric. Conversely, Guha *et al.*[39] observed a significant diffusion of metal impurities into the channel region in an Al_2O_3/Si system using secondary ion mass spectroscopy (SIMS) measurements. Additionally they showed degradation of electron mobility caused by the increase of impurity charge scattering with thermal annealing. Although the detailed origin of the mobility degradation in transistors incorporating high-κ gate dielectrics is still being debated,[40,41] mobilities comparable to those of SiO_2-based transistors were recently reported by researchers at Intel using dual metal gate electrodes and a high-κ gate dielectric.[42]

1.3.4 Crystallinity

Most of the high-κ dielectric candidates under consideration are polycrystalline thin films. There are concerns regarding grain boundaries in these films acting as high-leakage and high-diffusivity paths. However, this concern is not yet fully substantiated; polycrystalline Y_2O_3 and ZrO_2 with very low leakage current densities have been demonstrated.[43,44] In addition, no direct evidence of increased leakage currents was observed in our HfO_2 crystallization experiments conducted using *in-situ* and *ex-situ* annealing and atomic layer deposition (ALD); this will be discussed in Chapter 3. The introduction of metal electrodes may be a possible solution to the issue of enhanced impurity diffusion (e.g. boron in PMOS) through polycrystalline high-κ dielectrics and the corresponding depletion effects.

Recently, amorphous dielectrics, such as Zr- and Hf-silicates, which can remain in an amorphous state throughout the necessary post-thermal treatments, have been widely

investigated. However, a large thermodynamic driving force for phase separation of metal silicates into metal-rich and silicon-rich phases via a spinodal decomposition process is predicted to exist from thermodynamic phase diagram analysis[45] Experimental observations have also been reported.[46] While the crystallization and phase separation temperatures can be increased by adding dopants, such as nitrogen, which reduce the diffusivity of components in the metal silicate films, resulting dielectric constant is significantly lower than in metal oxide-rich dielectrics, which at least partially defeats the purpose of introducing a new high permittivity materials system.

1.4 Properties of equilibrium ZrO_2 and HfO_2

Considering the various issues involved in materials selection for high-κ gate dielectric applications discussed in Section 1.3, ZrO_2 and HfO_2 are very interesting and promising candidates. In this section, fundamental physical and electrical properties of ZrO_2 and HfO_2 in bulk form ascertained from the literature are reviewed.

1.4.1 Crystal structures

Although the thermodynamic and microstructural data available for HfO_2 is limited compared to that of ZrO_2, both oxides have similar phase transformation characteristics according to their respective equilibrium phase diagrams.[47] The monoclinic phase is the equilibrium phase for both at lower temperatures, while the tetragonal and cubic phases predominate at higher temperatures and pressures. Figure 1.7 shows the schematic diagrams of unit cells for different phases of ZrO_2 and HfO_2 systems.[48] Figure 1.8 shows the different coordination configuration corresponding to each crystal system.[49] The stable and naturally-occurring ZrO_2 phase, called *baddeleyite*, is monoclinic as shown in Figure 1.7 (a) and (b). It has directional bonding

characteristics with 7-fold coordination as displayed in Figure 1.8 (a). However, the tetragonal phase of both oxides has 8-fold coordination with a distorted fluorite structure as shown in Figure 1.8 (b). The cations are displaced from their positions in the face-centered cubic form and are located in the center of the cube formed by anions (Figure 1.7 (c)). The anions exist in the center of regular tetrahedra formed by cations. In the case of the cubic phase, a simple fluorite structure having 8-fold coordination is exhibited.

The major defect in both oxides is an oxygen vacancy created through the following redox reaction:[50]

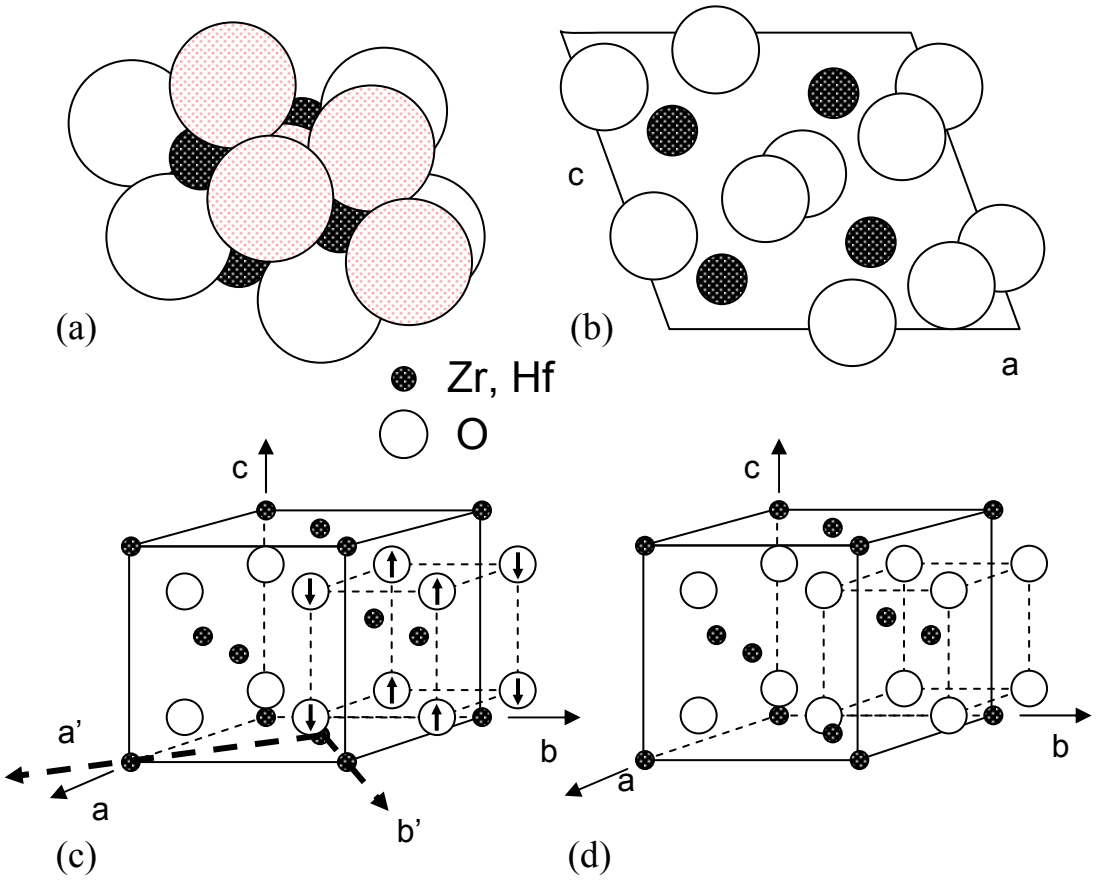

Figure 1.7: (a) 3-dimensional arrangement of the monoclinic *baddeleyite* phase viewed along the b axis, (b) projected view of monoclinic phase, (c) crystal structure of tetragonal phase (small axis indicates the direction of O atom deviation), and (d) crystal structure of cubic phase (CaF_2 structure).[48]

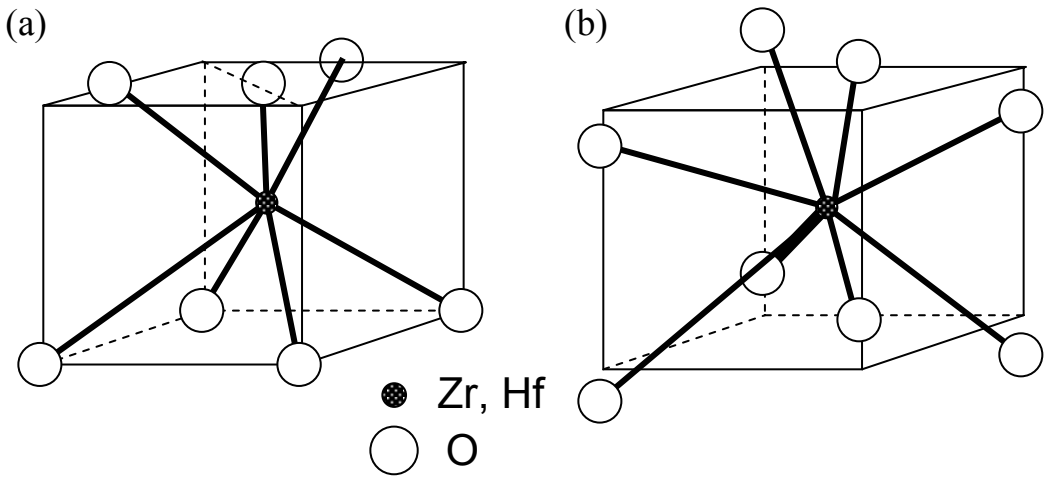

Figure 1.8: (a) Seven-fold coordination of oxygen about Zr or Hf in the monoclinic phase and (b) eight-fold coordination of oxygen about Zr or Hf in the tetragonal phase.[49]

$$O_O^{\times} \rightarrow V_O^{\bullet\bullet} + \tfrac{1}{2} O_2 + 2e' \qquad \text{Equation (1.3)}$$

where Kröger-Vink notation[51] is used to represent oxygen ions, charged oxygen vacancies, and electrons in ZrO_2 and HfO_2. Therefore, both oxides have a tendency to become oxygen-deficient under low oxygen partial pressures and can, therefore, have high oxygen diffusion rates.[52] These defects can act either as fixed charges or as bulk carrier traps when defective HfO_2 and ZrO_2 thin films are used in MOS capacitor applications.

1.4.2 Electrical properties

The dielectric constant of bulk ZrO_2 ceramics as a function of crystal structure was measured by Thompson *et al.*[53] through stabilization of different phases using additive cation dopants, such as yttrium, magnesium, calcium, and cerium. In agreement with other published results, they obtained a permittivity of 23 for monoclinic zirconia and 32 – 42 for tetragonal and cubic zirconia depending on the nature and the amount of

the stabilizing cation. The results suggested that the permittivity is principally determined by the crystallographic form rather than the nature or the amount of the added cation. In the case of HfO_2, although not much information is available in the literature, Gerstenberg[54] reported a permittivity of 25 for amorphous hafnia using a metal-insulator-metal (MIM) structure.

As discussed in Section 1.3.2, the band alignment and the corresponding barrier heights are important for a complete understanding of the electrical properties in real MOS capacitor applications. As an example, Figure 1.9 illustrates the ideal band diagram of a MOS capacitor stack ($Pt/HfO_2/SiO_2/p\text{-}Si$) based on the calculated bandgap and electron affinity.[22] The capacitor consists of a Pt-electrode and a p-type silicon substrate similar to what was used for electrical measurements in this experiment. In the case of ZrO_2, a similar band diagram is expected due to the similarity of electrical properties as discussed in Section 1.3.2.

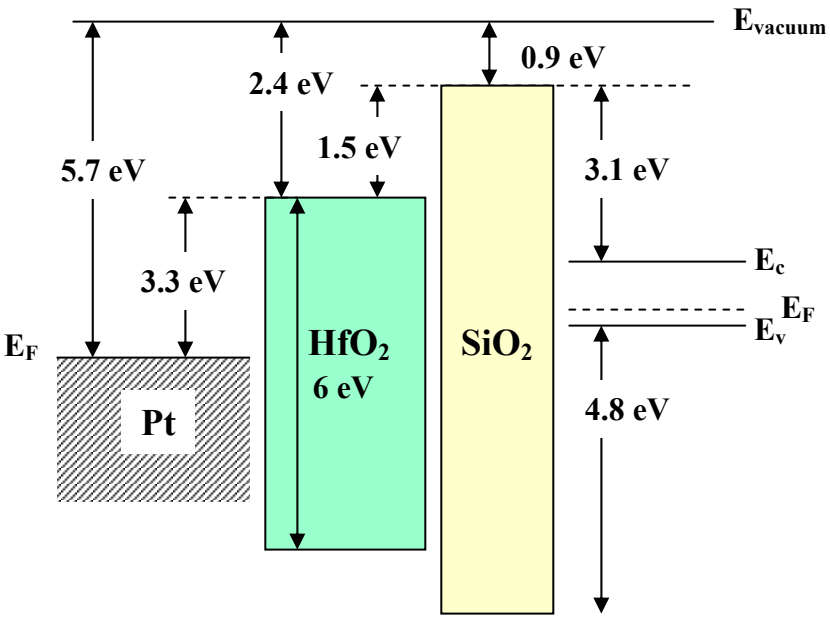

Figure 1.9: Ideal band alignment of $Pt/HfO_2/SiO_2/p\text{-}Si$ capacitor before contact. Capacitors with ZrO_2 dielectric have a similar band alignment.

References

[1] J. J. Ebers, Proc. IEEE **40**, 1361 (1952).

[2] F. M. Wanlass and C. T. Sah, Tech. Dig. – Int. Solid-State Circuit Conf. **1963**, 32 (1963).

[3] A. I. Kingon, J.-P. Maria, and S. K. Streiffer, Nature **406**, 1032 (2000).

[4] T. Hori, *Gate Dielectrics and MOS ULSIs* (Springer-Verlag, New York, 1997).

[5] L. Huang, J. O, Chu, S. A. Goma, C. P. D'Emic, S. J. Koester, D. F. Canaperi, P. M. Mooney, S. A. Cordes, J. L. Speidell, R. M. Anderson, and H.-S. P. Wong, IEEE Trans. Electron Devices **49**, 1566 (2002).

[6] C. J. Frosch and L. Derick, Proc. Electrochem. Soc., 547 (1957).

[7] D. A. Muller, T. Sorsch, S. Moccio, F. H. Baumann, K. Evans-Lutterodt, and G. Timp, Nature **399**, 758 (1999).

[8] S. Tang, R. M. Wallace, A. Seabaugh, and D. King-Smith, Appl. Surf. Sci. **135**, 137 (1998).

[9] G. Timp, A. Agarwal, F. H. Baumann, T. Boone, M. Buonanno, R. Cirelli, V. Donnelly, M. Foad, D. Grant, and M. Green, Tech. Dig. – Int. Electron Devices Meet. **1997**, 930 (1997).

[10] B. Yu, H. Wang, C. Riccobene, Q. Xiang, and M.-R. Lin, Tech. Dig. VLSI Symp. **2000**, 90 (2000).

[11] T. Ghani, K. Mistry, P. Packan, S. Thompson, M. Stettler, S. Tyagi, and M. Bohr, Tech. Dig. VLSI Symp. **2000**, 174 (2000)

[12] S.-H. Lo, D. A. Buchanan, Y. Taur, and W. Wang, IEEE Electron Device Lett. **18**, 209 (1997).

[13] M. Cao, P. V. Voorde, M. Cox, and W. Greene, IEEE Electron Device Lett. **19**, 291 (1998).

[14] D. A. Buchanan and S.-H. Lo, Proc. Electrochem. Soc. **96-1**, 3 (1996).

[15] P. Fahey, R. W. Dutton, and M. Moslehi, Appl. Phys. Lett. **43**, 683 (1983).

[16] Y. Wu and G. Lukovsky, IEEE Electron Device Lett. **19**, 367 (1997).

[17] G. Lukovsky, Y. Wu, H. Niimi, V. Misra, and J. C. Phillips, Appl. Phys. Lett. **74**, 2005 (1999).

[18] The international Technology Roadmap for Semiconductors, Semiconductor Industry Association, http://public.itrs.net/.

[19] K. J. Hubbard and D. G. Schlom, J. Mater. Res. **11**, 2757 (1996).

[20] D. G. Schlom and J. H. Haeni, MRS Bulletin **27**, 198 (2002).

[21] R. D. Shannon, J. Appl. Phys. **73**, 348 (1993).

[22] J. Robertson, J. Vac. Sci. Technol. B **18**, 1785 (2000).

[23] C. M. Perkins, B. B. Triplett, P. C. McIntyre, K. C. Saraswat, and E. Shero, Appl. Phys. Lett. **81**, 1417 (2002).

[24] K.-Y Lim, D.-G. Park, H.-J. Cho, J.-J. Kim, J.-M. Yang, I.-S. Choi, I.-S. Yeo, and J. W. Park, J. Appl. Phys. **91**, 414 (2002).

[25] D. C. Gilmer, R. Hegde, R. Cotton, R. Garcia, V. Dhandapani, D. Triyoso, D. Roan, A. Franke, R. Rai, L. Prabhu, C. Hobbs, J. M. Grant, L. La, S. Samavedam, B. Taylor, H. Tseng, and P. Tobin, Appl. Phys. Lett. **81**, 1288 (2002).

[26] G. D. Wilk, R. M. Wallace, and J. M Anthony, J. Appl. Phys. **87**, 484 (2000).

[27] C. H. Lee, H. F. Luan, W. P. Bai, S. J. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, Tech. Dig. – Int. Electron Devices Meet. **2000**, 27 (2000).

[28] J. H. Lee, K. Koh, N. I. Lee, M. H. Cho, Y. K. Kim, J. S. Jeon, K. H. Cho, H. S. Shin, M. H. Kim, K. Fujihara, H. K. Kang, and J. T. Moon, Tech. Dig. – Int. Electron Devices Meet. **2000**, 645 (2000).

[29] D. A. Buchanan, E. P. Gusev, E. Cartier, H. Okorn-Schmidt, K. Rim, M. A. Gribelyuk, A. Mocuta, A. Ajmera, M. Copel, S. Guha, N. Bojarczuk, A. Callegari, C. D'Emic, P. Kozlowski, K. Chan, R. J. Fleming, P. C. Jamison, I. Brown, and R. Arndt, Tech. Dig. – Int. Electron Devices Meet. **2000**, 223 (2000).

[30] D.-G. Park, K.-Y Lim, H.-J. Cho, J.-J. Kim, J.-M. Yang, J. Ko, I,-S. Yeo, J.-W. Park, He. De Waard, and M. Tuominem, J. Appl. Phys. **91**, 65 (2002).

[31] K. Onishi, L. Kang, R. Choi, E. Dharmarajan, S. Gopalan, Y. Jeon, C. Kang, B. Lee, R. Nieh, and J. C. Lee, Tech. Dig. VLSI Symp. **2001**, 131 (2001).

[32] D. G. Park, H. Cho, I. S. Yeo, J. A. Roh, and J. M Hwang, Appl. Phys. Lett. **77**, 2207 (2000).

[33] M. A. Quevedo-Lopez, M. El-Bouanani, M. J. Kim, B. E. Gnade, R. M. Wallace, M. R. Visokay, A. LiFatou, M. J. Bevan, and L. Colombo, Appl. Phys. Lett. **81**, 1074 (2002).

[34] J. M. Hergenrother, D. Monroe, F. P. Klemens, A. Kornblit, G. R. Weber, W. M. Mansfield, M. R. Baker, F. H. Baumann, K. J. Bolan, J. E. Bower, N. A. Ciampa, R. A. Hillenius, C. A. King, R. N. Kleiman, W. Y.-C. Lai, J. T.-C. Lee, R. C. Liu, H. L. Maynard, M. D. Morris, S.-H. Oh, C.-S. Pai, C. S. Rafferty, J. M. Rosamilia, T. W. Sorsch, and H. H. Vuong, Tech. Dig. – Int. Electron Devices Meet. **1999**, 75 (1999).

[35] S. H. Oh, J. M. Hergenrother, T. Nigam, D. Monroe, F. P. Klemens, A. Kornblit, W. M. Mansfield, M. R. Baker, D. L. Eaglesham, E. J. Ferry, A. T. Fiory, J. Frackoviak, J. P. Garno, H. J. Grossmann, J. L. Grazul, M. L. Green, S. J. Hillenius, R. W. Johnson, R. C. Keller, C. A. King, R. N. Kleiman, J. T.-C. Lee, J. F. Miner, M. D. Morris, C. S. Rafferty, J. M. Rosamilia, K. Short, T. W. Sorsch, A. G. Timko, G. R. Weber, G. D. Wilk, and J. D. Plummer, Tech. Dig. – Int. Electron Devices Meet. **2000**, 65 (2000).

[36] S. Takagi, A. Toriumi, M. Iwase, and H. Tango, IEEE Tran. Electron devices **41**, 2357 (1994).

[37] S. Guha, E. Gusev, M. Copel, L.-A. Ragnarsson, and D. A. Buchanan, MRS Bulletin **27**, 226 (2002)

[38] T. Yamaguchi, R. Iijima, T. Ino, A. Nishiyama, H. Stake, and N. Fukushima, Tech. Dig. – Int. Electron Devices Meet. **2002**, 621 (2002).

[39] S. Guha, E. P. Gusev, H. Okorn-Schmidt, L.-Å Ragnarsson, and P. Ronsheim, Appl. Phys. Lett. **81**, 2956 (2002).

[40] M. V. Fischetti, D. A. Neumayer, and E. A. Cartier, J. Appl. Phys. **90**, 4587 (2001).

[41] S. Saito, D. Hisamoto, S. Kimura, and M. Hiratani, Tech. Dig. – Int. Electron Devices Meet. **2003**, 797 (2003).

[42] R. Chau, S. Datta, M. Dockzy, J. Kavalieros, and M. Metz, International Workshop on Gate Insulator (Nov. 6, Tokyo, 2003)

[43] S. Guha, E. Cartier, M. Gribelyuk, N. A. Bojarczuk, and M. C. Copel, Appl. Phys. Lett. **77**, 2710 (2000).

[44] C. M. Perkins, B. B. Triplett, P. C. McIntyre, K. C. Saraswat, S. Haukka, and M. Tuominen, Appl. Phys. Lett. **78**, 2357 (2001).

[45] H. Kim and P. C. McIntyre, J. Appl. Phys. **92**, 5094 (2002).

[46] S. Stemmer, Y. Li, B. Foran, P. S. Lysaght, S. K. Streiffer, P. Fuoss, and S. Seifert, Appl. Phys. Lett. **83**, 3141 (2003).

[47] G. V. Samsonov, *The Oxide Handbook* (Plenum, New York, 1981).

[48] R. W. G. Wyckoff, *Crystal Structures*, Vol. 1 (Interscience Publishers, New York, 1982).

[49] Y. Kanno, J. Mater. Sci. **24**, 2415 (1989).

[50] W.D. Kingery, H.K. Bowen, and D.R. Uhlmann, *Introduction to Ceramics*, 2nd Edition (Wiley, New York, 1976).

[51] F. A. Kröger and H. J. Vink, Solid State Phys.-Adv. Res. Appl. **3**, 307 (1956).

[52] A. Kumar, D. Rajdev, and D. L. Douglass, J. Am. Chem. Soc. **55**, 439 (1972).

[53] D. P. Thompson, A. M. Dickins, and J. S. Thorp, J. Mater. Sci. **27**, 2267 (1992).

[54] D. Gerstenberg, in *Handbook of Thin Film Technology*, edited by L. I. Maissel and R. Glang (McGraw-Hill, New York, 1970).

Chapter 2

ALD Growth and Characterization

There are many deposition techniques that can be used to obtain high-κ dielectric films such as metal-organic chemical vapor deposition (MOCVD),[1] reactive sputtering,[2] UV-O_3 oxidation,[3] and atomic layer deposition (ALD).[4] Each of these deposition methods has its own advantages and disadvantages considering either the process itself or the characteristics of the resulting dielectric films. Among these techniques, ALD is promising due to the high quality of the film it produces and its controllability. In this chapter, the basic deposition mechanism and the growth kinetics of ALD are described based on both the published literature and the experimental results obtained using our laboratory-scale ALD system. Basic film qualities, such as surface roughness and conformality, were measured using ALD-ZrO_2 and HfO_2 dielectrics. Finally, the microstructural and electrical characterization tools and methods for characterizing ALD high-κ films deposited either on Si substrates or other novel substrates such as Ge are described.

2.1 Background of atomic layer deposition (ALD)

Originally, ALD was developed for the growth of epitaxial, polycrystalline, and amorphous thin films of ZnS and dielectric oxide layers for large-scale

electroluminescent display devices.[5] The ALD method uses alternating surface saturated adsorption by individually flowing each precursor sequentially, which results in high quality films having excellent uniformity and near-perfect surface conformality due to the surface adsorption-controlled nature of the method. The ALD process has some of the merits of both conventional chemical vapor deposition (CVD) and molecular beam epitaxy (MBE) techniques. Compared to these conventional deposition methods (CVD and MBE), a typical ALD process is cost efficient because a very large-scale substrate can be used with a superior surface uniformity. In terms of the hardware design, it has a very simple reactor scheme compared to sophisticated MBE or sputtering systems. Furthermore, a sub-monolayer deposition rate enables high film quality and near-perfect thickness uniformity without a sophisticated gas flow design. The characteristic features of ALD processing and their effects on the film deposition characteristics are summarized in Table 2.1.[6]

Characteristic features	Effects on film deposition & characteristics	Practical advantages
Self-limiting growth	Growth rate is linearly dependent on number of cycles and sub-monolayer growth rate per cycle	Accurate thickness controllability
	No need for reactant flux homogeneity	Near-perfect uniformity Excellent step coverage Large area capability Good reproducibility
Separate dosing of each reactants	No gas phase reactions	Clean deposition process Effective material utilization
	Layer-by-layer growth	High quality dense films can be deposited
Wide processing window	Processing conditions of different materials can be matched	Capability of multilayer in a continuous process

Table 2.1: Characteristic features and practical advantages of ALD technique.[6]

Currently, the ALD technique is drawing a lot of attention from the semiconductor industry due to its wide range of possible applications in electronic devices. The proposals of replacing the conventional SiO_2 growth process with an ALD

deposited high-κ film, and using an ALD film as the diffusion barrier layer for Cu metallization[7] are quite promising and may be essential for the future development of nano-range semiconductor devices. Moreover, great potential remains for other possible applications in many fields. In this section, the general mechanisms and the growth kinetics of various ALD processes based on recently published literatures are reviewed.

2.1.1 Deposition Mechanism

Theoretically, many material systems and even a single element, can be deposited using ALD if suitable precursors are used. Figure 2.1 illustrates a typical cycle of an ALD process using AX_n and BY_n precursors to obtain compound AB (e.g. a dielectric metal oxide film) through the following chemical reaction:

$$AX_n + BY_n \rightarrow AB + nXY \qquad \text{Equation (2.1)}$$

As an example, a step-by-step detailed chemistry for each cycle in the ALD-ZrO_2 process using $ZrCl_4$ and H_2O can be expressed as follows.

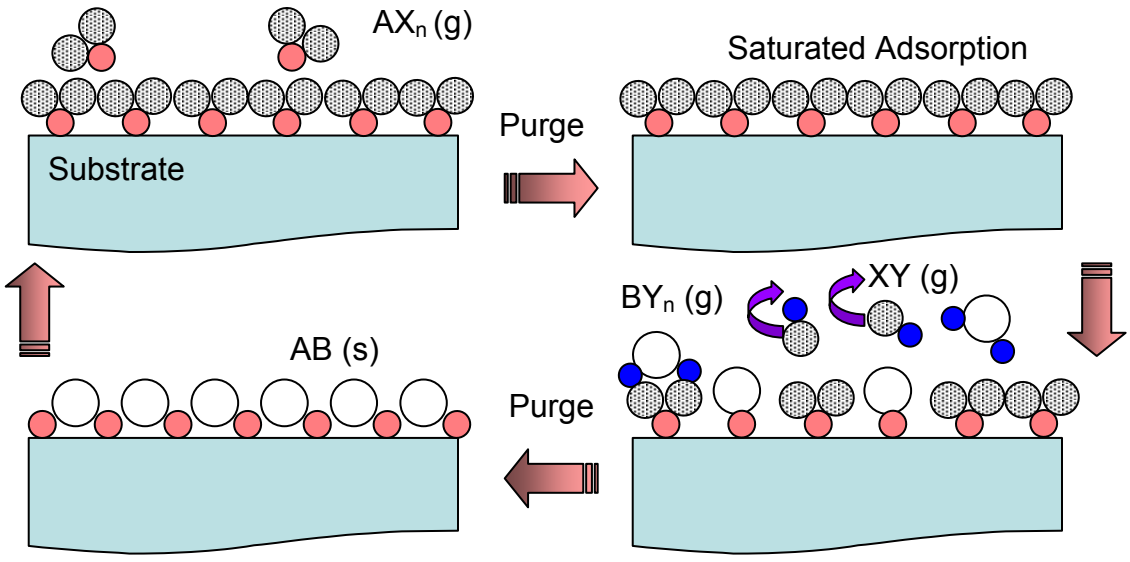

Figure 2.1: Typical sequence for one unit cycle of ALD process to obtain AB film using AX_n and BX_n precursors.

Category	Material	Chemical reaction	Category	Material	Chemical reaction
II-VI compound	ZnS	$ZnCl_2 + H_2S \rightarrow ZnS + 2HCl$		SiO_2	$SiCl_4 + 2H_2O \rightarrow SiO_2 + 4HCl$
	CdTe	$Cd(CH_3)_2 + Te(C_3H_7)_2 \rightarrow CdTe + 2C_4H_{10}$		Al_2O_3	$2Al(CH_3)_3 + 3H2O \rightarrow Al_2O_3 + 6CH_4$
III-V compound	GaAs	$Ga(CH_3)_3 + AsH_3 \rightarrow GaAs + 3CH_4$		SnO_2	$SnCl_4 + 2H_2O \rightarrow SnO_2 + 4HCl$
	GaN	$Ga(CH_3)_3 + NH_3 \rightarrow GaN + 3CH_4$	**Oxides**	TiO_2	$TiCl_4 + 2H_2O \rightarrow TiO_2 + 4HCl$
Nitrides /Sulfides	Si_3N_4	$3SiCl_4 + 4NH_3 \rightarrow Si_3N_4 + 12HCl$		ZrO_2	$ZrCl_4 + 2H_2O \rightarrow ZrO_2 + 4HCl$
	AlN	$Al(CH_3)_3 + NH_3 \rightarrow AlN + 3CH_4$		In_2O_3	$2InCl_3 + 3H_2O \rightarrow In_2O_3 + 6HCl$
	In_2S_3	$2InCl_3 + 3H_2S \rightarrow In_2S_3 + 6HCl$		HfO_2	$HfCl_4 + 2H_2O \rightarrow HfO_2 + 4HCl$
Element	Si	$Si_2Cl_6 + Si_2H_6 \rightarrow Si + 6HCl$			
	Ge	$H_2Ge(CH_2CH_3)_2 + \Delta T \rightarrow Ge + CH_2{=}CH_2 + 2H_2$			

Table 2.2: Various materials and corresponding chemical reactions which can be used for ALD processing.[8]

$$1^{st} \text{ half reaction: } Zr-OH^* + ZrCl_4 \rightarrow Zr-O-ZrCl_3 + HCl\uparrow \qquad \text{Equation (2.2)}$$

$$2^{nd} \text{ half reaction: } Zr-Cl^* + H_2O \rightarrow Zr-OH^* + HCl\uparrow \qquad \text{Equation (2.3)}$$

Initially, one precursor AX_n (e.g. $ZrCl_4$) is introduced for a short time (on the order of a second) and it is chemically adsorbed on the previous surface until it saturates the surface. Due to the availability of binding sites for the precursor and, perhaps, steric hindrance between the precursor molecules, less than a full monolayer of a given precursor is typically required to saturate the template surface. The remnant gases are removed during the following purging step with inert gas, such as N_2. After one monolayer is formed, a second precursor BY_n (e.g. H_2O) is introduced in a similar way and reacts with the existing precursor layer. The following purging step removes all remnant BY_n and the by-product XY (e.g. HCl) molecules as well. By cycling this loop, we can obtain a layer-by-layer deposition of AB film and the total growth rate is primarily determined by the surface saturation of each precursor. As a result of this surface adsorption-controlled mechanism, the ALD process has a linear growth rate characteristic that is proportional to the number of cycles, exclusively. It is independent on the deposition temperature, precursor flow rate, and duration time. In addition, due to the surface-saturation limited

growth feature, excellent conformality on complicated structures having a very high aspect ratio can be achieved with near-perfect uniformity. Various metal oxides, nitrides, compounds, and single elements can be deposited using ALD processes using the same sequence describe above. Some typical chemical reactions and precursors used for depositing various films that are experimentally verified are summarized in Table 2.2.[8]

2.1.2 Process windows and kinetics

Identifying the process window for ALD is important in optimization of process conditions and also for understanding the deposition kinetics in detail. Figure 2.2 shows the schematic diagram of a typical temperature process window for ALD and gives an indication of the limiting mechanism of ALD.[9] There are different regions in this window, depending on each of the ALD processes; the origin of each characteristic region is explained as follows.[9]

L1 region: condensation of a reactant or the result of an exchange reaction
L2 region: activation energy-limited process
W1 region: full monolayer saturation in each cycle
W2 region: surface reconstruction during the deposition or steric hindrance between large precursor molecules
H1 region: formation of non-volatile decomposition products from a reactant or a surface ligand
H2 region: desorption of a monolayer formed or dissociation of a surface ligand

Because the ALD growth rate is primarily determined by the surface adsorption of precursors, its dependence on the growth temperature should be minimal as long as the specific process is within the ALD regime. Therefore, the ALD window is characterized exclusively by a constant growth rate region (W1 or W2), which usually has a growth rate of either one monolayer per cycle or a sub-monolayer per cycle, depending on the chemistry, surface condition, and precursor size.

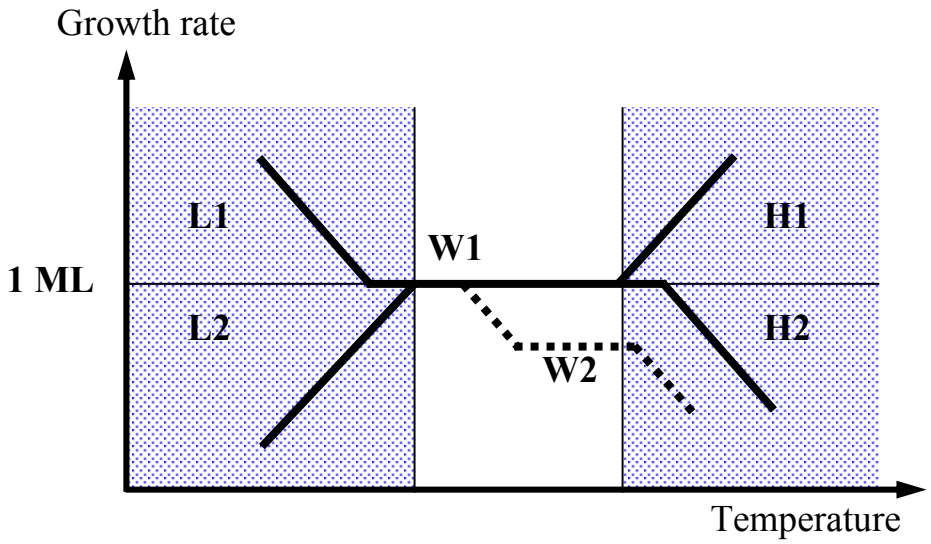

Figure 2.2: Temperature windows of a typical ALD process. ML stands for monolayer.[9]

Not only does the ALD process have a characteristic behavior that depends on temperature, it also depends on the design of the precursor delivery system. Among many possible reactor types, the "traveling-wave" type was first developed for initial large-area ALD depositions to enhance the precursor utilization.[10] This reactor schematic is a good starting point for determining the ALD window and the characteristic features of each precursor because it has a linear growth profile that depends on gas flow direction (Figure 2.3).[9] As displayed in this schematic diagram, insufficient dosing and purging, or desorption of precursors are the key factors in determining thickness uniformity. Detailed explanations for each thickness profile are provided in the caption for Figure 2.3. By correlating the thickness uniformity with the precursor and pumping directions, it is relatively easy to find process-related problems and solutions. If those parameters are well controlled, near-perfect uniformity on large-scale substrates, which can be used for display panels for example, can be easily obtained.

In choosing optimal precursors for a certain ALD process, there are a few constraints. In contrast to the requirements for reactants in the CVD process, the optimal reactants in ALD should react aggressively with each other (i.e., the activation energy of

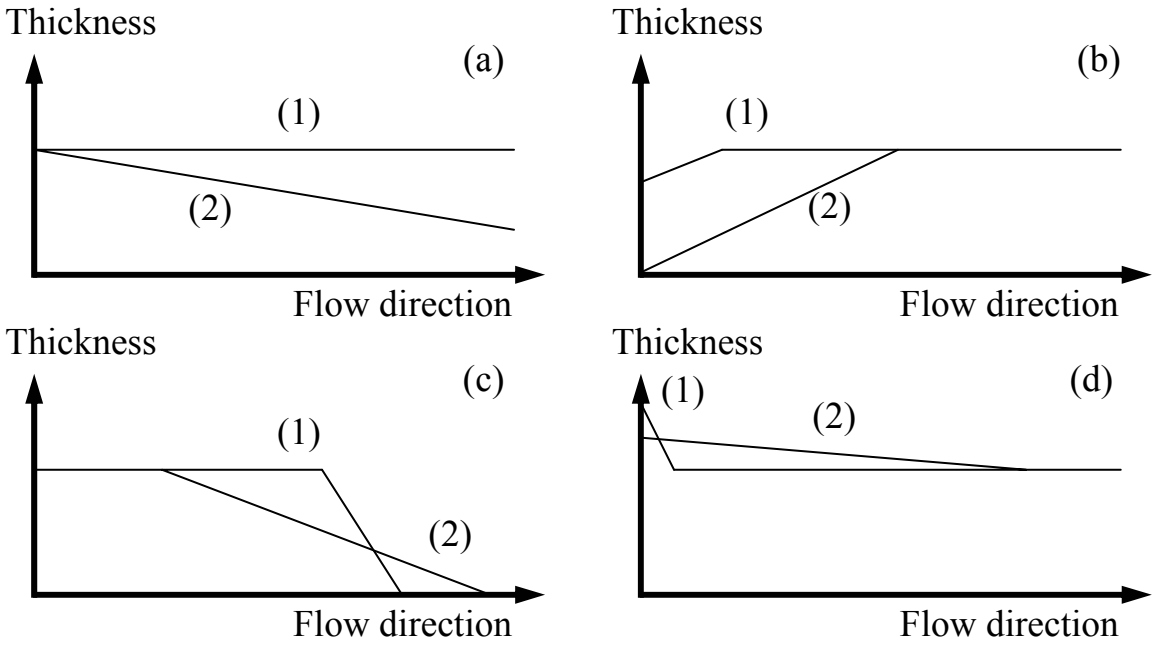

Figure 2.3: Characterization of the ALD process through the thickness profile in the direction of transport gas flow: (a) a good ALD process, (b) insufficient dosing of a reactant ((1) good and (2) poor reactivity), (c) desorption of formed monolayer ((1) slight and (2) strong desorption), and (d) insufficient purging ((1) slight and (2) strong effect of insufficient purging), CVD-like growth at the feeding end).[9]

the surface reaction should be low). In the absence of the other precursor, each reactant in ALD should also be stable at the processing temperature in order to avoid an undesirable decomposition or incomplete surface reaction.

2.1.3 Dependence on the surface status

Compared to other deposition techniques, the ALD method is very sensitive to the initial surface condition because of the inherent nature of surface-controlled growth mechanism. In the case of an ALD process based on H_2O and metal chloride precursors in particular, the initial surface template can play an important role in subsequent film quality and growth rate. For the high-κ gate dielectric deposition, it would be preferable

to have the initial interface oxide completely removed using HF treatment to increase the total capacitance per unit area for aggressive dimensional scaling of devices. Figure 2.4 shows the cross-sectional high resolution TEM image of ZrO_2 on hydrogen-terminated Si substrate after HF cleaning as reported by M. Copel *et al*.[11] It shows a discontinuous and irregular island-type growth at a reduced film growth rate. Due to the lack of a hydroxyl-terminated template for the initiation of ALD reaction, the nucleation observed on the hydrogen-terminated samples is clearly inhibited. Furthermore, some portion of the Si-H passivation is believed to be desorbed at the deposition temperature (300°C), and uneven nucleation of ZrO_2 may result in island formation rather than uniform film growth. With different initial surface treatments or different methods of forming a SiO_2 underlayer, different growth rate behavior, especially at the initial transient regime, is reported.[12] The use of a chemical oxide at the initial surface resulted in a dimensionally continuous film exhibiting uniform linear growth at constant film density due to the large concentration of OH groups, which act as effective ALD adsorption sites, in the chemical oxide.

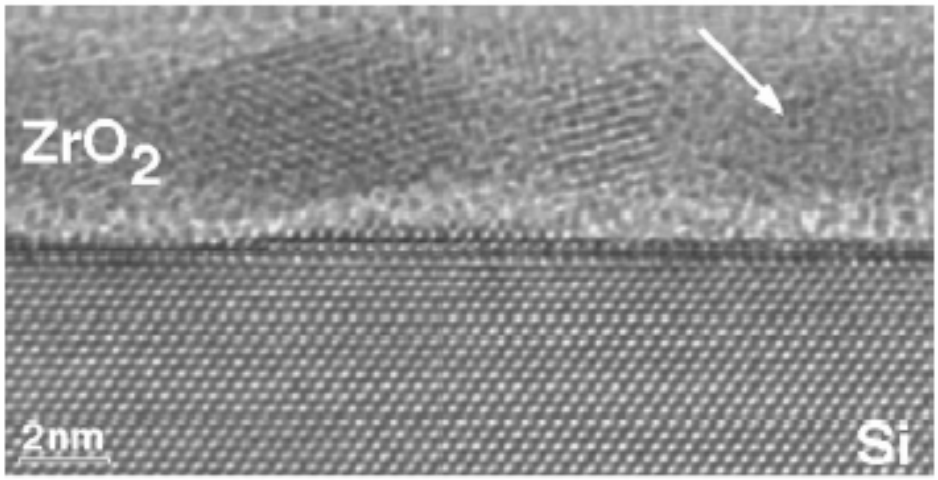

Figure 2.4: High resolution TEM image of a ZrO_2 layer grown on an HF-stripped Si (001) using ALD.[11]

2.2 Hardware configuration of the Stanford ALD system

In order to perform the high-κ gate dielectric depositions required in this research, a laboratory-scale ALD system was built using a conventional cold-wall type vacuum chamber. Figure 2.5 shows the schematic diagram of the Stanford ALD system having ZrO_2 and HfO_2 deposition capabilities. Figure 2.6 displays pictures of the ALD system taken at various angles. It is composed of a high vacuum main chamber for ALD processing and a loadlock system to prevent possible contamination during sample loading and unloading. Both chambers are maintained at a pressure of ~ 5×10^{-7} Torr using turbomolecular pumps backed by mechanical pumps. A 3-inch diameter susceptor is used to hold and to heat the wafer during the process. It was built with a ceramic heater enclosed by an inert Ni block to prevent possible HCl attack and oxidation of the heater in the strongly oxidizing ALD ambient. The temperature of the heater is monitored by a K-type thermocouple inserted into the Ni susceptor. The resistive ceramic heater can ramp up to 1000°C in oxidizing and corrosive ambients, and it is controlled by a temperature controller and power SCR (semiconductor).

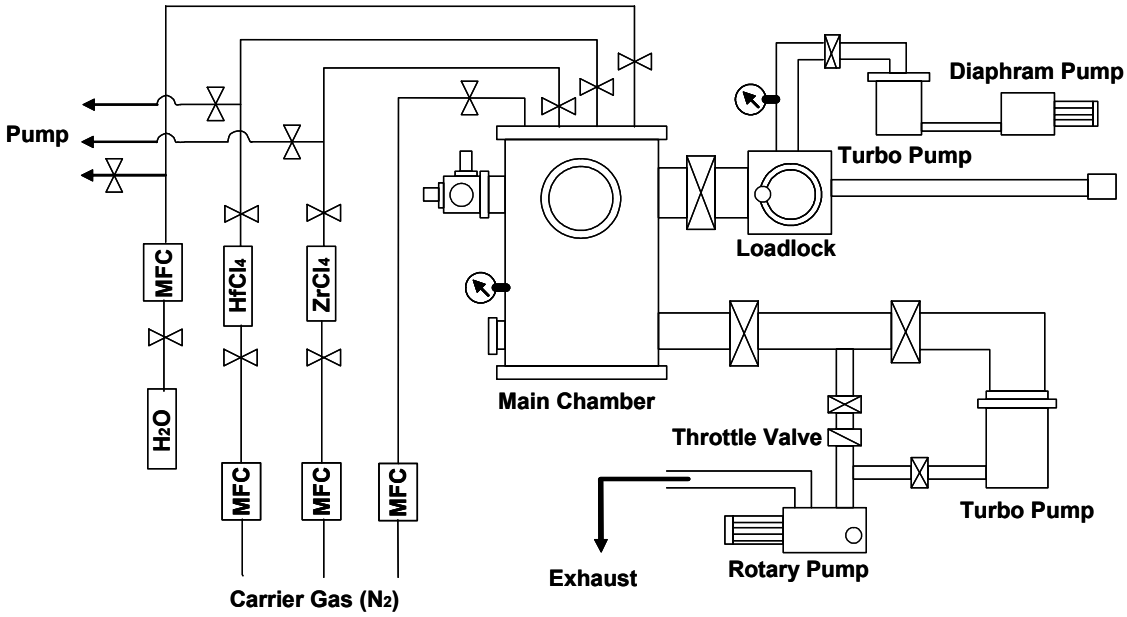

Figure 2.5: Schematic diagram of the Stanford ALD system.

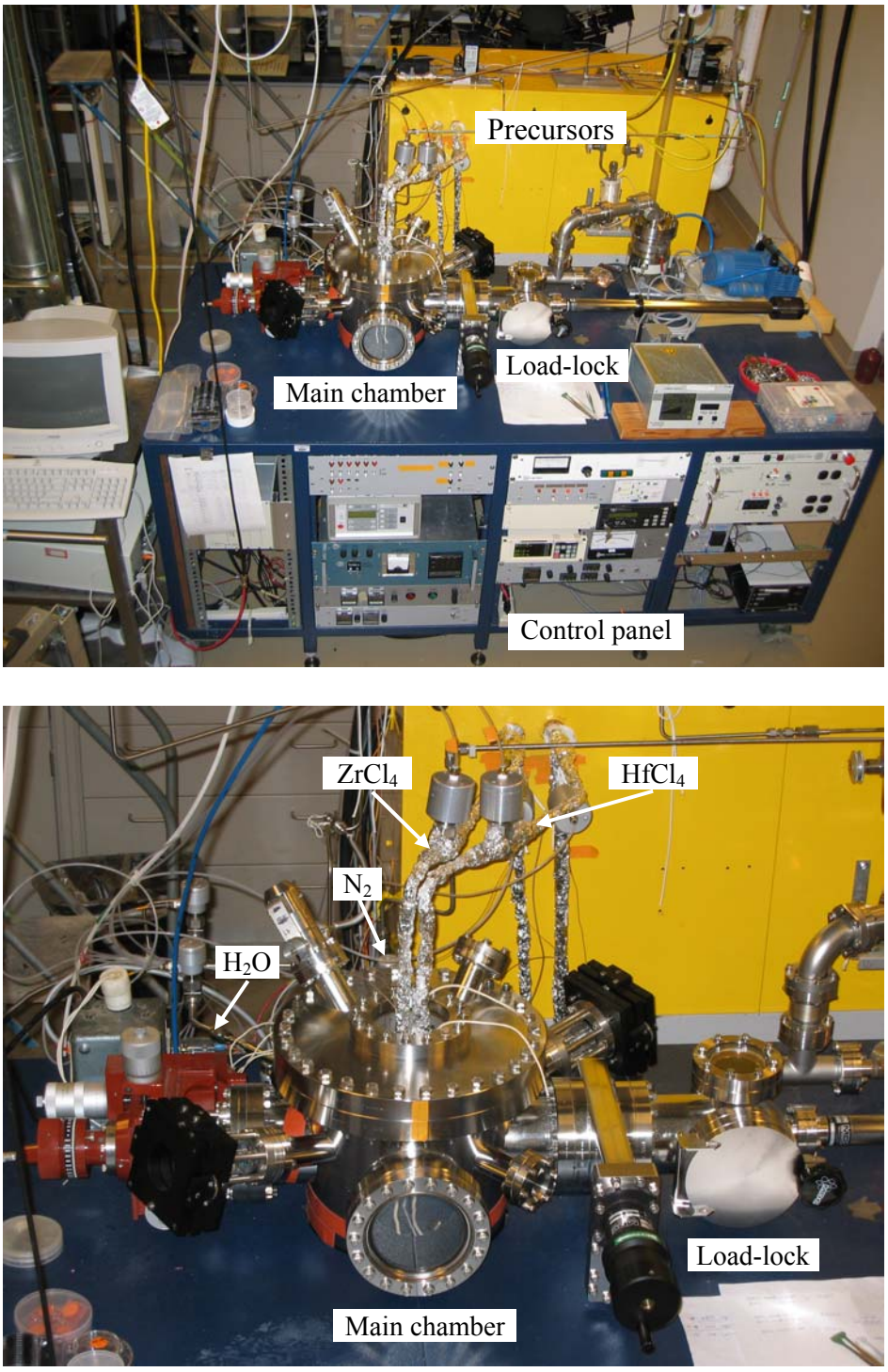

Figure 2.6: Front-views of the Stanford ALD system.

The details of the gas line manifold configuration are shown in Figure 2.7. Fine solid powder forms of $ZrCl_4$ and $HfCl_4$ which are used as ZrO_2 and HfO_2 precursors, respectively, are kept in stainless steel source bottles. Because of the low vapor pressures of $ZrCl_4$ and $HfCl_4$ at room temperature, each bottle is heated to 150°C to obtain adequate vapor pressure (~ 63 mTorr for $ZrCl_4$[13]). The rest of the gas manifold is also heated to prevent possible precursor condensation and line clogging problems. N_2 carrier gas, controlled by a mass flow controller (MFC), is used to obtain a sufficient flow rate. A precursor by-pass line, which can transport species directly to the mechanical pump during portions of the ALD cycle when a given precursor is not flowing into the chamber, is continuously pumped down by a mechanical pump to prevent condensation and also to stabilize the gas flow during the ALD process. Because of a particle flow problem originating from the powder form of metal precursors, a gas line filter (60 μm pore size) is incorporated before the injection point to the deposition chamber. As an oxidizer, high purity de-ionized H_2O in a stainless steel bubbler is used without heating due to its high

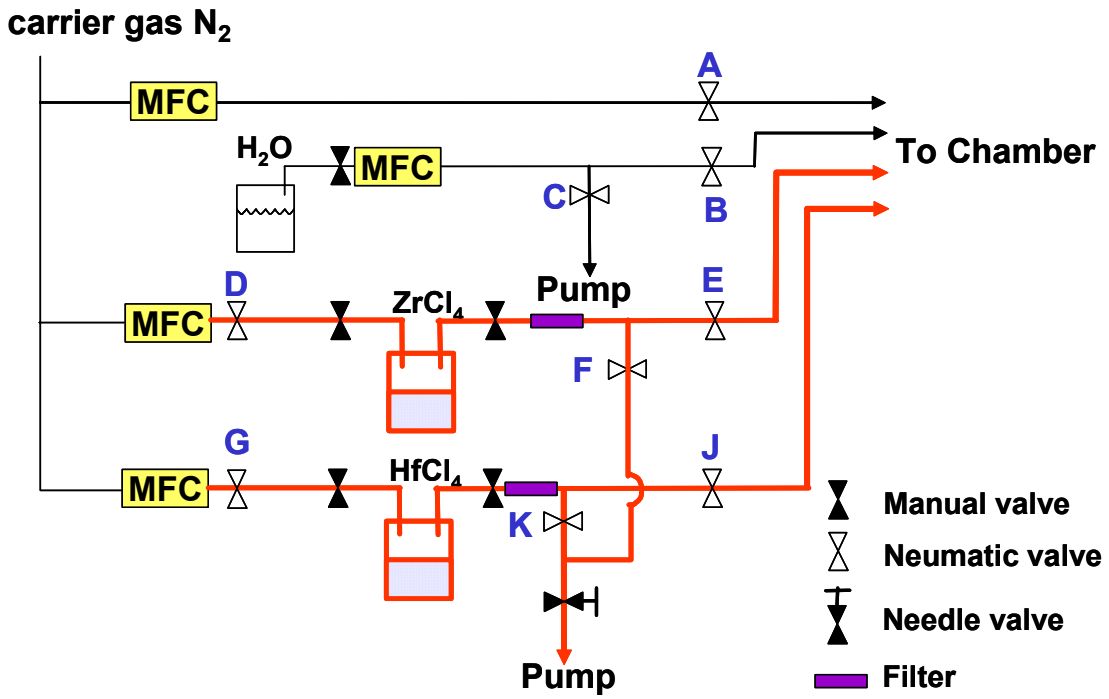

Figure 2.7: Schematic diagram of gas line configuration for $ZrCl_4$, $HfCl_4$, and H_2O.

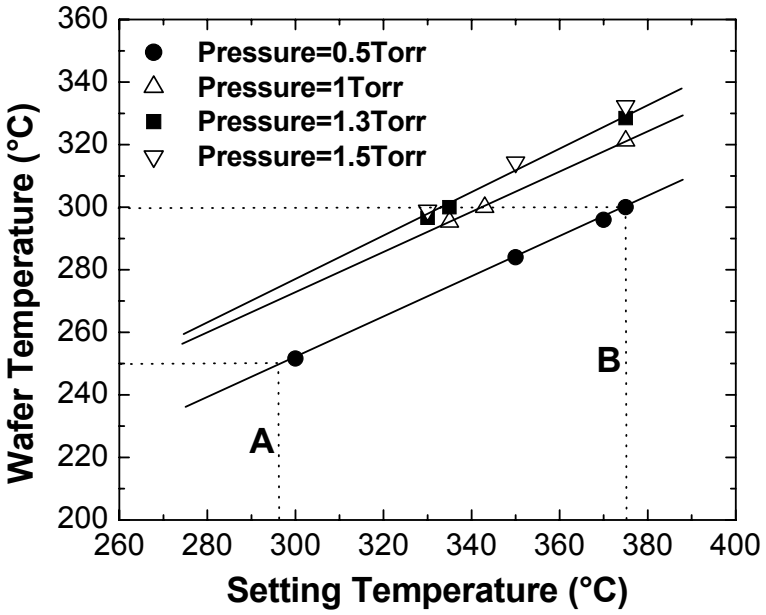

Figure 2.8: The actual wafer temperature as a function of heater set point temperature. (Chamber pressure was controlled by changing the N_2 flow rate). Point A and B indicate 250°C and 300°C process conditions, respectively.

vapor pressure at room temperature. In order to avoid cross-talk between the H_2O by-pass line, the metal precursor by-pass line, and the deposition chamber due to the strong reactivity between precursors, separate mechanical pumps are used to isolate these lines. All the pneumatic valves and process sequences are controlled by a computer using a LabVIEW™ program.

Before ALD process optimization, deposition temperatures were calibrated for various pressures using a bare-Si wafer with thermocouples attached to it (Figure 2.8). Two K-type thermocouple wires were attached on a 3-inch bare Si wafer at different locations using a high thermal conductivity Ag-paste. Due to the indirect contact between the ceramic heater and the actual silicon wafer, there was a large temperature difference that is dependent on the system pressure. Two deposition temperatures of 250°C and 300°C were used for the ZrO_2 and HfO_2 depositions, respectively, but for most of the samples used for electrical measurements, a deposition temperature of 300°C was used in order to minimize the amount of Cl residual impurities in the metal oxide

films originating from their Cl-based precursors. The temperature difference between the center and the edge of the 3-inch wafer was less than ± 1°C variation for all the deposition temperatures.

2.3 Process optimization for ALD-ZrO_2 and HfO_2 processes

2.3.1 Process conditions

After loading a wafer into the main deposition chamber, the pressure was reduced to ~ 0.5 Torr and maintained by flowing N_2 (92 sccm). The wafer temperature was then ramped to the desired set point for ~ 60 min. During the ramp-up, all the precursors were pumped to the by-pass line pump to stabilize the gas flow. Twenty sccm N_2 was used for the carrier gas for each metal precursor and 0.7 sccm H_2O was used as an oxidizer. During the deposition process, although the actual amount of metal precursor flowing in the chamber was not determined, the flow rate was controlled by the position of a needle valve which controlled the amount of precursor by-passed between each pulsing period. The needle valve setting was determined by monitoring the increase in system pressure

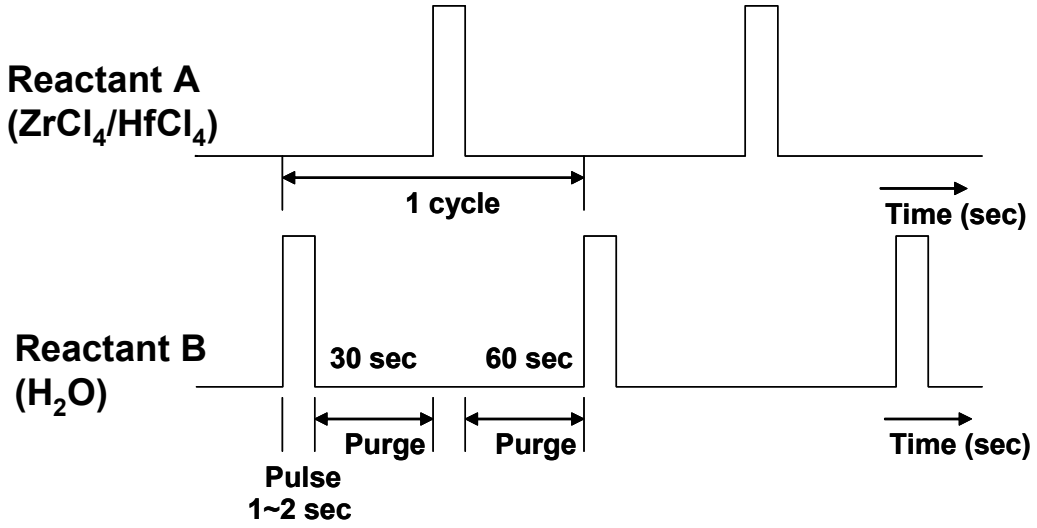

Figure 2.9: A schematic diagram of ALD recipe for ZrO_2 and HfO_2 deposition.

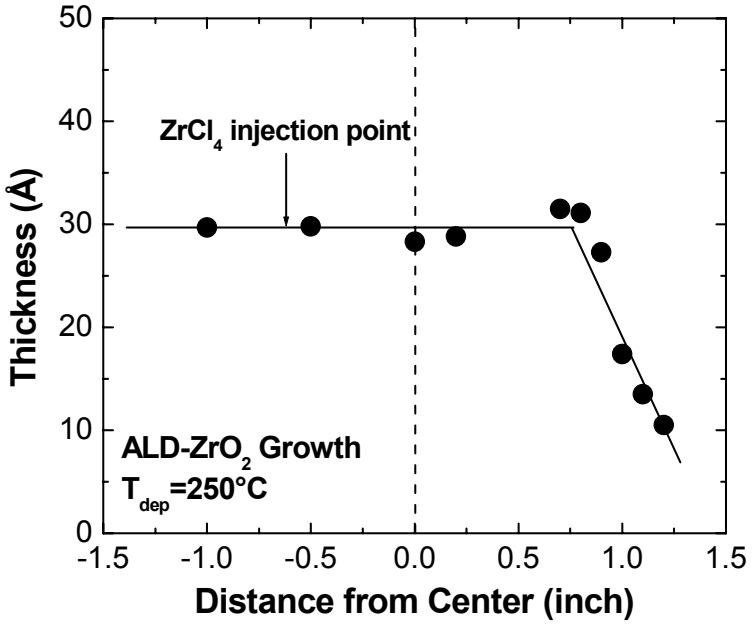

Figure 2.10: The thickness variation of ALD-ZrO_2 across a 3-inch Si wafer when the $ZrCl_4$ precursor is not sufficient. The arrow indicates the injection point of $ZrCl_4$.

during the precursor pulsing step and by characterizing the resulting film quality, in particular the thickness uniformity.

During deposition, the system pressure was maintained at 0.5 Torr and each pulsing/purging cycle time is shown in Figure 2.9. Initially, H_2O is introduced to the wafer surface to promote a hydroxylated surface, which facilitates uniform growth of metal oxides on SiO_2 passivated surfaces.[14] The durations of each pulsing and purging step were chosen to optimize thickness uniformity and to avoid CVD reactions which could be caused by remnant precursor gases after the purging step. Compared to commercially available ALD systems, the total time for each cycle is longer due to the large dead-volume of the chamber. If the precursor amount is insufficient, the final film thickness abruptly decreased away from the source injection region as shown in Figure 2.10, consistent with the discussion in Section 2.1.2. Excessive precursor injection requires longer purging time to remove all the remnant gases and as a result, increases the total processing time.

After a complete high-κ metal oxide deposition, the thickness of metal oxide was measured using an ellipsometer (Rudolph Auto-EL III) with 632.8 nm wavelength He-Ne laser and the measured optical thickness was calibrated using cross-sectional TEM analysis. Because all the high-κ depositions were carried out either on a chemical oxide on Si or on a thermally-grown oxide on Si in these experiments, the thickness was measured using a double-layer model[15] by assuming all necessary parameters, such as the refractive index of each layer and the sub-layer thickness. Through a series of process optimization steps, the resulting thickness uniformity was improved to < ±1 Å for 5 points measurement on 3-inch wafers for both ZrO_2 and HfO_2 films.

2.3.2 Linear and sub-monolayer growth rate

Initial process testing and optimization of the ALD-ZrO_2 and HfO_2 depositions were performed at 250°C and 300°C. However, the 300°C process was used primarily for electrical and microstructural analysis of the ALD-ZrO_2 and HfO_2 films because of the reduced residual chlorine concentration at this temperature. The 300°C process exhibited qualitatively similar growth kinetics behavior as the 250°C process due to the temperature independent characteristics of the ALD process as discussed in Section 2.1.2. For the growth kinetics studies, 3-inch p-type Si wafers having 1 – 10 Ω-cm resistivity, covered with a chemical oxide (~ 1.5 nm thickness) were used. Figure 2.11 (a) shows the thickness versus the number of ALD cycles for ZrO_2 grown at 250°C. It is observed that the thickness varies linearly with deposition cycles, as expected. The growth rate was ~ 0.6 Å/cycle, which is close to the typical sub-monolayer growth rate per cycle reported by other groups studying ALD of this material using chloride and H_2O precursors.[16] When the H_2O flow rate is excessive and the water is not properly removed during the subsequent N_2 purging step, a CVD-like growth behavior having a higher non-linear growth rate (> one monolayer/cycle) is observed, as indicated in Figure 2.11 (a); this results in an uncontrollable uniformity. In the case of HfO_2 growth, a similar linear growth behavior, having a sub-monolayer growth rate depending on the H_2O flow time,

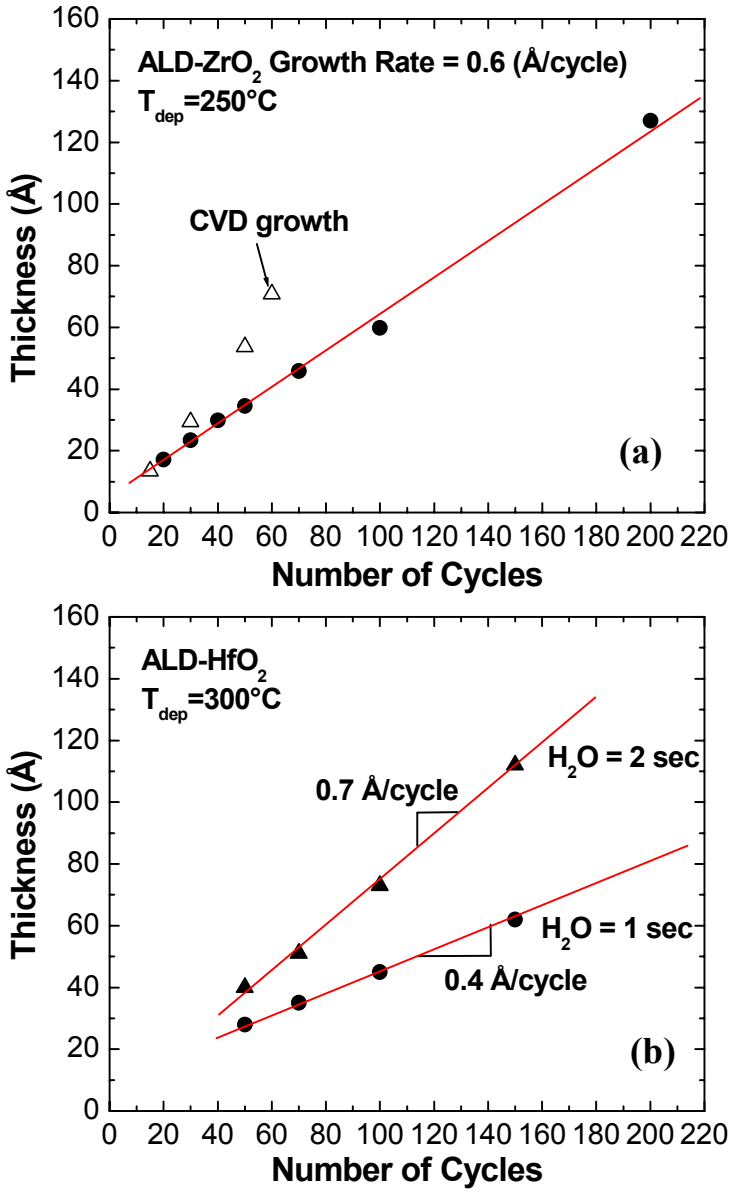

Figure 2.11: (a) The growth rate of ALD-ZrO_2 at 250°C. With excessive H_2O flow rate, the growth rate exhibited a CVD-like growth characteristic. (b) The growth rate of ALD-HfO_2 with different H_2O pulsing times.

is observed as shown in Figure 2.11 (b). The H_2O flow dependence of the growth rate also appeared in the ALD-ZrO_2 process and will be discussed in the following section.

Different from the ideal monolayer growth rate (~ 2.6 Å), i.e., one monolayer spacing along the <001> crystallographic axis, the growth rate of ZrO_2 and HfO_2 showed

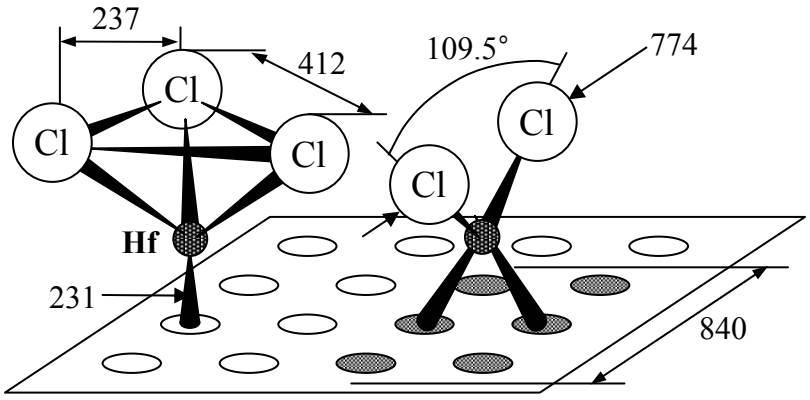

Figure 2.12: Two configurations of an adsorbed hafnium chloride molecule.[17] The unit of length used is picometers (pm).

less than 1 Å/cycle, regardless of H_2O flow. Ylilammi[17] modeled this phenomenon using the geometry of reactant molecules and the density of the adsorption sites on the surface in various ALD chemistries. Figure 2.12 illustrates the geometrically possible configuration of $HfCl_4$ adsorption on the surface. Based on the calculations of packing density and the growth rate, at least two Cl^- ions must be cleaved and $HfCl_2^{2+}$ should be tetrahedrally bonded to the surface oxygens. Ylilammi's calculated growth rate of ZrO_2 and HfO_2 was 0.66 Å/cycle, which agrees well with our experimental results. Another alternative explanation for the sub-monolayer growth rate per cycle could be the desorption of the relatively unstable intermediate species in each chloride-based ALD step for HfO_2 and ZrO_2. The effects of the purge duration have been investigated by Ritala *et al*.,[16] where the growth rate has been observed to decrease with increasing purge duration. This suggests that the adsorbed species, $ZrCl_4$/$HfCl_4$ and H_2O, are more likely to desorb than to further dissociate and decrease the growth rate accordingly. Also, Widjaja *et al*. [18,19] calculated the desorption activation free-energy of the adsorbed precursors in Cl-based ZrO_2 and HfO_2 ALD using density functional theory and found that it becomes smaller than the dissociation activation free-energy at higher temperature.

2.3.3 Dependency on the precursor flow rate

One of the intrinsic characteristics of the ALD process is the independence of the growth rate on the metal precursor dose due to the surface-saturation mechanism.[20] However, if H_2O is used as an oxidizer, the amount of the H_2O dose has a significant effect on growth rate, thickness uniformity, and the residual chlorine concentration in both hafnium and zirconium oxide films, as shown in Figures 2.13 and 2.14. In this experiment, the H_2O flow rate was controlled by the needle valve setting; therefore, the absolute amount of water introduced into the chamber is not known. By increasing the needle valve setting, we could increase growth rate and also decrease chlorine concentration incorporated in the films, which was measured by X-ray Photoelectron Spectroscopy (XPS, Surface Science Instruments S-Probe using an Al K_α x-ray source). Matero *et al.*[21] reported the same trend in many ALD deposition systems using H_2O as an oxidizer. They observed a growth rate per cycle increase of up to a factor of two depending on the metal oxide system, and attributed the phenomenon to the increased density of surface hydroxyl groups after the water exposure. By increasing the density of hydroxyl groups, each deposited metal precursor (metal-chloride) layer can be packed more densely and also more metal–Cl bonds can be removed, resulting in a low residual Cl level in the final metal oxide film. By increasing the H_2O flow rate and the deposition temperature to 300°C, the residual chlorine concentration was reduced to below the XPS detection limit (< 1 %) for both the ZrO_2 and HfO_2 processes performed in our ALD system.

In the case of metal precursor flow rate, the growth rate did not depend on the metal precursor flow rate, which is consistent with the results of many published ALD studies. This confirms that our metal oxide deposition processes were performed in the ALD regime as opposed to the CVD regime. Figure 2.14 illustrates an example of the ALD-ZrO_2 process. The $ZrCl_4$ injection time was controlled to change the total amount of precursor introduced into the chamber, and the H_2O flow rate was also varied by controlling the needle valve setting. Within the ALD regime, after a certain saturation period, the growth rate was independent of the precursor injection time. Conversely, the

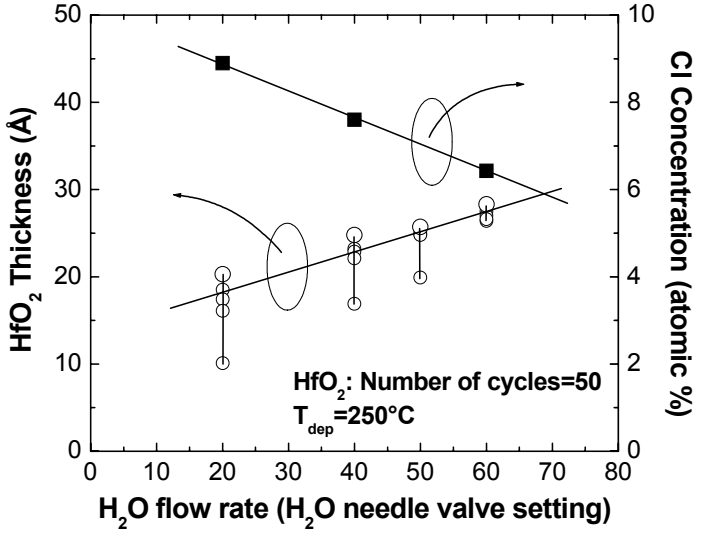

Figure 2.13: Thicknesses of ALD-HfO_2 measured from five different positions on a wafer and chlorine concentration as a function of H_2O flow rate (needle valve setting).

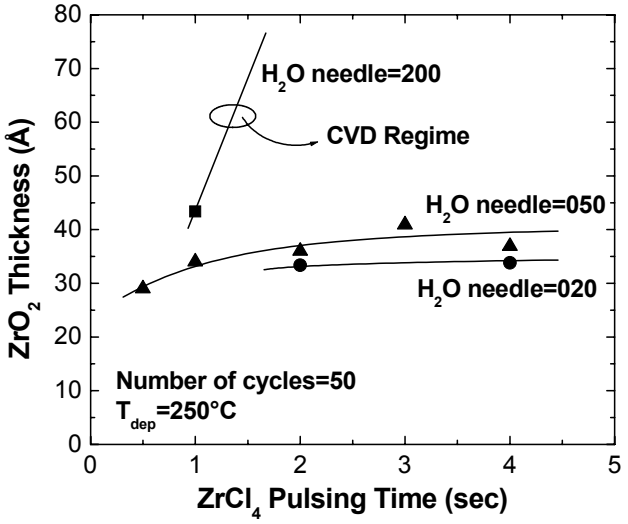

Figure 2.14: Thickness of ALD-ZrO_2 with different H_2O flow rates as a function of $ZrCl_4$ pulsing times.

onset of a CVD regime can be seen in the dramatic increase in growth rate as more metal precursor was introduced under conditions of excessive H_2O supply to the chamber.

2.3.4 Surface roughness and conformality

Due to surface saturation-controlled growth and resultant sub-monolayer deposition rate, ALD films have an atomically smooth surface and near-perfect surface conformality.[22] The surface roughnesses of ALD-ZrO_2 and HfO_2 films were measured

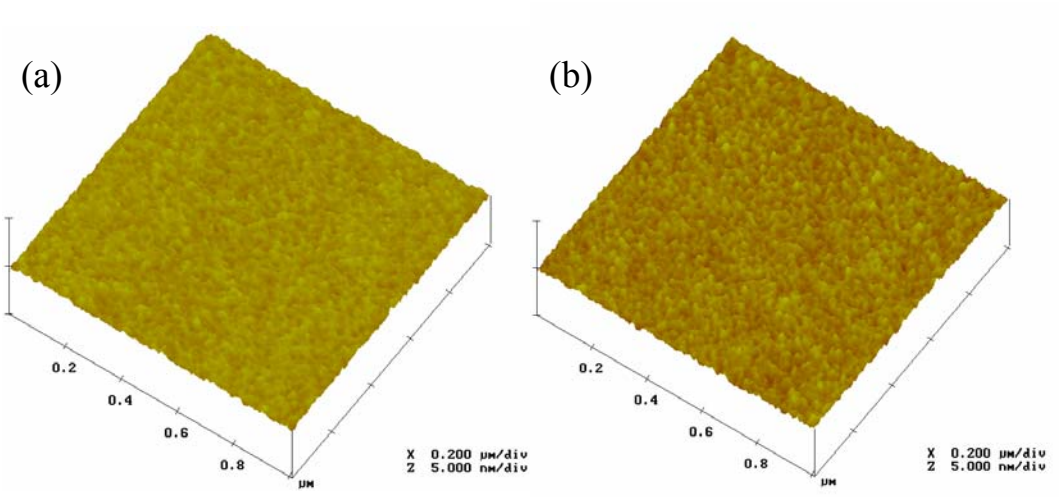

Figure 2.15: AFM images of (a) ~ 3 nm ZrO_2 and (b) ~ 3 nm HfO_2 with 1μm×1μm scan range. The RMS surface roughness of both samples is less than 1.5 Å.

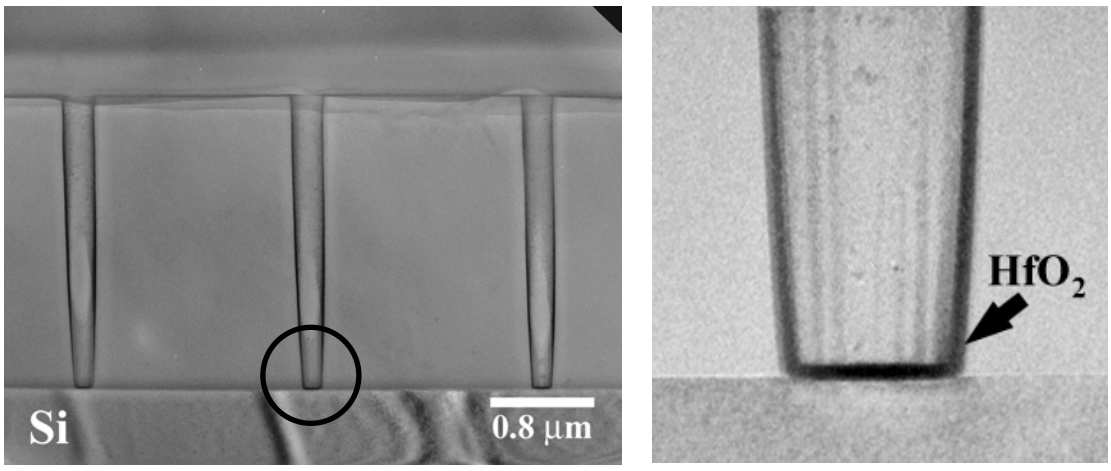

Figure 2.16: Cross-sectional TEM images of contact holes having 0.2 μm opening and 2 μm depth deposited with 12 nm ALD-HfO_2. Right image is a magnification of the region indicated by a circle in the left image.

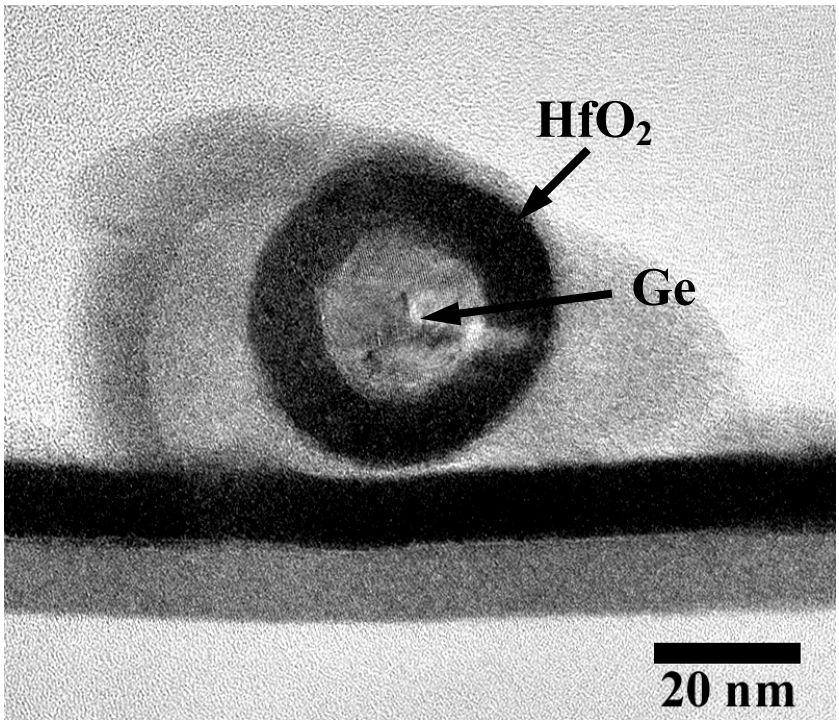

Figure 2.17: Cross-sectional TEM image of a Ge nanowire (~ 20 nm diameter) coated with ~ 10 nm ALD-HfO_2.

using an atomic force microscope (AFM – Digital Instruments Nanoscope 3000) in tapping mode. Figure 2.15 shows AFM images of ~ 3 nm thickness ALD-ZrO_2 and HfO_2 films grown at 300°C. The root-mean-square (RMS) was less than ~ 1.5 Å across 1 × 1 μm^2 scan area for both samples.

In order to check the conformality of our ALD films, ZrO_2 and HfO_2 were deposited on a patterned wafer having an array of contact structures. The contact size was ~ 0.2 μm and the height was ~ 2 μm thus giving an aspect ratio of 10. Figure 2.16 shows the cross-sectional TEM images of contact arrays having ~ 12 nm of ALD-HfO_2. It shows a conformal and continuous deposition along the contact hole without any shadow effect. The measured thicknesses at the contact bottom and sidewall were identical, showing almost 100 % step coverage. As an extreme case, ~ 10 nm ALD-HfO_2 was deposited on a Ge nanowire having ~ 20 nm diameter. Conformal deposition surrounding the wire was achieved as shown in Figure 2.17.

2.4 Microstructural characterization using TEM

Transmission electron microscopy (TEM) is a powerful tool for characterizing the microstructures of thin films, including nanometer-scale gate dielectrics.[23] The importance of TEM is rapidly increasing as many device structures are shrinking close to atomic dimension. In determining the exact thickness and analyzing the microstructural properties of high-κ thin dielectric films, a high resolution TEM imaging technique and other imaging techniques, such as the selected area electron diffraction pattern (SADP) and bright field/dark field diffraction contrast imaging, are crucial. Recently, very sophisticated analysis techniques, such as a high angle annular dark field (HAADF) scanning transmission microscopy (STEM) using atomic number sensitive "Z contrast" imaging and electron energy-loss spectroscopy (EELS), are used for studies of the local atomic and electronic structures of thin gate stacks and interfaces.[24]

2.4.1 TEM sample preparation

Careful cross-sectional TEM sample preparation of high-κ dielectrics is very important in obtaining accurate thickness measurements of dielectric films and also for avoiding artifacts that may confuse the interpretation of interface structure. In order to obtain a cross-sectional TEM specimen, two high-κ samples were bonded face-to-face using glue (G1 epoxy, Gatan) and thinned down using conventional mechanical polishing with a T-tool from both sides of the stacked specimen. Then a brief argon ion milling using a Gatan Precision Ion Polishing System (PIPS™) was used to thin the specimen to perforation. The ion milling energy was set to 3 keV and the total etching time was controlled to be less than 20 min by adjusting the mechanical polishing time to minimize the possible sample damage. For plan-view specimens, a dimpling technique was adopted using a dimple grinder (Gatan) for both mechanical thinning and polishing before the ion milling.

2.4.2 High resolution TEM

High-resolution TEM provides a unique and powerful way to characterize ultra-thin dielectric layers in terms of their morphology, thickness, and interface quality. In conventional high-resolution imaging, a nearly-parallel electron beam travels through the thin sample, and the transmitted beam and the diffracted beams interfere with each other and form a lattice image. Because the lattice in a material acts as a phase grating, the resulting image reflects the periodicity of the crystal lattice potential. In order to investigate the high-κ dielectrics and the interface with substrate, cross-sectional samples were prepared following the preparation sequence presented in the above section and were oriented along the <110> silicon zone axis of the underlying Si single crystal substrate. Rough zone axis alignment in the TEM was performed by centering Kikuchi lines in relatively thick specimen areas, and detailed alignment followed at the thin region of interest close to the film/substrate interface. To avoid interference effects (Fresnel fringes) and ion milling artifacts which often amorphize the substrate and dielectric films near the interface, a moderately thick area was carefully chosen to take high-resolution images. An internal magnification standard was obtained by measuring the lattice spacing of substrates (Si or Ge) along the (110) projection to measure the exact thicknesses of the dielectric and interfacial layer. Unless specifically stated otherwise, the TEM analyses in this thesis were performed using a Philips FEG CM20 microscope operating at 200 kV accelerating voltage, which offers a point-to-point spatial resolution of 2.4 Å.

2.4.3 Selected area diffraction pattern (SADP) and other imaging techniques

In identifying the existing phases in very thin films, a SADP is usually taken from plan-view TEM samples. For such samples, it is possible to collect diffraction over a relatively large area with accurate resolution. The SADP can easily reveal the presence

of long range atomic order (crystalline vs. amorphous phases) and also determine the Bravais lattice and lattice parameters of crystalline materials, if a sufficient number of crystallites having different orientations are present in the diffracting area. After following the procedure of making plan-view TEM samples, several diffraction patterns were taken by varying the selected area size and Si substrate orientation in the microscope. According to Bragg's law and the TEM geometry, the camera constant for a given magnification can be expressed as follows:[25]

$$K = \lambda L = Rd_{hkl} \qquad \text{Equation (2.4)}$$

where K is a camera constant, λ is the wavelength of the incident electron beam (0.025Å at 200 keV), L is the camera length, R is the distance between the diffraction spots/rings and the central transmitted beam at the screen, and d_{hkl} is the inter-planar lattice spacing of the reflecting (hkl) planes. By measuring the R corresponding to the substrate diffraction pattern, which has a well-known d_{hkl}, the camera length and the camera constant were calibrated for given magnifications. Measured R values from diffraction patterns of the high-κ samples were then converted to d_{hkl} values using the calibrated camera constant. These were then compared to available X-ray powder diffraction data from known material systems to identify the phases present in the selected area of the sample.

Imaging techniques using two-beam conditions, such as dark field imaging, were also adopted to identify the crystalline structures and defects present in some plan-view samples. The dark field imaging mode was especially important in identifying the crystalline phases from the amorphous matrix during crystallization kinetics studies of ALD-HfO_2 thin films. To obtain a dark field TEM image, the objective aperture was placed on one or several diffraction spots/rings under a condition in which two rings or spots have similar diffracted intensity (a two-beam condition). Because the objective lens aberration of the TEM can produce a distorted dark field image, the incident beam was tilted to center the objective aperture.

2.5 Capacitor fabrications and electrical characterization

Before fabrication and characterization of a metal-oxide-semiconductor (MOS) field effect transistor using high-κ gate stacks, it is advisable to first fabricate and analyze simple MOS capacitor structures. Electrical measurements on MOS capacitors can be used to determine the capacitance and leakage current properties of the dielectric as a function of applied voltage. This can provide valuable guidance in understanding and improving the gate dielectrics. In making simple MOS capacitors using ALD high-κ films, various sizes of Pt electrodes were deposited at room temperature by the shadow mask technique using an e-beam evaporation system. Due to the strong reactivity of certain metals (zirconium, hafnium and aluminum) with gate dielectrics of interesting this research and the resulting inferior electrical properties for MOS capacitors fabricated using these metals,[26, 27] thermodynamically inert metals should be used for the gate electrode to investigate the intrinsic properties of high-κ films.

Initially, a shadow mask was mounted on the sample and a sample holder having a small opening (1 in × 0.5 in) was tightly clamped to avoid a gap between the sample

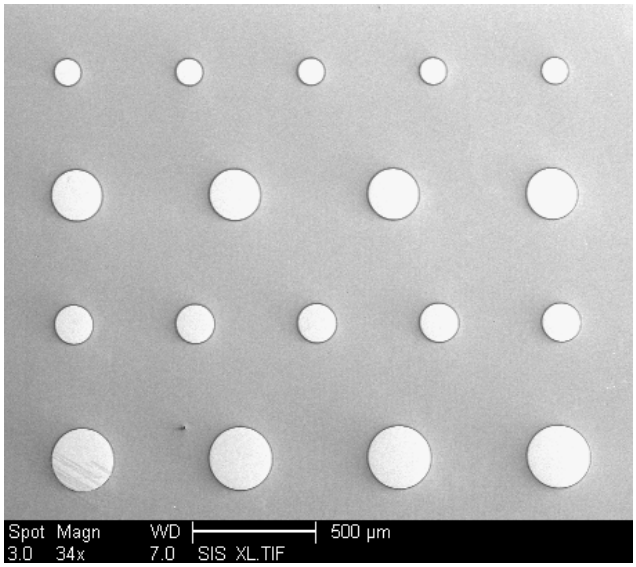

Figure 2.18: SEM image of capacitor structures after Pt electrode deposition.

and the shadow mask. The samples were transferred *ex-situ* from the ALD system to an e-beam evaporation system and ~ 50 nm-thick Pt was deposited at room temperature. In order to minimize the backside series resistance, the wafer backside was scratched to remove any native oxide using a diamond scribe and was coated with ~ 100 nm-thick Al film. The diameter of the capacitor electrodes was designed to be 100 μm, 150 μm, 200 μm, and 250 μm, and the actual size was calibrated using an optical microscope and a secondary electron microscope (Sirion SEM) as shown in Figure 2.18. The final distribution of measured capacitance values was evaluated across all the capacitors and it showed less than ± 5% variation from max-to-min, which is caused by nonuniform shadowing effects during the Pt deposition through a shadow mask. Unless specifically stated, all the electrical characterization was done on samples annealed in a forming gas ambient (4% H_2/96% N_2) at 400°C for 30min. Forming gas treatment is well known to passivate interfacial defects, such as Si dangling bonds, with H atoms and thereby reduce the total number of interface states in a MOS device.[28]

Capacitance-voltage measurements were performed using an HP4284A precision LCR meter at various frequencies. The capacitors were swept from inversion (+ 2 V) to accumulation (- 2 V) and back to check the amount of CV hysteresis. Typically, multiple sweeps saturated the amount of hysteresis due to initial permanent carrier trapping. Capacitance-voltage data reported in this thesis were collected during subsequent bias sweep. To minimize the effect of serial resistance during measurements, a parallel mode measurement[29] was adopted and the dissipation factor (D) was carefully monitored to ensure accurate results. Three different ac frequencies (10 kHz, 100 kHz, and 800 kHz) were used for the capacitance measurements and the D factor for each frequency in the accumulation region was observed to be < 0.005, < 0.05, and < 0.5 for reliable measurements. Because of the high series resistance occurring from the relatively resistive Si substrate and possible back-side contact resistance, frequency dispersion was observed for all the capacitor samples. For the extraction of an electrically equivalent oxide thickness (EOT), a resistance correction procedure using two different measurement frequencies, which was described by Yang and Hu[30] was applied. It assumes a three-element circuit model having a series resistance and corrects for the

measurement capacitance using dissipation factors (loss tangents) at two different frequencies as given by:

$$C = \frac{f_1^2 C_1^{'}(1 + D_1^{'2}) - f_2^2 C_2^{'}(1 + D_2^{'2})}{(f_1^2 - f_2^2)} \qquad \text{Equation (2.5)}$$

where C is the true capacitance, f_1 and f_2 are the two measurement frequencies, and C_1', D_1', C_2', D_2' are the capacitance and dissipation factors measured at two different frequencies, respectively. After correcting for the sample series resistance, the equivalent oxide thicknesses (EOT) of high-κ gate stacks were calculated using the following formula:

$$EOT = \varepsilon_{SiO_2} \varepsilon_O \frac{A}{C} \qquad \text{Equation (2.6)}$$

where A is the measured capacitor area, ε_{SiO2} is the dielectric constant of SiO_2, and ε_o is the permittivity of vacuum. According to the quantum mechanical theory, the centroid of the inversion charge is located approximately 8 Å from the gate dielectric/Si interface in the channel region for a transistor under a typical gate bias.[31] This can create an additional increase in the EOT of approximately 3 to 6 Å. In this thesis, the EOT of high-κ gate stacks was calculated without considering possible quantum mechanical effect. The capacitance (C) for the EOT extraction was measured from the maximum accumulation voltage depending on the scanning bias range. Because all the ALD films were deposited either on a chemical oxide or on a thermal oxide on Si, there could be a possible interfacial mixing during deposition to form a silicate phase and a resulting increase of the dielectric constant of the interfacial oxide.[32] To avoid the complexity of analyzing each layer separately, the effective EOT of a whole gate stack was calculated and compared in all experimental results.

For current-voltage measurements, a Keithley 230 programmable voltage source and a 6512 programmable electrometer were used. Since the Si substrates used in this work were doped with low concentrations of p-type impurities, the gate electrode was negatively biased and swept under gate injection conditions. Conduction mechanism modeling through leakage current measurement at different temperatures can provide

valuable information about the electrical quality of dielectrics. Therefore, I-V characteristics of selected samples were measured as a function of temperature. The actual temperature of the sample during the measurement was monitored by a thermocouple attached to a reference Si wafer mounted on the chuck.

References

[1] J. Shappir, A. Anis, and I. Pinsky, IEEE Trans. Electron Devices **33**, 442 (1986).

[2] B. H. Lee, L. Kang, W.-J. Qi, R. Nieh, Y. Jeon, K. Onishi, and J. C. Lee, Tech. Dig. Int. Electron Devices Meet. **1999**, 133 (1999).

[3] S. Ramanathan, G. D. Wilk, D. A. Muller, C.-M. Park, and P. C. McIntyre, Appl. Phys. Lett **79**, 2621 (2001).

[4] C. M. Perkins, B. B. Triplett, P. C. McIntyre, K. C. Saraswat, S. Haukka, and M. Tuominen, Appl. Phys. Lett. **78**, 2357 (2001).

[5] T. Suntola and J. Antson, Patent US 4058430 (1977).

[6] C. M. Perkins, Stanford university (2001).

[7] H. Kim, A. J. Kellock, and S. M. Rossnagel, J. Appl. Phys. **92**, 7080 (2002).

[8] S. M. George, A. W. Otto, and J. W. Klaus, J. Phys. Chem. **100**, 13121 (1996).

[9] T. Suntola, *Handbook of Crystal Growth*, vol.3, Chapter 14 (North-Holland, New York, 1994).

[10] J. I. Skarp, P. J. Soininen, and P. T. Soininen, Appl. Surf. Sci. 112, 251 (1997).

[11] M. Copel, M. Gribelyuk, and E. Gusev, Appl. Phys. Lett. **76**, 436 (2000).

[12] M. L. Green, M.-Y. Ho, B. Busch, G. D. Wilk, T. Sorsch, T. Conard, B. Brijis, W. Vandervorst, P. I. Räisänen, D. Muller, M. Bude, and J. Grazul, J. Appl. Phys. **92**, 7168 (2002).

[13] NIST chemistry webbook, http://webbook.nist.gov/.

[14] M. Copel, M. Gribelyuk, and E. P. Gusev, Appl. Phys. Lett. **76**, 436 (2000).

[15] Rudolph Auto-EL III ellipsometer user's manual.

[16] M. Ritala and M. Leskelä, Appl. Surf. Sci. **75**, 333 (1994).

[17] M. Ylilammi, Thin Solid Films **279**, 124 (1996).

[18] Y. Widjaja and C. B. Musgrave, Appl. Phys. Lett. **81**, 304 (2002).

[19] Y. Widjaja and C. B. Musgrave, J. Chem. Phys. **117**, 1931 (2002).

[20] J. W. Klaus, A. W. Ott, A. C. Dillon, and S. M. George, Surface Science **418**, L14 (1998).

[21] R. Matero, A. Rahtu, M. Ritala, M. Leskelä, and T. Sajavaara, Thin Solid Films **368**, 1 (2000).

[22] R. G. Gordon, Chem. Vap. Deposition **9**, 73 (2003).

[23] A. C. Diebold, A. Venables, Y. Chabal, D. Muller, M. Weldon, and E. Garfunkel, Materials Science in Semiconductor Processing **2**, 103 (1999).

[24] D. A. Muller, T. Sorsch, S. Moccio, F. H. Baumann, K. Evans-Lutterodt, and G. Timp, Nature **399**, 758 (1999).

[25] D. B. Williams and C. B. Carter, *Transmission Electron Microscopy, II Diffraction* (Plenum Press, New York, 1996).

[26] V. Misra, G. P. Heuss, and H. Zhong, Appl. Phys. Lett. **78**, 4166 (2001).

[27] G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. App. Phys. **89**, 5243 (2001).

[28] K. L. Brower, Appl. Phys. Lett. **53**, 508 (1988).

[29] E. H. Nicollian and J. R. Brews, *MOS(Metal Oxide Semiconductor) Physics and Technology* (Wiley and Sons, New Jersey, 2003).

[30] K. J. Yang and C. M. Hu, IEEE Trans. Electron Devices **46**, 1500 (1999).

[31] S. A. Hareland, S. Krishnamurthy, S. Jallepalli, C.-F. Yeap, K. Hasnat, A. F. Tasch, and C. M. Maziar, Tech. Dig. – Int. Electron Devices Meet. **1995**, 933 (1995).

[32] W.-J. Qi, R. Nieh, B. H. Lee, L. Kang, Y. Jeon, K. Onishi, T. Ngai, S. Banerjee, and J. C. Lee, Tech. Dig. – Int. Electron Devices Meet. **1999**, 145 (1999).

Chapter 3

Microstructural and Electrical Properties of ALD-ZrO_2 and HfO_2 on Silicon Substrates

3.1 Introduction

Among many possible high-κ gate dielectric metal oxide systems, ZrO_2 and HfO_2 in particular, are drawing attention due to their high dielectric constants (15 ~ 30), large bandgaps (5.7 ~ 6 eV), and large conduction band offsets to silicon (1.4 ~ 1.5 eV).[1] In bulk form, these metal oxides exhibit similar thermodynamic and microstructural properties, as discussed in Chapter 1. However, in thin films deposited by techniques such as ALD, the behavior of these two metal oxides changes. In this chapter, the microstructural and electrical properties of ultra-thin ZrO_2 and HfO_2 dielectric films are systematically compared using identical deposition parameters and similar chloride precursor systems in the Stanford ALD chamber. The crystallization kinetics of the amorphous as-deposited HfO_2 films was investigated using post-deposition *in-situ* transmission electron microscopy (TEM) annealing. Detailed microstructural characterization of fully crystallized HfO_2 specimens was performed using high resolution TEM. Also, the effects of crystallization on the electrical properties of HfO_2

gate dielectric were studied using both *ex-situ* and *in-situ* crystallization anneals and IV measurements.

3.2 Microstructural properties of ALD-ZrO_2 and HfO_2

In order to compare the microstructural and electrical properties of as-deposited ALD-ZrO_2 and HfO_2 thin films, a range of thicknesses was deposited on 3-inch diameter

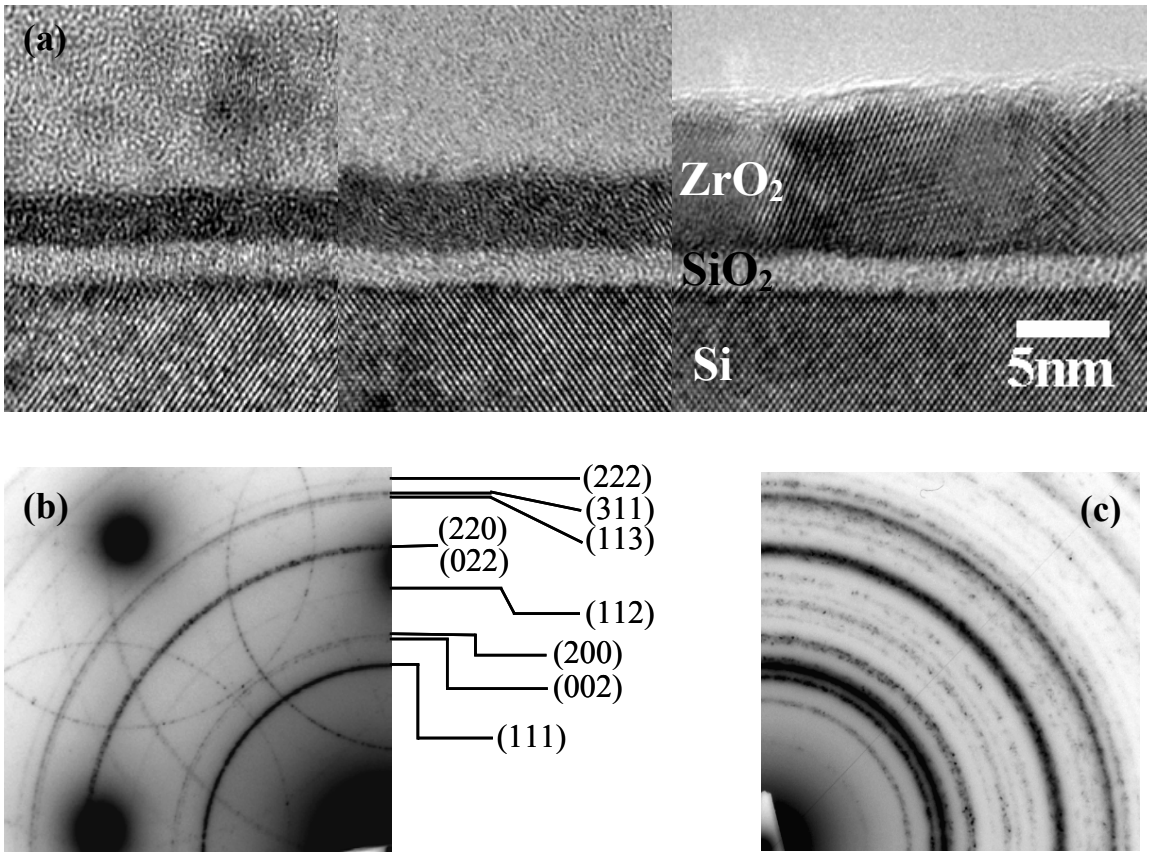

Figure 3.1: Microstructural analysis of ALD-grown ZrO_2 films of different thicknesses (samples were grown on Si passivated by a ~ 1.5 nm chemical oxide layer): (a) cross-sectional high resolution TEM images of ALD-ZrO_2 films with different thicknesses, 2.9 nm, 4.3 nm and 8.2 nm, respectively, (b) selected area electron diffraction pattern (SADP) of ALD-ZrO_2 less than 14 nm thickness, and (c) SADP of ALD-ZrO_2 greater than 14 nm thickness.

silicon wafers having a chemical oxide surface passivation (~ 1.5 nm in thickness); no cleaning was performed on the wafers. All the ALD depositions were performed at 300°C to minimize Cl contamination, which could increase the bulk defect density and the resulting leakage current density measured across the films. Figure 3.1 shows representative cross-sectional TEM images and plan-view electron diffraction patterns obtained from ZrO_2 specimens of different film thicknesses. The as-deposited samples are polycrystalline and their crystal structure is dependent on the ZrO_2 film thickness. According to the careful indexing of diffraction patterns (Figure 3.1 (b)), the major phase in films of sufficiently small thickness is tetragonal ZrO_2 possibly dispersed in an amorphous matrix.[2] Although the exact film thickness at which the phase transition from tetragonal to monoclinic ZrO_2 was not determined in these experiments, ALD-grown films of ~ 14 nm and greater thickness showed the coexistence of both the tetragonal and the monoclinic phases of zirconia (Figure 3.1 (c)). According to reported thermodynamic data for bulk ZrO_2, the stable phase of ZrO_2 is monoclinic at the ALD deposition temperature (~ 300°C) and the tetragonal phase is the lowest-energy bulk phase at higher temperatures (> 1170°C).[3] Maintaining the tetragonal ZrO_2 at low temperatures is usually accomplished by adding a dopant such as yttrium and/or by minimizing the grain size.[4] In response to a stress concentrator, these tetragonal zirconia crystallites transform locally to monoclinic zirconia via a martensitic transition involving an anisotropic lattice expansion.[5] Aita *et al.*[6] explained the stabilization of tetragonal ZrO_2 films using end-point thermodynamics by assuming a hemispherical cap-shaped crystallite and considering the effects of the finite crystallite size on phase stability. They demonstrated that unity volume fraction of tetragonal zirconia which is favored under the capillary pressure is produced when the thickness of each zirconia is less than the radius at which an unconstrained, unstressed hemispherical tetragonal zirconia crystallite spontaneously transforms to monoclinic. According to their model, the calculated critical radius below which the tetragonal phase was predicted to be stable is ~ 6.3 nm at 300°C, which is smaller than the grain sizes at which the tetragonal ZrO_2 is observed in our experiments. This may be caused either by 1) their assumption of hemispherical cap-shaped crystallites or 2) the slow kinetics of the transformation of an initially tetragonal film to the

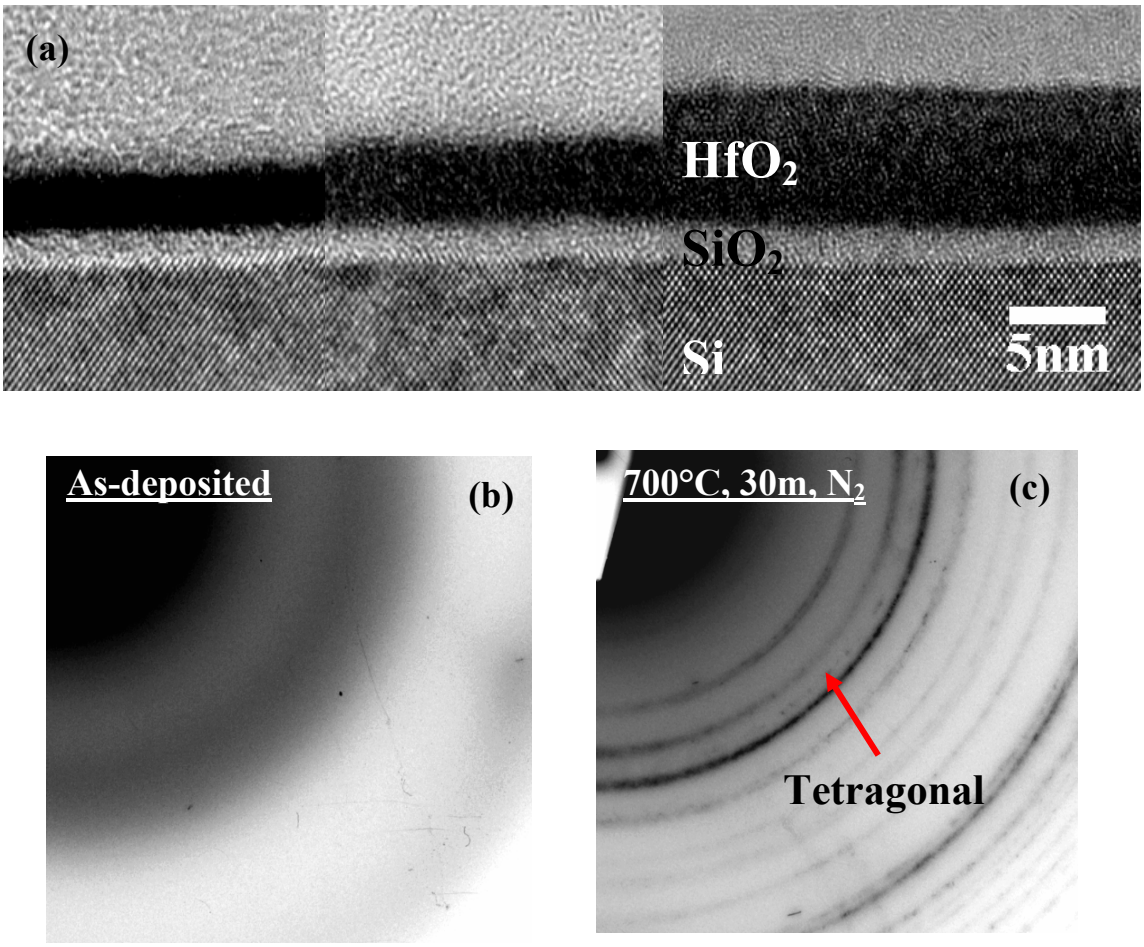

Figure 3.2: Microstructural analysis of ALD-grown HfO_2 films of different thickness (The samples were grown on Si having a chemical oxide (~ 1.5 nm) passivation): (a) cross-sectional high resolution TEM images of ALD-HfO_2 films of different thickness, 2.8 nm, 4.5 nm and 6.2 nm, respectively, (b) SADP of as-deposited ALD-HfO_2 (~ 3 nm), and (c) SADP of ALD-HfO_2 (~ 3 nm thickness) after crystallization (annealed at 700°C for 30 min in N_2).

monoclinic phase as the grain size grows during deposition under the process conditions used in the present work.

Although bulk hafnia has crystallographic and thermodynamic properties similar to bulk ZrO_2, an amorphous phase was consistently observed across the thickness range investigated for the ALD-HfO_2 deposited in this study, as shown in Figure 3.2. Recently, Ho *et al.*[7] reported more detailed microstructural analysis using annular dark field (ADF)

STEM and fluctuation electron microscopy (FEM). They investigated rather thick (~ 20 nm) ALD-HfO_2 on chemical oxide (~ 0.55 nm) and observed large fluctuations in the diffracted intensity, which indicated that the resulting structure was heterogeneous and ordered. Their suggestion was that ALD-grown HfO_2 contains small (~ 1 nm or less) crystal-like clusters and competition between clusters of the monoclinic, orthorhombic, and tetragonal phases may prevent complete crystallization. However, in terms of long range atomic order, it is generally reported that as-deposited HfO_2 films of thickness suitable for transistor gate dielectrics exist in amorphous state. Crystallization of ~ 3 nm-thickness HfO_2 films was detectable by post-anneal electron diffraction at annealing temperatures greater than 500°C. Monoclinic hafnia was the dominant phase observed, although a small volume fraction of the tetragonal phase was also detected in the selected area electron diffraction patterns (Figure 3.2 (c)). In contrast to the as-deposited (or annealed) ALD-ZrO_2 films, which assumed the tetragonal phase as opposed to the monoclinic phase expected from the bulk phase diagram, ALD-grown HfO_2 films exhibit the bulk equilibrium phase (monoclinic) after the crystallization anneal. Detailed microstructural analysis after crystallization and the crystallization kinetics of ALD-HfO_2 will be discussed in the following sections.

3.3 Electrical Properties of ALD-ZrO_2 and HfO_2

3.3.1 C-V characteristics

In order to measure the dielectric constant of the ALD high-κ layer and the interfacial layer, a series of capacitors having different thicknesses of ZrO_2 and HfO_2 were fabricated and characterized. As evident from Figures 3.1 and 3.2, varying the metal oxide film thickness had no measurable change on the thickness of the underlying interface layer. Figure 3.3 shows the C-V characteristics of ZrO_2 and HfO_2 with different thicknesses measured after forming gas annealing (400°C, 30 min in 4% H_2/N_2). For

films grown at a lower temperature (~ 250°C), the hysteresis observed in the C-V characteristics increased significantly with film thickness, suggesting an increase in the density of bulk traps, possibly caused by Cl contamination due to incomplete ALD reaction.[8] By increasing the deposition temperature to 300°C and optimizing the H_2O flow rate, acceptable hysteresis levels (< ~ 30 mV) that were not thickness-dependent for either ZrO_2 or HfO_2 gate stacks were achieved. From the measured minimum capacitance in the inversion bias regime and the maximum oxide capacitance measured at -2 V, the surface doping density of the Si substrate was calculated to be $1 \sim 3\times10^{15}$ (cm^{-2}) and matched reasonably with the normal substrate resistivity (1 ~ 10 ohm-cm). Considering the workfunction difference between the Pt electrode and the Si substrate of this doping density, the calculated ideal flatband voltage is ~ 0.66 V. The flatband voltage of the measured C-V curves was extracted and compared with the ideal value by calculating the flatband capacitance. Most of the samples showed a negative shift relative to the ideal flatband condition which indicates positive fixed or trapped charge. This is consistent with other published results for hafnia and zirconia gate dielectrics prepared by ALD.[9] The calculated positive charge density in the films obtained from our C-V measurements was ~ 10^{12} (cm^{-2}).

Increasing the ZrO_2 and HfO_2 film thickness, however, resulted in flatband

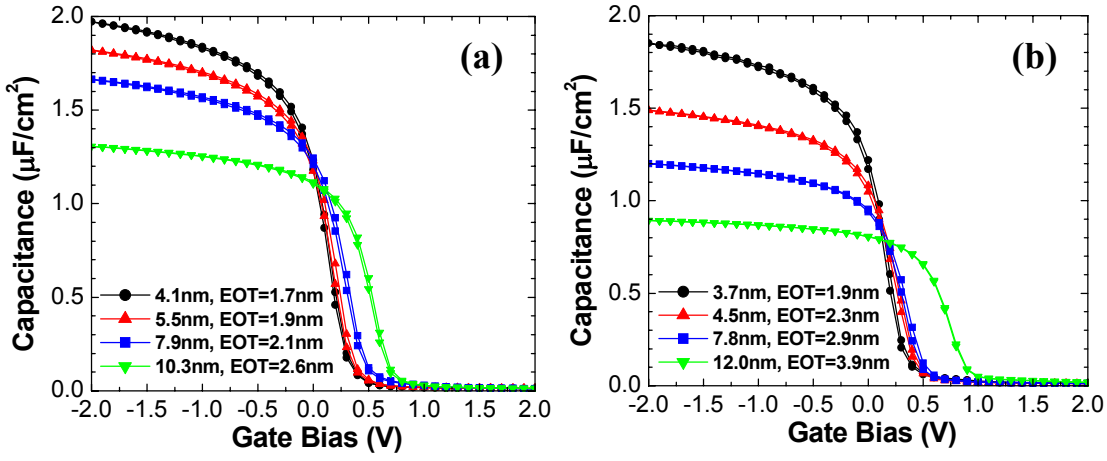

Figure 3.3: Capacitance vs. voltage characteristics of (a) ALD-ZrO_2 and (b) ALD-HfO_2 as a function of thickness.

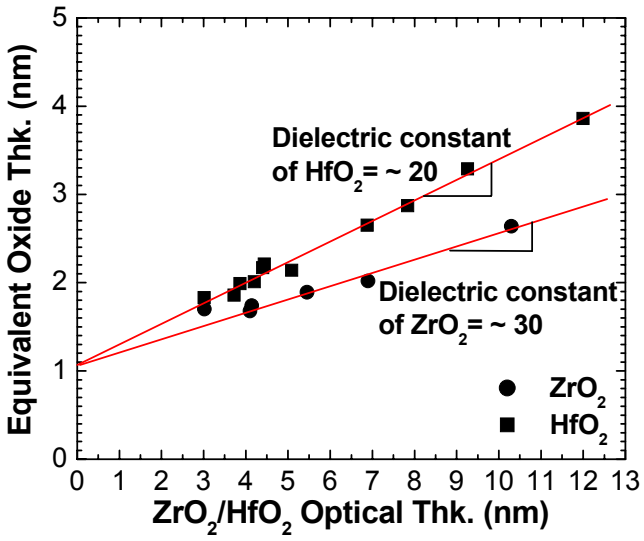

Figure 3.4: Equivalent oxide thickness (EOT) as a function of physical thicknesses of ALD-grown ZrO_2 and HfO_2 films.

voltage shifts toward more positive values, indicating the introduction of net negative charge either in the metal oxide or at the metal oxide/interface layer interface. A large amount of fixed charge in these films could have an enormous influence on the feasibility of their insertion into a CMOS process. Although many different reports regarding the sign and magnitude of charges causing flatband voltage shifts in high-κ dielectrics for various processing conditions are available in the literature,[9,10,11,12,13] ascertaining the exact formation mechanism and identity of the charges in the oxides deposited here requires more investigation.

Figure 3.4 shows the measured equivalent oxide thickness (EOT) versus the physical thickness of each metal oxide layer. Assuming that the fabricated gate stack is composed of two capacitors connected in series, the following relationship can be derived:

$$EOT_{stack} = \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-\kappa}} t_{high-\kappa} + EOT_{it} \qquad \text{Equation (3.1)}$$

where EOT_{stack} refers to the total gate stack, EOT_{it} refers to the interfacial layer, and $t_{high\text{-}\kappa}$ is the physical thickness of high-κ layer. By measuring the slope from trend lines throughout the experimental data, the dielectric constants of ZrO_2 and HfO_2 were calculated to be approximately 30 and 20, respectively. These values are consistent with the experimentally determined results for tetragonal ZrO_2 and amorphous HfO_2 films as discussed in Chapter 1 (section 1.4.2).[14] Although the ALD-ZrO_2 film has a high dielectric constant close to the bulk ZrO_2 value, the ALD-HfO_2 film exhibits a dielectric constant considerably lower than that of bulk HfO_2.[1] This was found to be independent of the processing conditions. We believe that the low dielectric constant of ALD-HfO_2 is caused by the low atomic density of the ALD-HfO_2 film, which is not unexpected given the amorphous microstructure of the film discussed in the previous section. The EOT of interfacial oxide was extrapolated to be ~ 1.1 nm, smaller than the physical thickness measured by the HR-TEM (1.4 ~ 1.5 nm). It has been reported that the interfacial SiO_2 layer may be moderately mixed with Zr and Hf atoms during metal oxide film deposition and form a mixed amorphous alloy (commonly called a silicate phase) having a relatively high dielectric constant.[12]

3.3.2 I-V characteristics

Figure 3.5 shows the leakage current characteristics of ALD-ZrO_2 and HfO_2 dielectrics as a function of their physical thickness, measured under gate injection conditions at room temperature. The magnitude of the leakage current scaled as predicted with the thickness variation. Hard breakdown occurred around 4 V for 3 nm-thick samples, indicating a breakdown field of over ~ 10 MV/cm. The leakage current was measured at $|V_{app}\text{-}V_{FB}| = 1$ (V) and is plotted as a function of EOT for both oxides in Figure 3.6. Compared with reference leakage current data for SiO_2,[15] the leakage current of ZrO_2 and HfO_2 dielectrics was several orders of magnitude lower due to the increase in physical thickness.

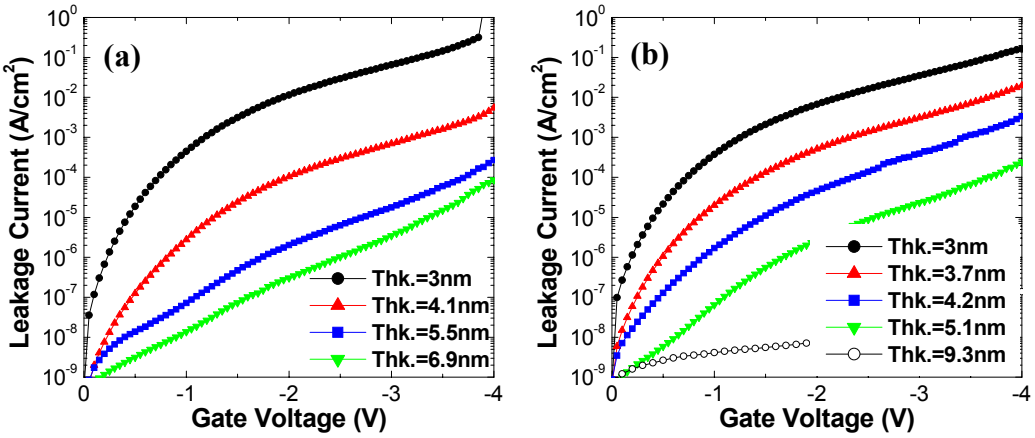

Figure 3.5: Leakage current density vs. voltage characteristics of (a) ALD-ZrO_2 and (b) ALD-HfO_2 as a function of thickness.

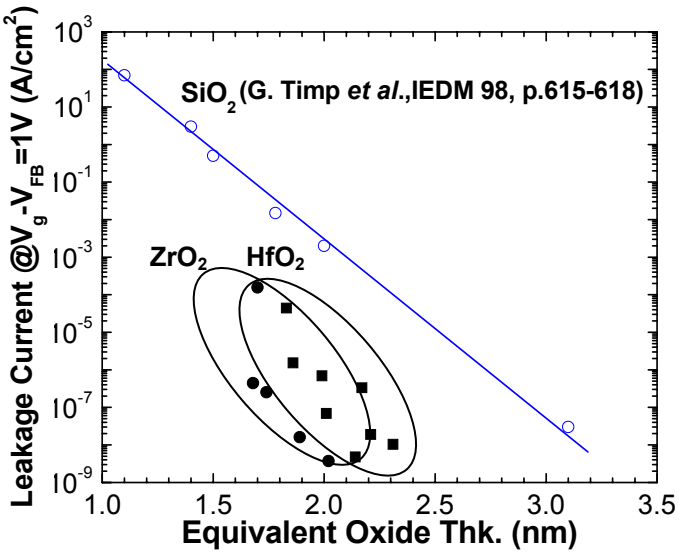

Figure 3.6: Leakage current density of ALD-ZrO_2 and HfO_2 as a function of electrically measured equivalent oxide thickness (EOT).

In order to identify the leakage current conduction mechanism and the conduction barrier height between the Pt electrode and the dielectric films, two types of MOS capacitor structures with different interfacial layers were prepared: chemical oxide approximately 1.5 nm thick and thermally grown SiO_2 approximately 2.5 nm thick. Figure 3.7 shows the leakage current behavior of ~ 3 nm-thick ALD-ZrO_2 and HfO_2 MOS capacitors with thick interfacial oxide. Because of the thick interfacial oxide layer,

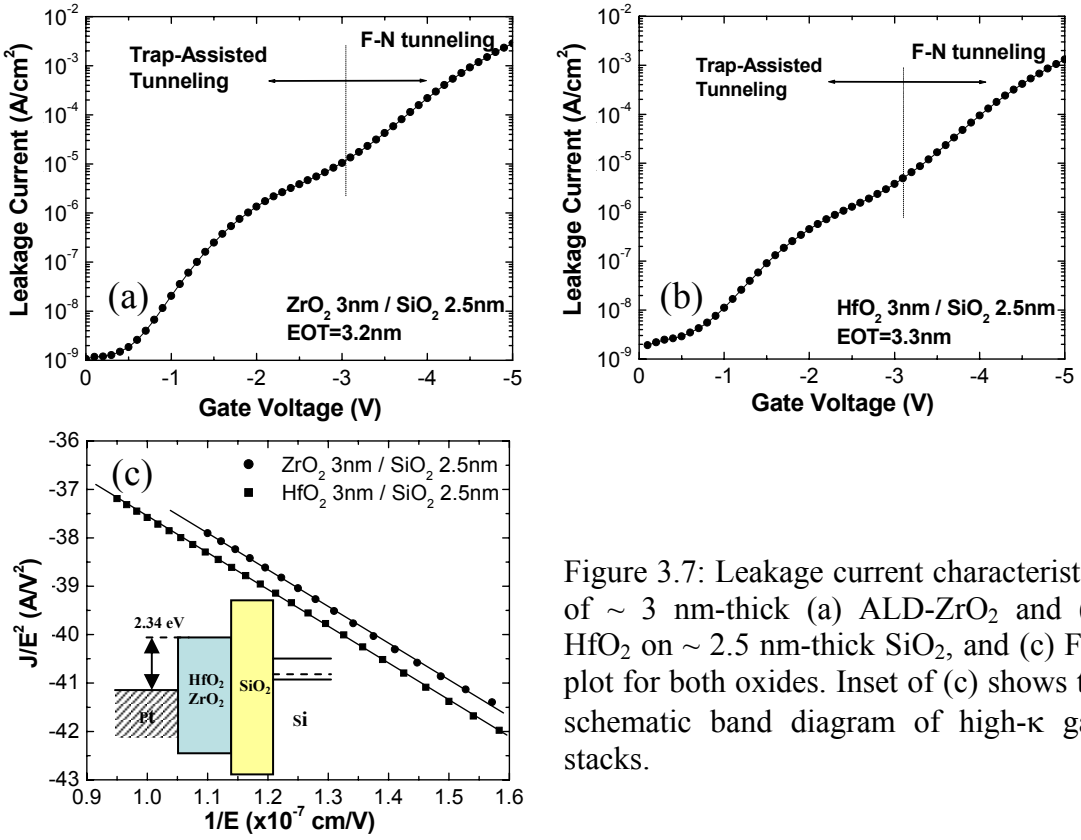

Figure 3.7: Leakage current characteristics of ~ 3 nm-thick (a) ALD-ZrO_2 and (b) HfO_2 on ~ 2.5 nm-thick SiO_2, and (c) F-N plot for both oxides. Inset of (c) shows the schematic band diagram of high-κ gate stacks.

the Fowler-Nordheim (F-N) tunneling component makes a major contribution to the total leakage current. This is apparent in the higher field region. Both metal oxide films showed a distinct change in leakage current mechanism to F-N tunneling at ~ 3.2 V consistent with reported results.[16] By fitting both sets of measured results with the F-N tunneling equation[17] shown below, an effective interface potential barrier of ~ 2.34 eV with the Pt electrode was obtained for both oxides by assuming the effective electron mass in ZrO_2 and HfO_2 films is $0.1m_o$ (m_o is the effective mass of the electron in vacuum).[18]

$$J_{F-N} = AE_{ox}^2 \exp(-\frac{B}{E_{ox}}) \qquad \text{Equation (3.2)}$$

where $A = q^3 / 8\pi h m_{ox}^* \phi_B$, $B = 8\pi\sqrt{2m_{ox}}\phi_B^{3/2} / 3hq$, q is the electron charge, h is Plank's constant, ϕ_B is the barrier height at the interface of the injecting electrode and the oxide film, m_{ox} is the average electron mass in the bandgap of the oxide, m_{ox}^* is the ratio of the effective mass of the electron in the oxide to that in vacuum. Our calculated barrier height value is very similar to a recently published experimental value measured at low temperatures: 2.48 eV.[18] At low electric fields, a trap-assisted tunneling conduction mechanism is consistent with the data observed from these films in variable-temperature IV measurements, similar to other published experimental results.[16]

Using 4.1 nm-thick ALD-ZrO_2 and 3.9 nm-thick HfO_2 on thin interfacial oxide (~ 1.5 nm), the leakage current was measured as a function of temperature. As shown in Figure 3.8, the films exhibited very similar leakage current behavior as a function of temperature and applied voltage despite their different microstructures and compositions. At higher fields and low temperatures, the temperature dependence of the leakage current was negligible. Considering the band diagram of ZrO_2/SiO_2 and HfO_2/SiO_2 gate stacks, it is reasonable to expect Fowler-Nordheim (FN) tunneling to dominate the conduction process for biases greater than 3 V across films of this thickness as shown in Figure 3.7.

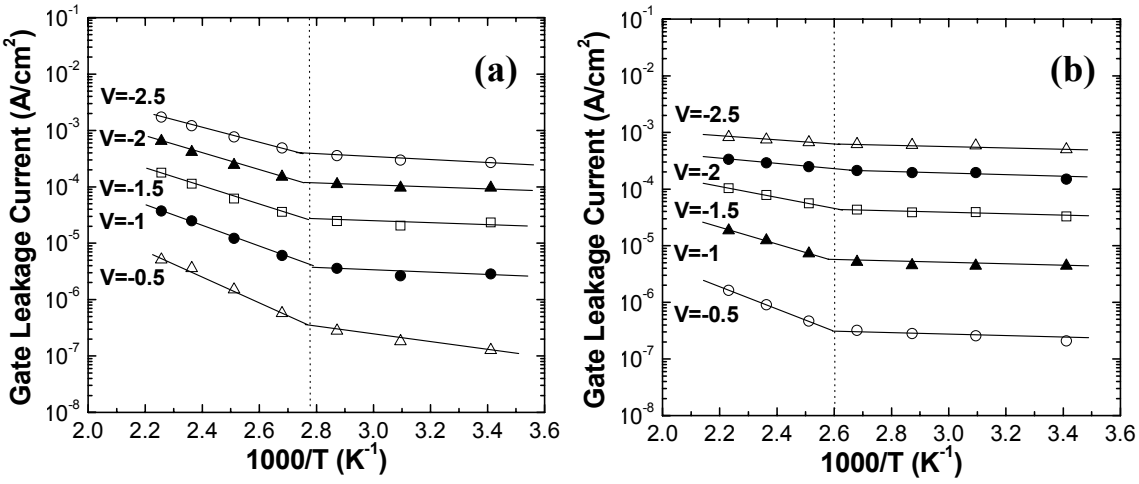

Figure 3.8: Leakage current density as a function of 1/T with different applied gate voltage: (a) ALD-ZrO_2 and (b) ALD-HfO_2 on ~ 1.5 nm chemical oxide.

For the lower gate voltages examined in Figure 3.8, the possible leakage current mechanisms are direct tunneling (DT), trap-assisted tunneling (TAT), and Poole-Frenkel (PF) conduction. While direct tunneling current has a weak temperature dependence,[16] TAT and PF conduction are strong functions of temperature depending on the trap energy level and density.[19] The PF hopping current is given by

$$J_{PF} \approx AE \exp\left[-\frac{q(\phi_t - \sqrt{qE/(\pi\varepsilon_i)})}{kT}\right] \qquad \text{Equation (3.3)}$$

where ϕ_t is the energy level of a trap with respect to the conduction band of the insulator, E is the effective electric field across the insulator, and ε_i is the high frequency dielectric constant.[17] Although this equation can be fitted to the temperature dependent leakage data in Figure 3.8 at higher temperatures, the extrapolated high frequency dielectric constants of HfO_2 and ZrO_2 are unreasonably large (> 9) compared to the reported values (~ 4).[1] In addition, it was reported that shallow traps (0.5 ~ 0.8 eV) are located above the Fermi level of Pt for relatively low fields;[19] these cannot contribute to the leakage conduction mechanism. Therefore, the data suggests that DT through the thin ZrO_2 and HfO_2 layer or TAT via deep traps is the dominant leakage current mechanism at low temperatures (< 125°C). For increasing measurement temperatures, TAT through shallow traps may become the dominant leakage mechanism for both the crystalline ZrO_2 and amorphous HfO_2 films.

3.4 Crystallization kinetics of ALD-HfO_2

As-deposited HfO_2 films prepared by methods, such as low temperature chemical vapor deposition and atomic layer deposition (ALD) are usually amorphous and undergo crystallization during post-deposition-annealing at modest temperatures (~500°C).[20,21,22] Because the conventional MOSFET fabrication process requires high-temperature annealing steps in order to activate source/drain dopants after the gate stack formation,[23] thermal stability study of high-κ films is extremely important. A significant increase in

leakage current measured at room temperature was observed during the crystallization process of relatively thick chemical vapor deposited Ta_2O_5 system, which was believed to be caused by the high leakage current path along the grain boundaries.[24] Therefore, many researchers are searching for thermally stable, amorphous metal oxides that do not crystallize. Metal silicates[25] and metal oxide doped with crystallization inhibitors, [26] such as Al and N are two candidates. The crystallization kinetics and the effects of crystallization on the leakage current for ALD-HfO_2 films are crucial issues and not currently understood in detail.

3.4.1 Ex-situ annealing study

In order to identify the crystallization temperature and the crystalline phases present in the ALD-grown HfO_2 dielectric layers, 2.8 ~ 3 nm-thick HfO_2 films were deposited at 300°C and annealed at temperatures in the range of 450°C to 900°C in N_2 ambient for 30 minutes using a conventional atmospheric pressure furnace. The metal oxide films were directly exposed to the annealing ambient without any capping layer. After making plan-view TEM samples from the samples subjected to different annealing conditions, selected area electron diffraction (SAED) patterns were collected as shown in Figure 3.9. The corresponding dark field images of identical samples were also taken to confirm the degree of crystallization and to study microstructural changes, as shown in Figure 3.10. The as-deposited state exhibited a typical amorphous diffraction pattern and a few widely-separated nanometer-sized crystallite "seeds" were detected after extensive high resolution TEM plan-view studies. Significant crystallization of the 3 nm-thick ALD-grown HfO_2 films was detected after annealing for 30 min at ~ 500°C. The majority of the crystalline phase formed was found to be monoclinic, in agreement with reports in the literature.[21, 22] After 30 min N_2 anneals at 600°C and 700°C, the HfO_2 film appeared to be fully-crystallized based on the plan-view images. An additional, second-phase diffraction ring was detected during the SAED studies of the samples annealed at temperatures in this range. Some researchers[21, 22] have reported formation of residual

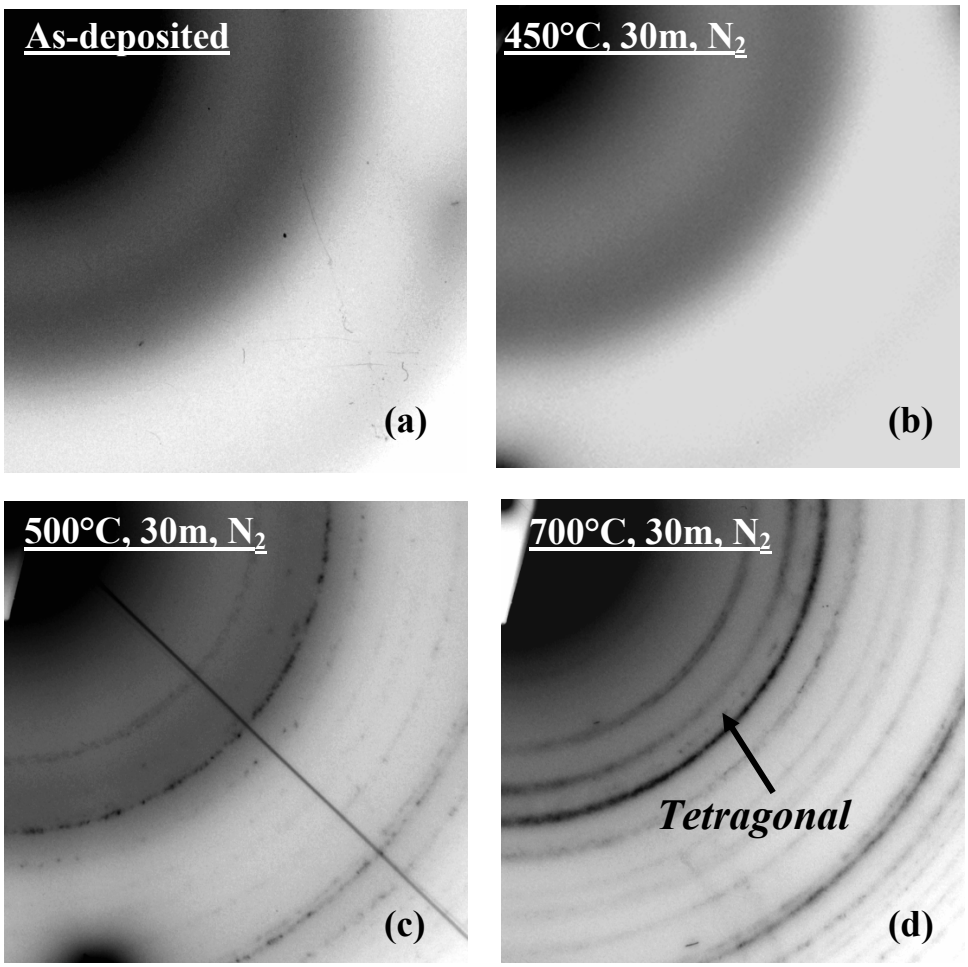

Figure 3.9: Selected area electron diffraction patterns of 3 nm HfO_2 film after N_2 annealing at various temperatures for 30 min: (a) as-deposited, (b) 450°C, (c) 500°C, and (d) 700°C.

cubic, orthorhombic or tetragonal phases during crystallization of the amorphous HfO_2. Careful measurement of interplanar spacings detected from SAED patterns of the present ALD-grown films of this phase suggests that the only crystalline second phase observed in this experiment is tetragonal HfO_2.

Figure 3.11 shows plan-view bright field and dark field images of ALD-HfO_2 films after complete crystallization during anneals at 700°C. In the bright field image, distinct white boundaries can be seen separating large domains of constant image contrast. The dark field image, conversely, exhibits many distorted sub-grains having different

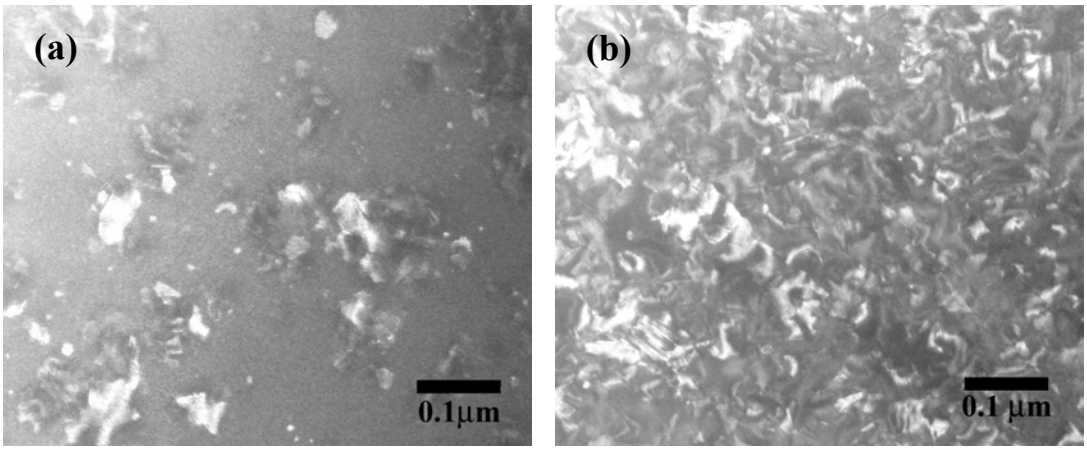

Figure 3.10: Dark field TEM images of 3 nm HfO_2 film after N_2 annealing for 30 min: (a) 500°C and (b) 700°C.

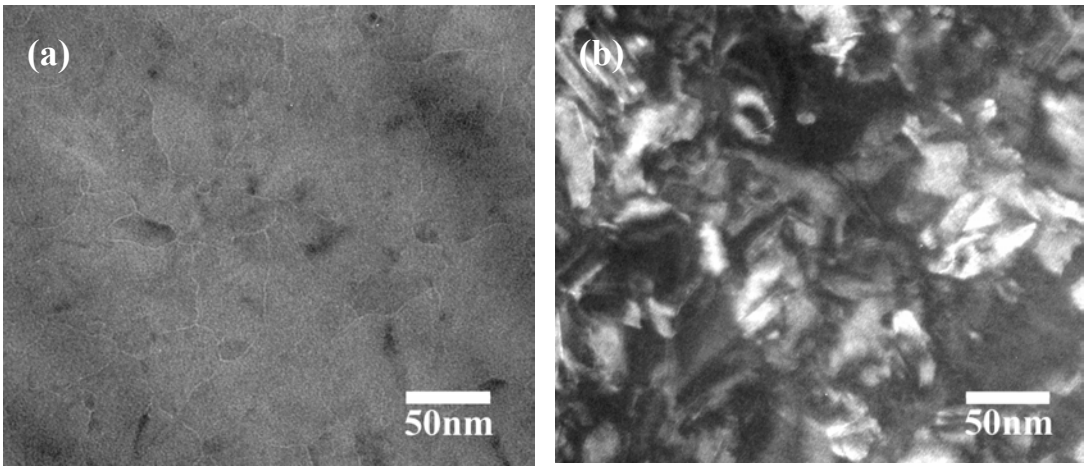

Figure 3.11: (a) Bright field and (b) dark field TEM image of 3 nm HfO_2 film after N_2 annealing at 700°C for 30 min.

orientations with much smaller grain sizes. In order to investigate the detailed microstructures of individual clusters, high resolution TEM pictures were taken from several regions. Our results indicate that the crystallized microstructure is composed of clusters of very small grains (less than ~ 10 nm) separated by either low angle grain boundaries or twin boundaries, as shown in Figure 3.12. These clusters of nanometer-scale grains with small mutual misorientation were a few hundred Å in diameter (about one order of magnitude larger than the film thickness) and were separated from each

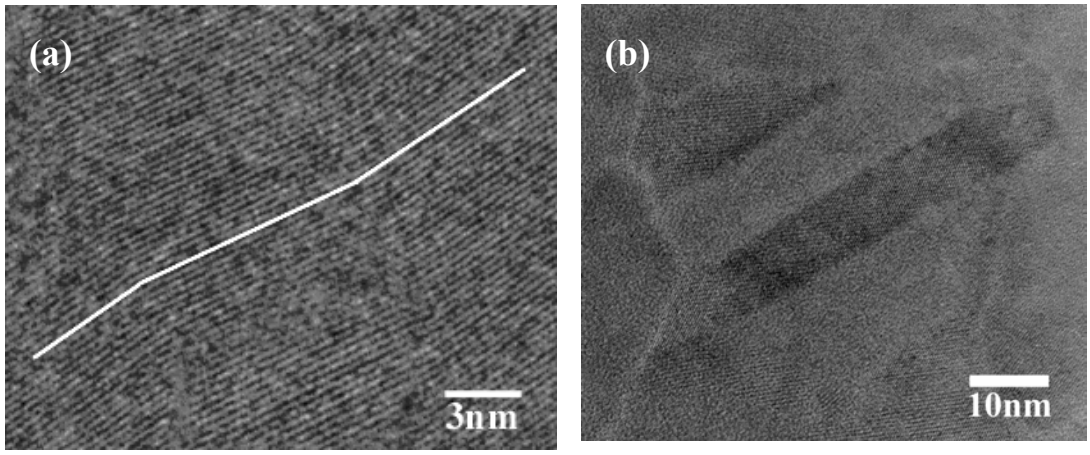

Figure 3.12: High resolution plan-view TEM images of ~ 3 nm HfO_2 film after N_2 annealing at 700°C for 30 min: (a) distorted grain structure and (b) twin structure in a large grain.

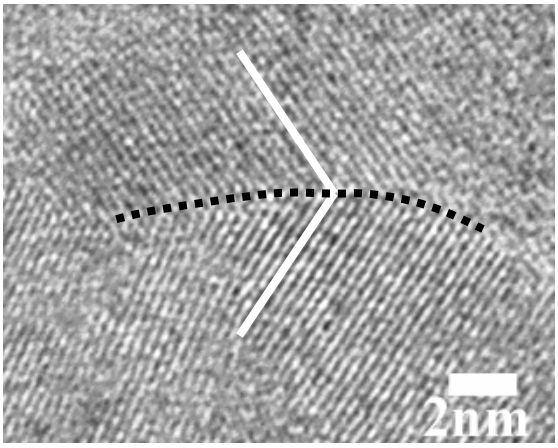

Figure 3.13: High resolution plan-view TEM images of HfO_2 film after N_2 annealing at 700°C for 30 min showing high angle grain boundary.

other by surrounding high-angle grain boundaries from the adjacent clusters, as depicted in Figure 3.13.

3.4.2 Crystallization kinetics study using in-situ TEM

In this experiment to characterize the microstructural evolution kinetics, HfO_2 films of ~ 3 nm thickness were deposited onto Si wafers passivated by a relatively thick

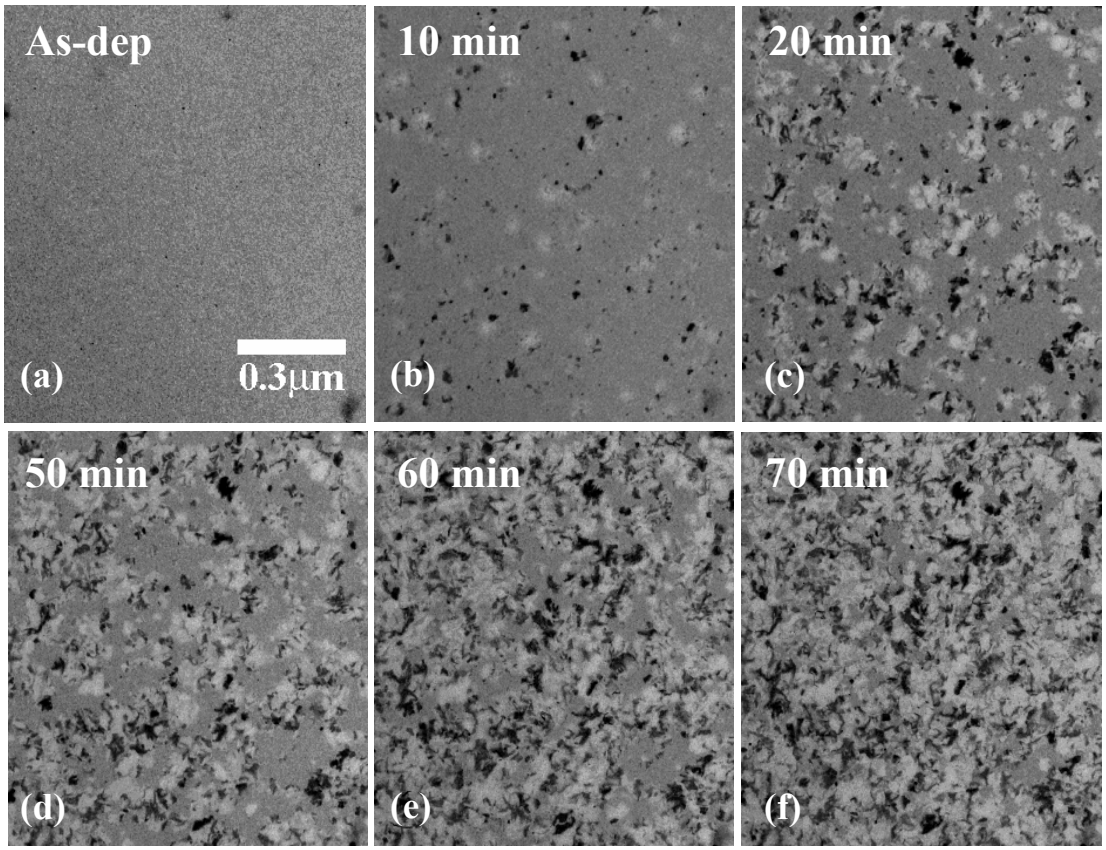

Figure 3.14: Dark field images of 3 nm HfO_2/2.5 nm SiO_2 stack at different stages of crystallization. Samples were annealed *in-situ* in the TEM at 520°C for different times: (a) 0 min, (b) 10 min, (c) 20 min, (d) 50 min, (e) 60 min, and (f) 70 min.

(2.5 nm) initial thermal oxide layer. In order to investigate the isothermal crystallization kinetics of HfO_2, plan-view TEM samples were prepared using a conventional dimpling and ion milling technique and heated in the TEM (Philips CM20 FEG–TEM) at 520°C for various times. During the *in-situ* annealing study, a specific particle or a surface defect was used to keep track of the region of interest. A series of electron diffraction patterns and dark field images were taken as a function of *in-situ* annealing time. Figure 3.14 shows the plan-view, dark field images of a 3 nm ALD-HfO_2 film at various stages in the crystallization process. In order to investigate the mechanistic details and kinetics of HfO_2 crystallization, the crystalline volume fraction was calculated using gray-scale image analysis of a series of dark field images taken from the same area. The imaged

area was ~ 1.2 μm^2, sufficiently large to include many hundreds of individual HfO_2 grains. Figure 3.15 shows the change of crystalline volume fraction with annealing time, which follows the typical S-shaped crystallization kinetics curve. According to the Avrami isothermal transformation model,[27] the volume fraction of crystalline phase formed (F) can be expressed as:

$$F = 1 - \exp\left(-(kt)^n\right) \qquad \text{Equation (3.4)}$$

where k and n are time-independent constants, and t is the annealing time. For 2-dimensional transformation in which the growth rate of the transformed regions does not vary with time, the parameter n is between 2 and 3, depending on the nucleation rate of the transformed material. In the limit of a fixed number of sites that host essentially instantaneous nucleation events at the start of the transformation, n will be exactly 2. When the nucleation rate decreases with time, n will be close to 2, and n approaches 3 if the system sustains a constant nucleation rate. By fitting the experimental data to the Equation (3.4), the solid line in Figure 3.15 follows the Avrami's isothermal transformation equation given by Equation (3.4) with n equal to 2.2. This suggests that

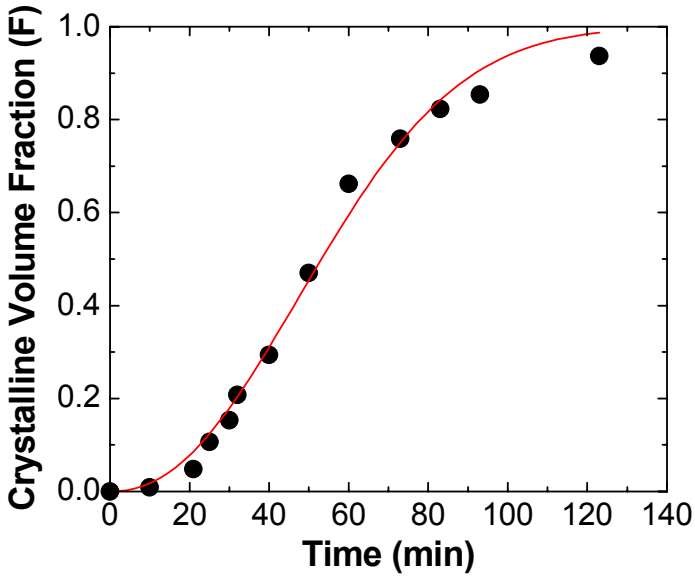

Figure 3.15: Volume fraction of crystallized HfO_2 as a function of annealing time; the solid line is a fit to the data using Equation (3.4).

the transformation occurs from a fixed population of initial nuclei or that the nucleation rate decreases quickly with annealing time. Therefore, it appears that 1) isothermal crystallization of ALD-HfO_2 follows a 2-dimensional nucleation and growth mechanism as a result of the very small film thickness relative to the final crystalline grain size formed and that 2) the crystallization process involves either instantaneous or very rapid initial nucleation.

3.5 Effect of HfO_2 crystallization on electrical properties

Hafnium oxide is an attractive choice for high permittivity gate dielectric applications due to the possibility of its compatibility with conventional poly-Si gate electrodes. This may avoid need for a barrier layer between the metal oxide dielectric and poly-Si gate.[28] However, unlike ALD-grown ZrO_2 films, which are typically observed to be polycrystalline, there is a phase change during annealing of as-deposited HfO_2 in which an amorphous phase transforms to a polycrystalline film of monoclinic phase as discussed in the previous section. The effects of crystallization on the electrical characteristics of the HfO_2 film have not yet been studied in detail. In this section, we discuss the effects of microstructural changes on the electrical characteristics of the resulting gate stacks as probed by capacitance-voltage (C-V) and current-voltage (I-V) measurements using both *ex-situ* and *in-situ* annealing experiments.[29,30]

3.5.1 Ex-situ annealing study

In this experiment, 2.8 ~ 3 nm-thick HfO_2 films were deposited at 300°C either on a thick (~ 2.5 nm) or thin (~ 1.5 nm) thermally grown SiO_2/Si and annealed at temperatures in the range 450°C to 900°C in N_2 ambient for 30 minutes using a conventional atmospheric pressure furnace, without any capping layer on the metal oxide films. After fabricating simple MOS capacitors, high frequency CV measurements were

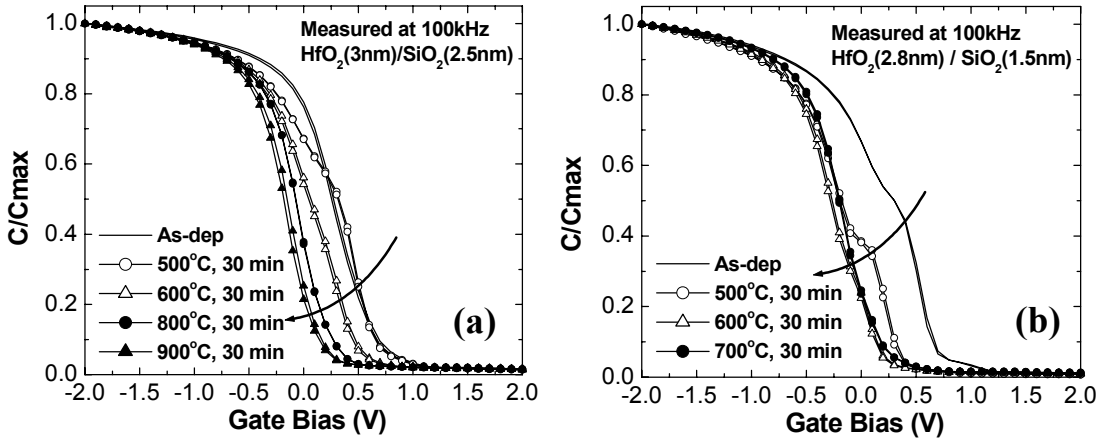

Figure 3.16: Normalized CV characteristics as a function of N_2 annealing temperature measured at 100 kHz before forming gas anneal: (a) 3 nm HfO_2/2.5 nm SiO_2 and (b) 2.8 nm HfO_2/1.5 nm SiO_2.

performed before and after forming gas annealing (400ºC, 30 min). In general, MOSFET devices are annealed in forming gas to passivate interface states with hydrogen in the final stage of fabrication, and this annealing step can screen out changes of intrinsic interface and bulk properties that would otherwise be detected in CV measurements.[31] Therefore, in this experiment, the characteristics of HfO_2 films having various microstructural evolution stages were also analyzed by CV measurement prior to forming gas annealing. As is evident from Figure 3.16, there was no significant change in the CV hysteresis, as the crystallization of the initially-amorphous HfO_2 films took place. This suggests that introduction of grain boundaries or crystalline/amorphous boundaries does not significantly increase the density of carrier-trapping defect sites that contribute to CV hysteresis at these measurement frequencies (10 kHz – 800 kHz). The initial CV curve from the as-deposited sample was slightly stretched compared to the one measured after forming gas annealing, indicating a high density of interface states prior to hydrogen exposure, which were significantly passivated by the forming gas anneal. A noticeable shoulder on the CV curve was observed at a gate bias of ~ 0.25 V in the case of HfO_2/2.5 nm SiO_2 structure annealed at 500ºC before forming gas anneal (Figure 3.16 (a)). When a very thin (~1.5 nm) interfacial SiO_2 layer was used (Figure 3.16 (b)), this shoulder was

detected in CV measurements of the as-deposited sample and became more distinct after 500ºC annealing. It is believed that this feature, which can be attributed to a very large density of interface states, may originate from metal impurity (Hf) diffusion and incorporation into the interface between SiO_2 layer and Si substrate during deposition and subsequent annealing. Guha *et al.*[32] observed a significant diffusion of metal impurities into the channel region in an Al_2O_3/Si system using secondary ion mass spectroscopy (SIMS) measurements. As a result, there may be some structural rearrangement occurring, likely at the HfO_2/SiO_2 interface, and that the states thus created have a greater effect on the carrier statistics in the Si when a thin oxide layer is present than they do when a thick oxide layer is present. After the forming gas anneal in 4% H_2/N_2 ambient, most of the interface states were passivated as expected by hydrogen passivation effects (not shown here). At higher annealing temperatures, new interfacial oxidation or phase separation of the interfacial layer resulted in the decrease of the CV feature, indicating a decrease of interface state density. Above 700°C, the flatband voltages were shifted toward lower values and deviated further from the ideal value (~ 0.66 V). This is believed to be caused mainly by either the decrease of total maximum capacitance (see Figure 3.17) while maintaining a similar fixed oxide charge density or by the change in defect density which may act as a fixed charge.

Figures 3.17 (a) and (b) show the change in the maximum capacitance measured in the accumulation bias regime (- 2 V) as a function of N_2 annealing temperatures for capacitor samples having different thicknesses of interfacial oxide. All results shown in the figure are for capacitors measured after forming gas anneal. The maximum capacitance decreased as the annealing temperature was increased. This decrease was particularly dramatic for 30 min anneals at temperatures of 700°C and greater in the case of the samples having a thin interfacial oxide. For the samples having a thin interfacial oxide (Figure 3.17 (b)), the abrupt capacitance decrease was observed at a much lower temperature (600°C). The significant change in capacitance after high temperature annealing was caused by the growth of the amorphous interfacial oxide layer, as confirmed by cross-sectional TEM studies. In plan-view bright field TEM images of samples annealed at 700°C and above, distinct white boundaries were observed and

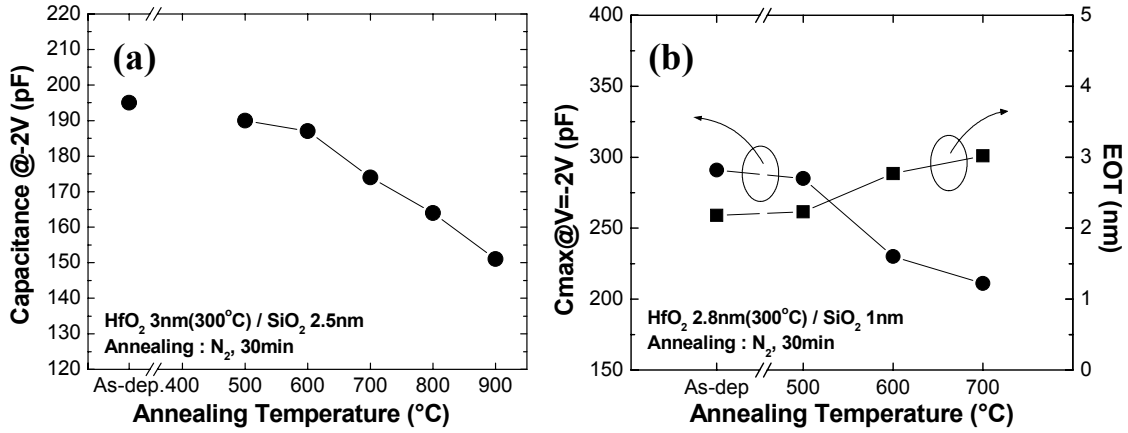

Figure 3.17: Change in maximum capacitance and EOT at –2V with N_2 annealing temperature: (a) 3 nm HfO_2/2.5 nm SiO_2 and (b) 2.8 nm HfO_2/1.5 nm SiO_2.

attributed to high angle grain boundaries as discussed in the previous section. This boundary contrast may result from thermal grooving of grain boundaries on the film surface during anneals, which tends to reduce the surface energy along the grain boundaries that separate the nanometer-scale HfO_2 grains. As displayed in Figure 3.18, the cross-sectional TEM pictures show significant interfacial oxide growth (25 % increase after 900°C annealing) during the N_2 annealing. Although we used high purity N_2, the interface oxide growth may result from the presence of 1 – 10 ppm of oxygen as an impurity in the nitrogen gas.[33]

Room temperature leakage current behavior was measured at various stages of

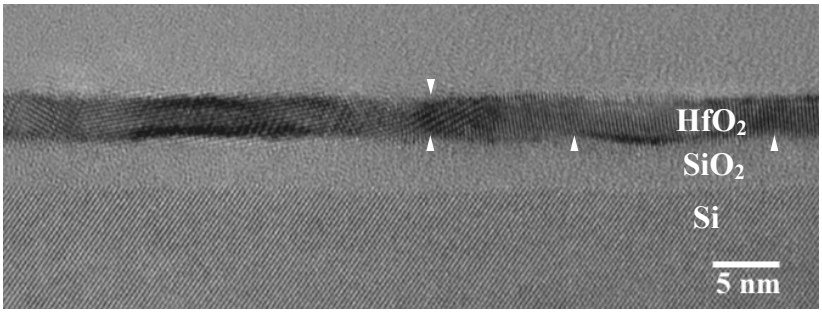

Figure 3.18: Cross-sectional HR-TEM micrograph of HfO_2/SiO_2 after 900°C N_2 annealing for 30 min.

microstructural evolution after annealing. Representative results are shown in Figure 3.19 for the HfO_2 films deposited onto Si substrates, passivated by different thicknesses of thermal silicon oxides. As discussed in Section 3.3.2, a distinct leakage current mechanism change is observed at ~ 3.2 V for the identical gate structures (~ 3 nm HfO_2/ 2.5 nm SiO_2). At higher electric fields, the Fowler-Nordheim tunneling mechanism matches well with measured results. At low electric fields, a trap-assisted tunneling conduction mechanism is consistent with the data observed from these films in variable-temperature IV measurements. Previous detailed TEM and electron diffraction results indicate that significant crystallization is observed after 30 min anneal at 500°C, and HfO_2 crystallization is essentially complete in 30 Å films after a 600°C anneal of the same duration. However, as is evident from Figure 3.19 (a), the leakage current in the trap-assisted tunneling regime did not change significantly as a result of these crystallization anneals. A monotonic decrease in leakage current density with increasing annealing temperature is observed after 30 min anneals at temperatures of 700°C and higher. This trend, as well as the change in the transition voltage from trap-assisted tunneling to Fowler-Nordheim tunneling conduction, are consistent with a decreasing electric field across the gate stack with increasing anneal thermal budget. Trends in the IV data are consistent with the observed increase in interfacial oxide thickness after annealing the ALD-HfO_2 dielectric layer at these annealing temperatures. In the case of HfO_2 samples annealed at various temperatures on thin SiO_2 (1.5 nm) (Figure 3.19 (b)), interfacial oxide growth and a simultaneous decrease in the leakage current was detected at much lower annealing temperatures.

There are concerns that leakage current densities may be higher across polycrystalline dielectrics than in amorphous films of the same composition since defective grain boundary regions may enhance electronic conduction. For this and other reasons, a number of methods are now being studied to suppress the crystallization of high-κ gate dielectric materials.[34] Our polycrystalline, as-deposited ALD-ZrO_2 gate dielectrics, however, exhibited leakage current densities comparable to or even lower than those reported for amorphous high-κ dielectric candidates with comparable EOT's, as discussed in Section 3.3.2. The present experimental results examining crystallization

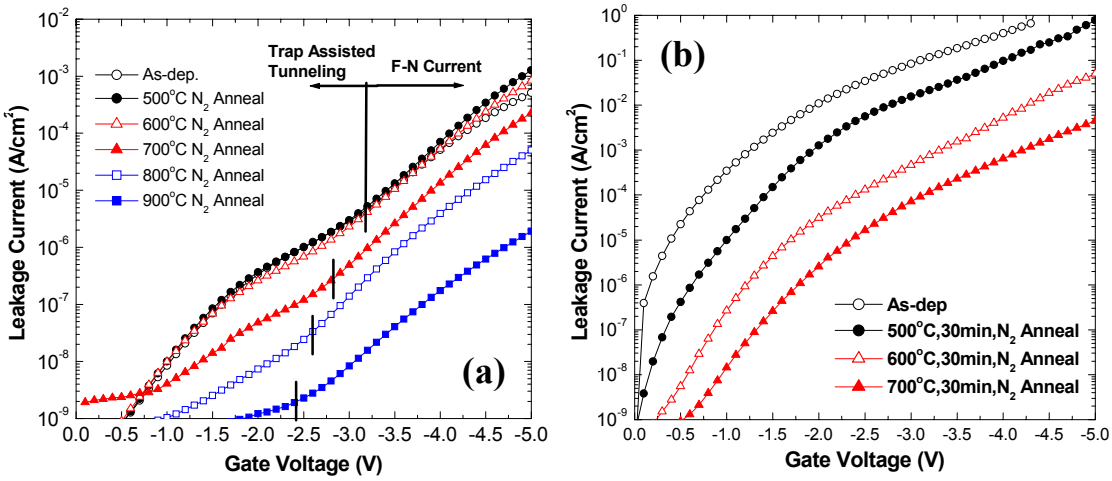

Figure 3.19: Leakage current characteristics as a function of N_2 annealing temperature: (a) 3 nm HfO_2/2.5 nm SiO_2 and (b) 2.8 nm HfO_2/1.5 nm SiO_2.

of HfO_2 films and its effects on the gate leakage current suggests that the additional trap states introduced by formation of grain boundaries make little contribution to conduction. One possible interpretation of these data is that the "bulk" defects within the dielectric layer (e.g. point defects and Cl impurities) or the "interface" defects located at metal oxide/SiO_2 produce a far greater trap density than that contributed by grain boundaries. However, the capacitor areas used in these experiments are very large compared to gate areas in real transistors and that there may be grain-to-grain variations in leakage current, which could have important effects on uniform device properties if the grain size is large relative to the gate length.

3.5.2 Low pressure in-situ annealing study

In a previous Section 3.5.1, the minimal effect of crystallization on the electrical properties of thin ALD-HfO_2 films was discussed. In particular, the formation of crystalline defects, such as grain boundaries, was found to have almost no effect on the measured leakage current densities across Pt/HfO_2/SiO_2/Si MOS capacitors. However, during *ex-situ* annealing, the ppm quantity of O_2 present in the high purity N_2 annealing

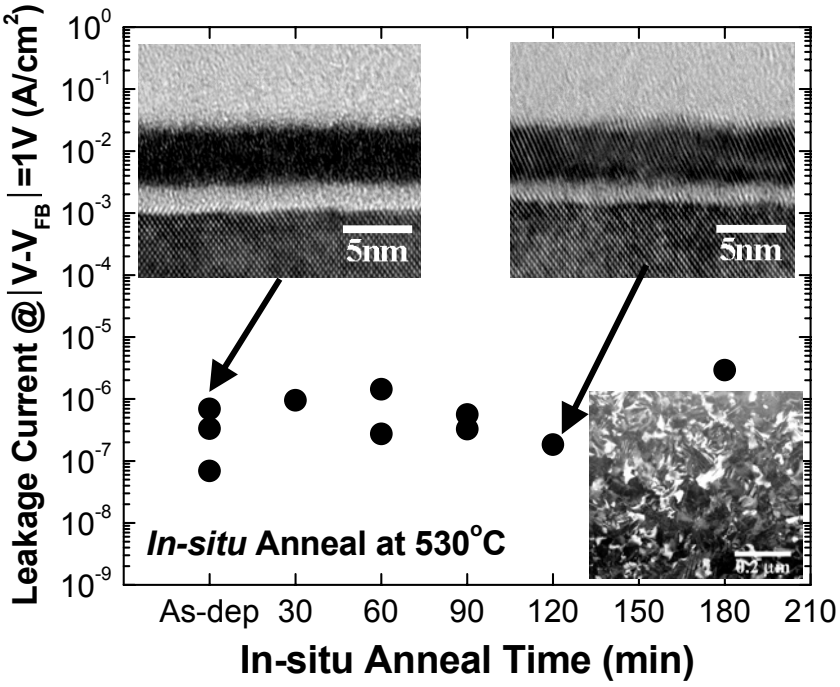

Figure 3.20: Gate leakage current density of HfO_2/SiO_2 stacks measured at $|V-V_{FB}| = 1$ (V) condition as a function of *in-situ* annealing times. The top insets show cross-sectional high resolution TEM images of amorphous and fully crystallized HfO_2. The bottom inset is a dark field plan-view TEM image of a fully crystallized HfO_2 sample.

ambient induced growth of the interfacial oxide layer and prevented direct comparison of capacitor electrical properties for all the annealing conditions of interest. This limitation was especially significant in the case of gate stacks having a thin initial interfacial SiO_2 layer.

In order to compare the leakage current values and conduction mechanisms of as-deposited amorphous HfO_2 films and fully crystallized HfO_2 films without a thickness change in the interfacial oxide during crystallization, *in-situ* annealing in the ALD vacuum chamber (1.3 Torr, N_2 ambient) was used. Approximately 4 nm-thick ALD-HfO_2 films were deposited on a Si wafer passivated by a ~ 1.5 nm chemical oxide layer. Samples were annealed for various times at 530°C immediately following deposition without breaking vacuum. Cross-sectional TEM images indicated a negligible change in

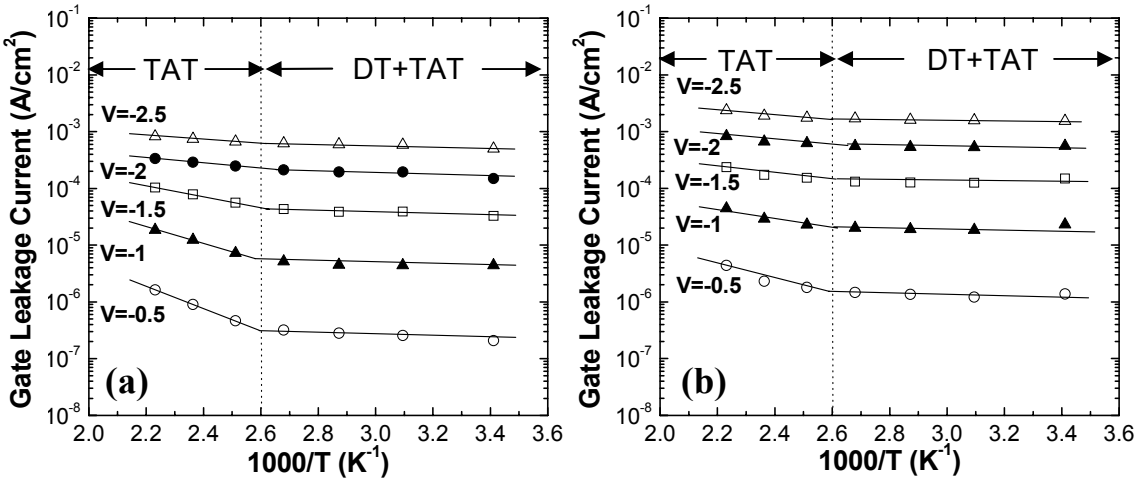

Figure 3.21: The gate leakage current density vs. applied voltage for HfO_2/SiO_2 stacks as a function of 1/T: (a) as-deposited amorphous HfO_2 and (b) fully crystallized HfO_2 *in-situ* annealed at 530°C for 120min.

HfO_2 film and interfacial oxide thickness for the annealing time range investigated (up to 180 minutes, see the inset of Figure 3.20) and CV measurement showed minimal change of the accumulation capacitance with complete crystallization. The degree of crystallization of the ALD-HfO_2 films was investigated through dark field imaging (lower inset of Figure 3.20), and it revealed that all the samples were fully crystallized after 30 min *in-situ* annealing. The leakage current data measured at $|V_{applied}-V_{FB}| = 1$ V are shown in Figure 3.20 and exhibit no significant increase (within experimental error) in the leakage current as a function of annealing time.

Figure 3.21 plots the leakage current density versus the inverse of measurement temperature for the as-deposited (amorphous) and the annealed (fully-crystalline) ALD-HfO_2 films. The films exhibited the same leakage current behavior as a function of temperature and applied voltage regardless of their microstructures; this is consistent with the previous results using an *ex-situ* annealing experiment, which demonstrated the minimal effects of crystallization on the electrical properties of ultra thin ALD-HfO_2 dielectrics (Section 3.5.1).

3.6 Summary

The microstructures of ALD-ZrO_2 and HfO_2 films were characterized and compared as a function of film thickness. As-deposited ALD-ZrO_2 showed a polycrystalline structure with a tetragonal phase in the thinnest films but exhibited a mixture of monoclinic and tetragonal phases at thicknesses greater than ~ 14 nm. In contrast, ALD-HfO_2 is primarily amorphous in the as-deposited state. Crystallization into a mixture of monoclinic and tetragonal phases occurred during post-deposition thermal annealing (> 500°C). Through extensive electrical characterization, the dielectric constants of ZrO_2 and HfO_2 were determined to be ~ 30 and ~ 20, respectively. The leakage current density was low compared to that of conventional SiO_2 gate dielectrics.

The crystallization kinetics of ALD-HfO_2 films was studied using an *in-situ* TEM technique. The transformation kinetics data were consistent with a 2-dimensional nucleation and growth mechanism in which nucleation either occurred instantaneously or with a rapid decrease of the nucleation rate. The crystallized microstructure after high temperature annealing (> 700°C) was composed of clusters of very small grains separated by either low angle grain boundaries or twin boundaries.

The effects of HfO_2 crystallization on the electrical properties after *ex-situ* and *in-situ* annealing were also investigated. *Ex-situ* furnace annealing showed the independence of the trap assisted tunneling leakage current on the crystallinity of the initially-amorphous HfO_2 films. An abrupt decrease in the maximum capacitance and a corresponding decrease in the leakage current densities were observed after complete crystallization. This was caused primarily by growth of the interfacial oxide layer due to the presence of a small partial pressure of O_2 in the N_2 tube furnace annealing atmosphere. The *in-situ*, post-deposition crystallization performed in the ALD chamber circumvented thickening of the initial SiO_2 passivation of the Si substrate. This study revealed that the effect of crystallization on the gate leakage current density was negligible and that the conduction mechanisms for amorphous and fully crystalline HfO_2 were identical.

References

[1] J. Robertson, J. Vac. Sci. Technol. B **18**, 1785 (2000).

[2] S. K. Dey, C.-G. Wang, D. Tang, M. J. Kim, R. W. Carpenter, C. Werkhoven, and E. Shero, J. Appl. Phys. **93**, 4144 (2003).

[3] G. V. Samsonov, *The Oxide Handbook* (Plenum, New York, 1981).

[4] C. M. Scanlan, M. Gajdardziska-Josifovska, and C. R. Aita, Appl. Phys. Lett. **64**, 3548 (1994).

[5] R. C. Garvie and M. V. Swain, J. Mater. Sci. **20**, 1193 (1985).

[6] C. R. Aita, M. D. Wiggins, R. Whig, C. M. Scanlan, M. Gajdardziska-Josifovska, J. Appl. Phys. **79**, 1176 (1996).

[7] M.-Y. Ho, H. Gong, G. D. Wilk, B. W. Busch, M. L. Green, P. M. Voyles, D. A. Muller, M. Bude, W. H. Lin, A. See, M. E. Loomans, S. K. Lahiri, and P. I. Räisänen, J. Appl. Phys. **93**, 1477 (2003).

[8] H. Kim, P. C. McIntyre, and K. C. Saraswat (unpublished work).

[9] C. M. Perkins, B. B. Triplett, P. C. McIntyre, K. C. Saraswat, S. Haukka, and M. Tuominen, Appl. Phys. Lett. **78**, 2357 (2001).

[10] B. H. Lee, L. Kang, W.-J. Qi, R. Nieh, Y. Jeon, K. Onishi, and J. C. Lee, Tech. Dig. – Int. Electron Devices Meet. **1999**, 133 (1999).

[11] L. Kang, B. H. Lee, W.-J. Qi, Y. Jeon, R. Nieh, S. Gopalan, K. Onishi, and J. C. Lee, IEEE Electron Device Lett. **21**, 181 (2000).

[12] W.-J. Qi, R. Nieh, B. H. Lee, L. Kang, Y. Jeon, K. Onishi, T. Ngai, S. Banerjee, and J. C. Lee, Tech. Dig. – Int. Electron Devices Meet. **1999**, 145 (1999).

[13] M. Houssa, V. V. Afanas'ev, A. Stesmans, and M. M. Heyns, Appl. Phys. Lett. **77**, 1885 (2000).

[14] D. Gerstenberg, in *Handbook of Thin Film Technology*, edited by L. I. Maissel and R. Glang (McGraw-Hill, New York, 1970).

[15] G. Timp, K. K. Bourdelle, J. E. Bower, F. H. Baumann, T. Boone, R. Cirelli, K. Evans-Lutterodt, J. Garno, A. Ghetti, H. Gossmann, M. Green, D. Jacobson, Y. Kim, R. Kleiman, F. Klemens, A. Kornlit, C. Lochstampfor, W. Mansfield, S. Moccio, D. A.

Muller, I. E. Ocola, M. I. O'Malley, J. Rosamilia, J. Sapjeta, P. Silverman, T. Sorsch, D. M. Tennant, W. Timp, B. E. Weir, Tech. Dig. – Int. Electron Devices Meet. **1998**, 615 (1998).

[16] Z. Xu, M. Houssa, S. D. Gendt, and M. Heyns, Appl. Phys. Lett. **80**, 1975 (2002).

[17] S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981).

[18] W. J. Zhu, T. P. Ma, and T. Tamagawa, IEEE Elec. Dev. Lett., **23**, 97 (2002).

[19] M. Houssa, M. Tuominen, M. Naili, V. Afanas'ev, A. Stesmans, S. Hukka, M. M. Heyns, J. Appl. Phys. **87**, 8615 (2000).

[20] H. Kim, P. C. McIntyre, and K. C. Saraswat, Appl. Phys. Lett. **82**, 106 (2003).

[21] J. Aarik, A. Aidla, H. Mandar, V. Sammelselg, and T. Uustare, J. Crys. Growth. **220**, 105 (2000).

[22] J. Aarik, A. Aidla, H. Mandar, T. Uustare, K. Kukli, and M. Schuisky, Appl. Surf. Sci., **173**, 15 (2001).

[23] D. A. Buchanan, IBM J. Res. Develop. **43**, 245 (1999)

[24] T. Hori, *Gate Dielectrics and MOS ULSIs: Principles, Technologies, and Applications* (Springer, Berlin, 1997).

[25] G. D. Wilk, R. W. Wallace, and J. M. Anthony, J. Appl. Phys. **87**, 484 (2000).

[26] M.-Y. Ho, H. Gong, G. D. Wilk, B. W. Busch, M. L. Green, W. H. Lin, A. See, S. K. Lahiri, M. E. Loomans, P. I. Räisänen, and T. Gustafsson, Appl. Phys. Lett. **81**, 4218 (2002).

[27] W.D. Kingery, H.K. Bowen, and D.R. Uhlmann, *Introduction to Ceramics*, 2nd Edition (Wiley, New York, 1976).

[28] L. Kang, Y. Jeon, K. Onishi, B. H. Lee, W-J Qi, R. Nieh, S.Gopalan, and J. C. Lee, Tech. Dig. VLSI Symp. **2000**, 44 (2000).

[29] H. Kim, P. McIntyre, and K. C. Saraswat, Appl. Phys. Lett. **82**, 106 (2003).

[30] H. Kim, A. Marshall, P. McIntyre, and K. C. Saraswat, Accepted to Appl. Phys. Lett. (2004).

[31] K. L. Brower, Appl. Phys. Lett. **53**, 508 (1988).

[32] S. Guha, E. P. Gusev, H. Okorn-Schmidt, L.-Å Ragnarsson, and P. Ronsheim, Appl. Phys. Lett. **81**, 2956 (2002).

[33] S. Ramanathan, C. M. Park, and P. C. McIntyre, Appl. Phys. Lett. **91**, 4521 (2002).

[34] G. D. Wilk, R. M. Wallace, and J. M. Anthony, J. Appl. Phys. **87**, 484 (2000).

Chapter 4

Microstructural and Electrical Properties of ALD-ZrO_2 and HfO_2 on Germanium Substrates

4.1 Introduction

As the continued scaling of Si complementary metal-oxide-semiconductor (CMOS) devices approaches its fundamental limits, various methods are being investigated to increase the drain current by improving the carrier mobility in the channel region. Improvements of carrier mobility have been obtained by replacing the conventional Si channel with strained Si.[1] However, a major breakthrough may be achieved if the conventional Si substrate is replaced by an alternative semiconductor material with higher intrinsic carrier mobility, such as Ge. Because of its higher low-field carrier mobility for improved saturation current and smaller bandgap for supply voltage scaling, there have been many attempts to use Ge as a channel material in high-speed field effect transistors.[2,3] Unfortunately, during device manufacturing, the lack of a sufficiently stable native oxide poses problems in obtaining a high quality surface passivation. Recently, however, Ge based metal-oxide-semiconductor (MOS) capacitors

and transistors incorporating high-κ dielectrics showing superior electrical properties have been demonstrated in our work[2,4] and that of others.[5]

In this chapter, the microstructural and electrical characteristics of ALD-grown ZrO_2 and HfO_2 dielectric layers on Ge (100) substrates are presented and compared with those films on Si substrates. In order to characterize the effects of surface passivation conditions and optimize the electrical properties of high-κ gate dielectric stacks, various surface treatments, such as HF cleaning, H_2O cleaning, and nitridation using NH_3 as well no surface preparation, were used in this experiment. Microstructural and electrical properties of ALD dielectric films on Ge were investigated using transmission electron microscopy (TEM), X-ray photoelectron spectroscopy (XPS), medium energy ion scattering (MEIS), and basic MOS electrical characterization.

4.2 Properties of Germanium

4.2.1 Germanium as a channel material

The first bipolar transistor fabricated was made using germanium by a research team at Bell Laboratories in 1947.[6] However, germanium was replaced with silicon in subsequent devices because of the lack of a stable insulator layer which could be used as a gate dielectric for MOS devices. If high-κ materials are adopted for the gate dielectric, then it may be advantageous to revisit Ge technology due to its beneficial properties.

As summarized in Table 4.1,[7,8] Ge has similar materials and electrical properties compared to those of Si. The property that distinguishes Ge from a device point of view is the high carrier mobilities at low electric fields (Figure 4.1[9]), a consequence of the low effective mass and the sub-band valley degeneracy of Ge.[10] This attribute can significantly improve MOS transistor speed by decreasing the gate delay, which is inversely proportional to the source injection velocity, v_{inj}:[11]

$$\frac{C_{LOAD}V_{DD}}{I_{DS}} = \frac{L_{gate} \times V_{DD}}{(V_{DD} - V_T) \times v_{inj}} \qquad \text{Equation (4.1)}$$

where C_{LOAD} is the load capacitance, V_{DD} is the supply voltage, I_{DS} is the drain current, L_{gate} is the gate length, and V_T is the threshold voltage. In particular, the significantly larger hole mobility in Ge can enhance the total speed of CMOS devices by increasing the PMOS saturation current compared to Si technology.

Property	**Silicon**	**Germanium**
Crystal structure	Diamond cubic	Diamond cubic
Melting point	1417 °C	937 °C
Density	2.328 g/cm^3	5.32 g/cm^3
Lattice constant	0.543 nm	0.566 nm
Atomic density	5×10^{22} cm^{-3}	4.418×10^{22} cm^{-3}
Young's modulus	$Y_{100}=1.3\times 10^{12}$ dyne/cm^2 $Y_{111}=1.9\times 10^{12}$ dyne/cm^2	-
Thermal conductivity k_s at 300K	0.358 cal/(sec cm °C)	0.143 cal/(sec cm °C)
Band gap at 300K	1.107 eV	0.67 eV
Electron mobility at 300K	1500 cm^2 volt^{-1} sec^{-1}	3900 cm^2 volt^{-1} sec^{-1}
Hole mobility at 300K	450 cm^2 volt^{-1} sec^{-1}	1900 cm^2 volt^{-1} sec^{-1}
Electron affinity χ	4.05 eV	4.0 eV
Intrinsic carrier concentration n_i at 300K	1.45×10^{10} cm^{-3}	2.4×10^{10} cm^{-3}
Relative permitivity ε_r	11.9	16

Table 4.1: Comparison of material and electrical properties of silicon and germanium.[7,8]

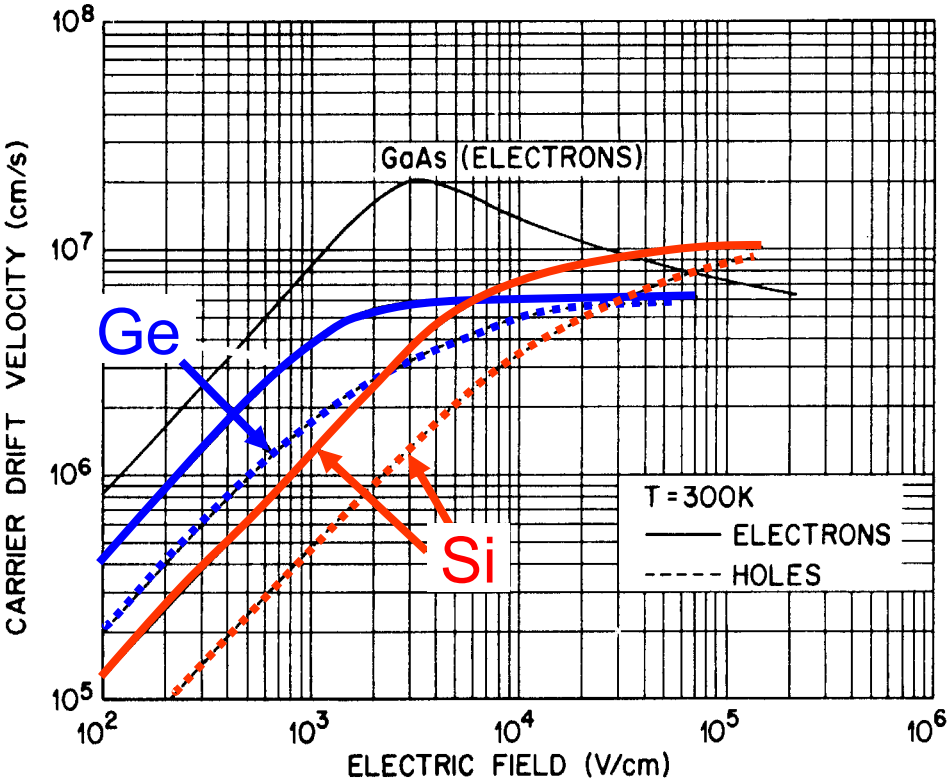

Figure 4.1: Carrier drift velocity of electrons and holes as a function of electric field in silicon and germanium at room temperature.[9]

4.2.2 Thermodynamic stability of Ge in contact with high-κ dielectrics

In order to incorporate Ge as a channel material with new high-κ gate dielectric materials, it is important to consider its thermodynamic stability in contact with various metal oxide dielectrics. However, due to the lack of available thermodynamic data for Ge-related compounds (especially, metal-germanide (MGe_x) and metal-germanate (MGe_xO_y) phases), it is relatively difficult to ascertain the stability of Ge compounds compared to Si-based material systems. Based on the thermodynamic analysis using a pseudo-ternary phase diagram as discussed in Chapter 1, the thermodynamic stability of ZrO_2 and HfO_2 with respect to solid state reaction with a Ge substrate was predicted.

Silicon and Ge are quite similar in terms of material and electrical characteristics, as discussed in the previous section. Thus, similar kinds of compounds can be assumed to exist in Zr-Ge-O and Hf-Ge-O ternary system as displayed in Figure 4.2. The Gibbs free energy change of the following reaction[12] at ALD deposition temperature (~ 600 K) indicates the absence of the Zr-GeO_2 tie line in Zr-Ge-O ternary phase diagram.

$$GeO_2 + Zr \rightarrow Ge + ZrO_2 \qquad \Delta G° = -520\ (kJ/mol) \qquad \text{Equation (4.2)}$$

Although the thermodynamic data for the relevant metal germanides are not available, the relatively large formation energy of ZrO_2 (~ 1135 (kJ/mol)) suggests that the tie line should emanate from ZrO_2 as depicted in Figure 4.2. Compared with a Zr-Si-O ternary system, a similar thermal stability is expected and theoretically it is quite possible to obtain an interfacial layer-free ZrO_2/Ge gate stack provided that ALD can occur on an initially oxide-free Ge surface and that no significant oxidation of the Ge substrate occurs under the ALD process conditions. For an Hf-Ge-O ternary system, a similar procedure was used and a prediction of similar thermal stability of HfO_2 films deposited on Ge at ALD deposition temperature used in these experiments resulted.

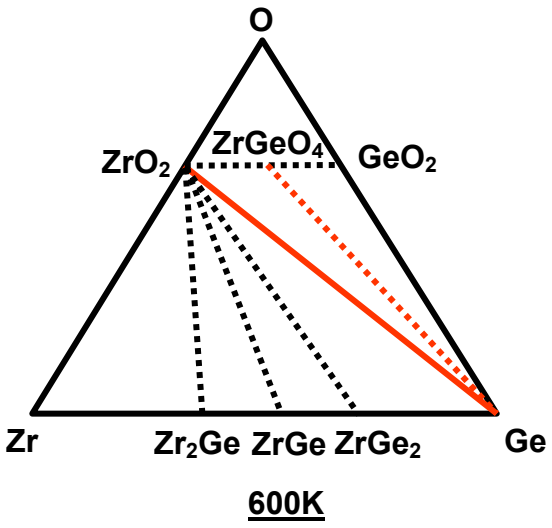

Figure 4.2: Calculated Zr-Ge-O phase diagram at T=600K.

4.2.3 Surface passivation using Ge-oxides

According to the previous thermodynamic stability analysis of high-κ dielectrics on Ge substrates, it is hypothetically possible to form a gate dielectric stack with little or no low-κ interfacial oxide. However, considering the possible increase of interface states and the resulting mobility degradation in transistor structures, a high quality interfacial layer between the Ge substrate surface and the metal oxide dielectric may be needed even though it has adverse effects with respect to gate capacitance. Different from well-known SiO_2 characteristics, the properties of GeO_2 and its sub-oxides are not well established. The thermal and process stability of Ge-oxides was investigated based on the published literature. To investigate the possibility of applying Ge-oxides as template layers before high-κ deposition, the bonding characteristics of various chemical oxides were studied using XPS techniques.

The main problem which inhibits the use of pure Ge as a channel region in CMOS

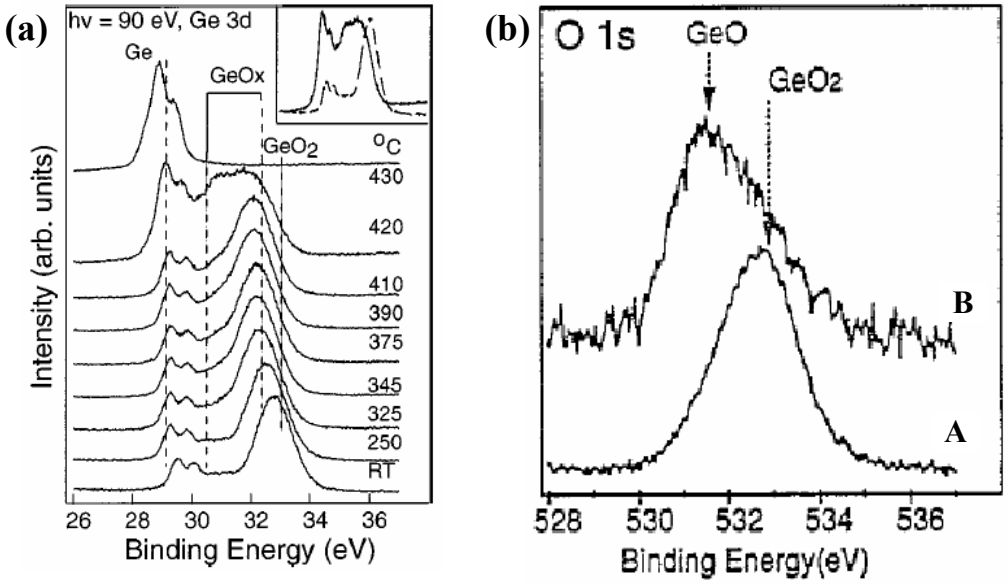

Figure 4.3: (a) Ge *3d* core level spectra as a function of temperature for chemical oxide on Ge (100) surface[13] and (b) O *1s* spectra of Ge (111) exposed to clean air for 5 h (A) and after rinsing in warm water (B).[14]

transistors is the instability of Ge-oxide during CMOS processing. It is well known that Ge-oxides (GeO and GeO_2) are strongly volatile at moderately high temperatures and also readily dissolved in liquid H_2O.[13,14] Figure 4.3 displays XPS spectrums showing the thermal stability of GeO_2 grown by concentrated H_2O_2 oxidation and the dissolution of GeO_2 in deionized H_2O rinsing reported by Prabhakaran *et al.*[13,14] Upon annealing the Ge oxides in ultra-high vacuum conditions, the intensity of the spectral component due to the dioxide species (GeO_2) decreases with a concomitant increase in intensity of the peak due to the sub-oxide species (GeO_x, $x < 2$)) as shown in Figure 4.3 (a). At ~ 430°C complete desorption takes place, leading to the formation of a clean Ge surface. In contrast, the decomposition and desorption of SiO_2 occurs at much higher temperatures (> 780°C). Furthermore, GeO_2 with the hexagonal structure has high water solubility, while the tetragonal form does not.[15] Figure 4.3 (b) exhibits the significant removal of the GeO_2 phase after H_2O rinsing at room temperature. However, Ge sub-oxide (GeO)

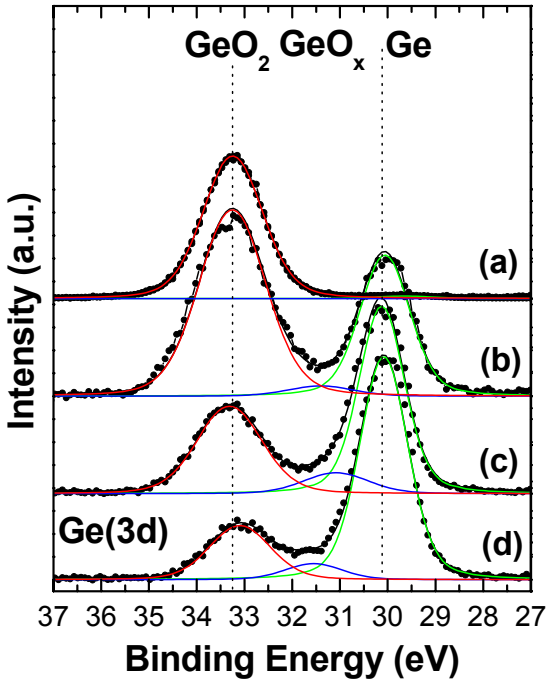

Figure 4.4: Ge *3d* spectra with different surface oxidation of Ge substrates: (a) thermally grown oxide, (b) native oxide, (c) H_2O_2 oxide, and (d) HNO_3 oxide.

cannot be completely removed through H_2O rinsing. Although H_2O rinsing can provide a convenient way to clean Ge substrates before metal oxide gate dielectric deposition, the poor quality of the residual sub-oxide may degrade the electrical properties of the fabricated devices.

Several surface oxides were grown on pure Ge using different kinds of chemical treatments. The resulting chemical bonding characteristics of the layers were analyzed using an XPS (Surface Science Instruments S-Probe, Al K_α x-ray source) in order to investigate the surface passivation behavior of Ge substrates before high-κ deposition. A ~ 8 nm-thick thermal oxide was grown at 500°C in O_2 ambient for 8 min. Other chemical oxides were prepared by dipping in either 30% H_2O_2/70% H_2O or 100% HNO_3 for 1 min directly after HF cleaning to remove native oxide. Figure 4.4 shows the Ge *3d* spectra of various oxides and fitted curves which were simulated by assuming the existence of three binding types, i.e., Ge, GeO_x, and GeO_2. Thermal oxide was mainly composed of only GeO_2 binding state, and other oxides were mixed with GeO_2 and Ge sub-oxide. Considering the relative intensity of features related to GeO_x to GeO_2, the relative amount of GeO_x is higher for the oxides prepared with H_2O_2 and HNO_3. Due to the non-stoichiometry of Ge sub-oxide, these chemical oxides may result in a high density of trapping sites and interface states in MOS capacitors fabricated on Ge substrates.

4.3 Locally epitaxial growth of ALD-ZrO_2 on Ge substrates

As a first experiment to incorporate high-κ gate dielectrics into Ge MOS devices, ZrO_2 high-κ dielectrics were deposited by ALD onto pure Ge (100) substrates cleaned with HF vapor. Although ALD high-κ dielectrics growth on HF-last Si substrate resulted in non-uniform and discontinuous film growth as discussed in Chapter 2, non-uniform surface adsorption was avoided on Ge, possibly due to the relative instability of the Ge-H bond compared to Si-H. Also, the thermal and chemical instability of Ge-oxide species made it possible to obtain a locally, epitaxial growth of ZrO_2 film both on Ge (100) and Ge (111). The microstructural and electrical characteristics of locally, epitaxially-grown ZrO_2 dielectric layers on Ge (100) and (111) substrates will be discussed in the subsequent sections.[16]

4.3.1 Microstructural analysis

As substrates, 4-inch diameter n-type <100> or <111> Ge wafers having 0.25 (Ω-cm) resistivity were used and the native oxide (GeO_x) was completely removed by exposing the wafers to HF vapor before ZrO_2 deposition. After cleaning, the Ge wafers were immediately transferred to the ALD system within an hour and deposition of ZrO_2 film was performed at 300°C.

Figure 4.5 shows the cross-sectional TEM image of ALD-ZrO_2 (~ 5.5 nm) grown on a HF vapor cleaned Ge (100) substrate. In contrast to the deposition characteristics typically observed on Si substrates, ALD deposition of ZrO_2 films on Ge (100) exhibited local epitaxial growth without a distinct interfacial layer as shown in Figure 4.5 (a). High-κ dielectric deposition by ALD occurs readily on hydroxylated surfaces such as chemical SiO_2 or a hydroxylated oxynitride passivation. Moreover, uncontrolled formation of a thin interfacial oxide layer is observed if the Si is not already passivated

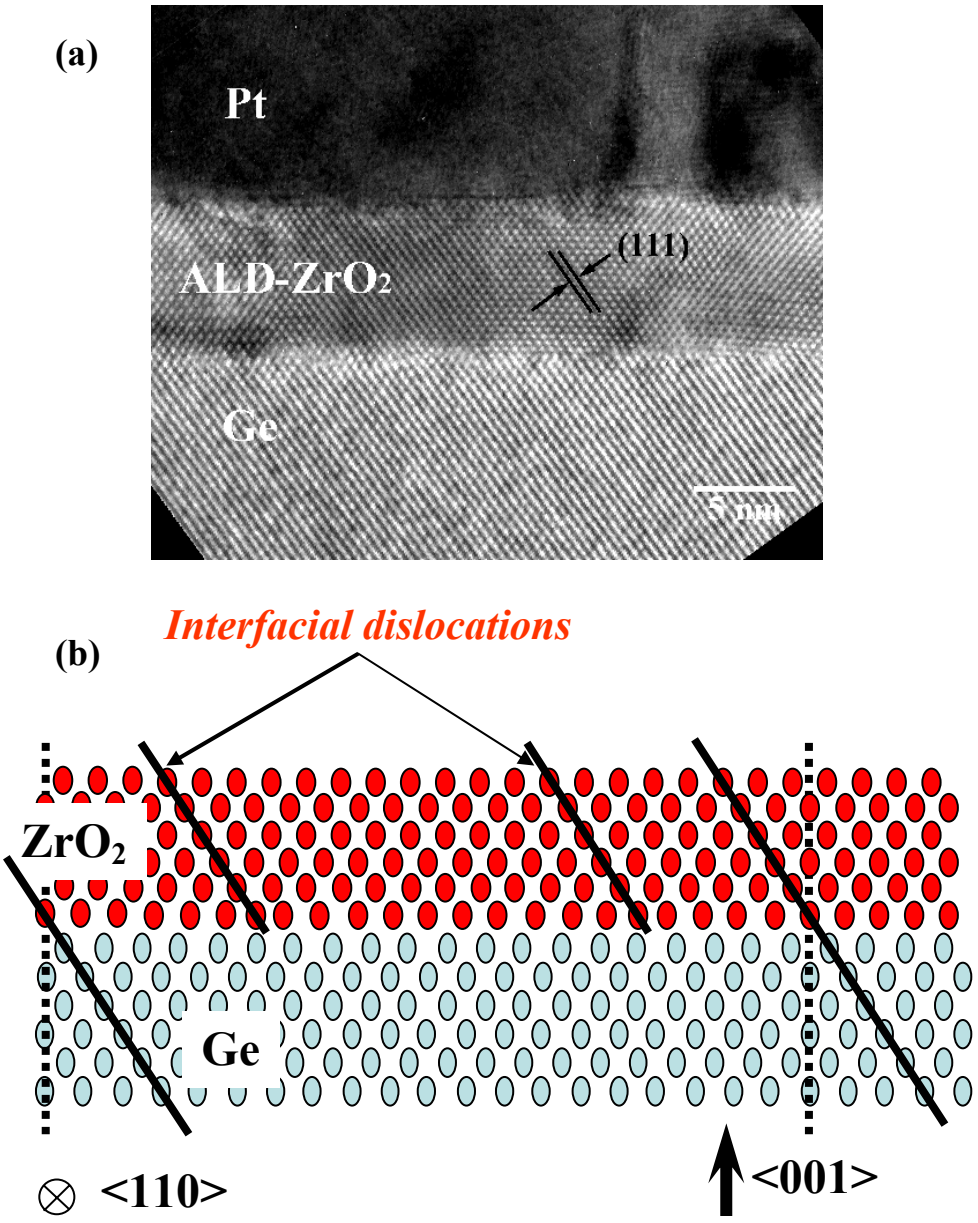

Figure 4.5: (a) Cross-sectional HR-TEM micrograph of Pt/5.5 nm ZrO_2/Ge (100) along the <110> zone-axis, and (b) schematic diagram showing the epitaxial relationship and the interfacial dislocations.

by such a layer prior to deposition.[17] High-κ materials such as ZrO_2 and HfO_2 are stable with respect to solid state reactions with Si; however, because metal oxide films are often deposited in an oxidizer-rich environment, some oxidation of the Si surface during high-k

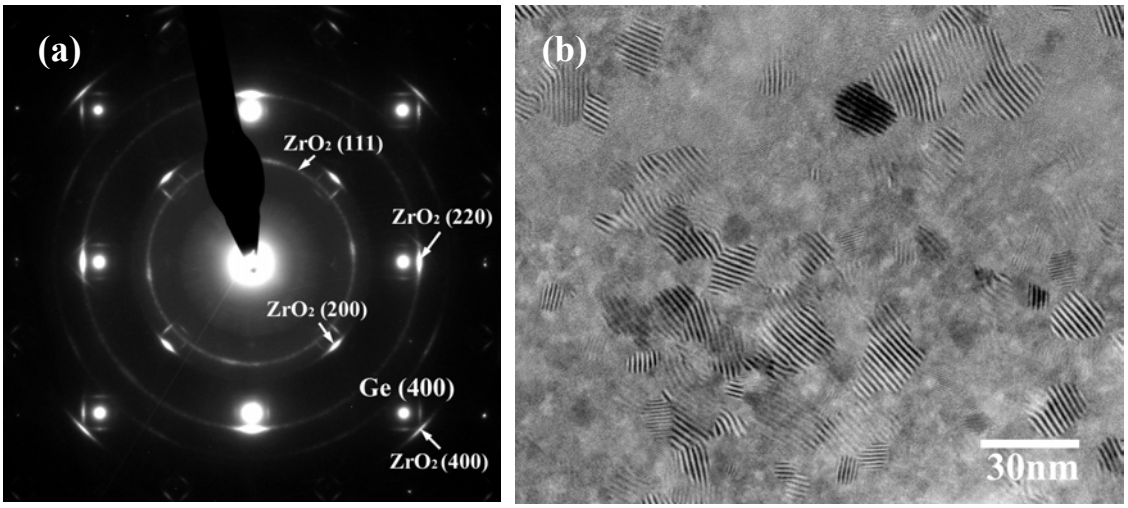

Figure 4.6: (a) Selected area electron diffraction pattern showing the corresponding epitaxial relationship and (b) bright-field plan-view image of 5.5 nm ZrO_2/Ge (100).

film deposition is almost unavoidable and the growth of this low-κ interface layer tends to limit the extent to which the equivalent oxide thickness (EOT) can be scaled. Considering the Gibbs free energy of formation for ZrO_2 (-1135 kJ/mol at 600K) and GeO_2 (-610 kJ/mol at 600K), it is plausible that ZrO_2 should be thermodynamically stable with respect to solid state reactions with the Ge substrate as discussed in Section 4.2.2, similar to the Si case. In contrast to the ZrO_2/Si case, ZrO_2 deposited by ALD on to Ge (100) consistently resulted in an interface layer-free structure. This was the case in spite of the fact that the Ge substrates were exposed to air after HF treatment to remove the native oxide, possibly resulting in some reformation of native oxide prior to ALD. However, as discussed in the previous Section 4.2.3, Ge-oxides (GeO and GeO_2) are very unstable at moderately high temperatures (> 400°C) in vacuum and also are readily dissolved in H_2O. During ALD deposition, it is possible that any interfacial oxide which formed in one part of the deposition process was dissociated and removed in a subsequent step. Due to the large lattice mismatch (~ 10%) between ZrO_2 (a=b=5.07 Å for tetragonal ZrO_2) and Ge (a=5.657 Å), a significant areal density of interfacial dislocations

can be seen in the cross-sectional image in Figure 4.5 (a). This relationship is schematically illustrated in Figure 4.5 (b).

The epitaxial relationship between film and substrate was further verified using plan-view imaging and electron diffraction analysis as shown in Figure 4.6. Indexing of electron diffraction patterns obtained during electron microscopy indicates that the ALD-grown ZrO_2 film may be in either the tetragonal or cubic phase. It is difficult to distinguish between a- or b-axis oriented tetragonal grains for the epitaxial orientation present in these films. However, careful investigation of electron diffraction patterns has verified that ZrO_2 films grown by ALD on SiO_2/Si substrates are in the tetragonal phase as discussed in Chapter 3. Therefore, it is quite likely that ALD-ZrO_2 films on the Ge (100) substrate are also tetragonal. Due to the large lattice mismatch, local epitaxial growth generated numerous distorted Moiré fringes, as shown in the plan-view image of Figure 4.6 (b). The mosaic spread of the epitaxial film orientation also manifests itself in a distortion of diffraction spots seen in the electron diffraction pattern (Figure 4.6 (a)). The (001) Ge // (001) ZrO_2 and [100] Ge // [100] ZrO_2 epitaxial relationship is observed, as expected for this system, and the existence of one extra ZrO_2 (111) atomic plane per

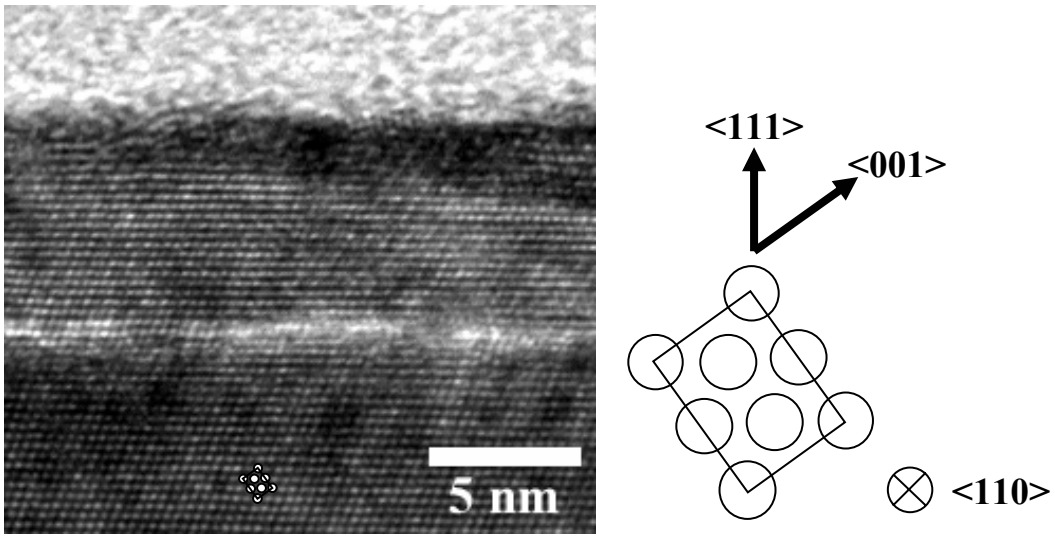

Figure 4.7: Cross-sectional HR-TEM micrograph of ~ 6.8 nm ZrO_2/Ge (111) along the <110> zone-axis.

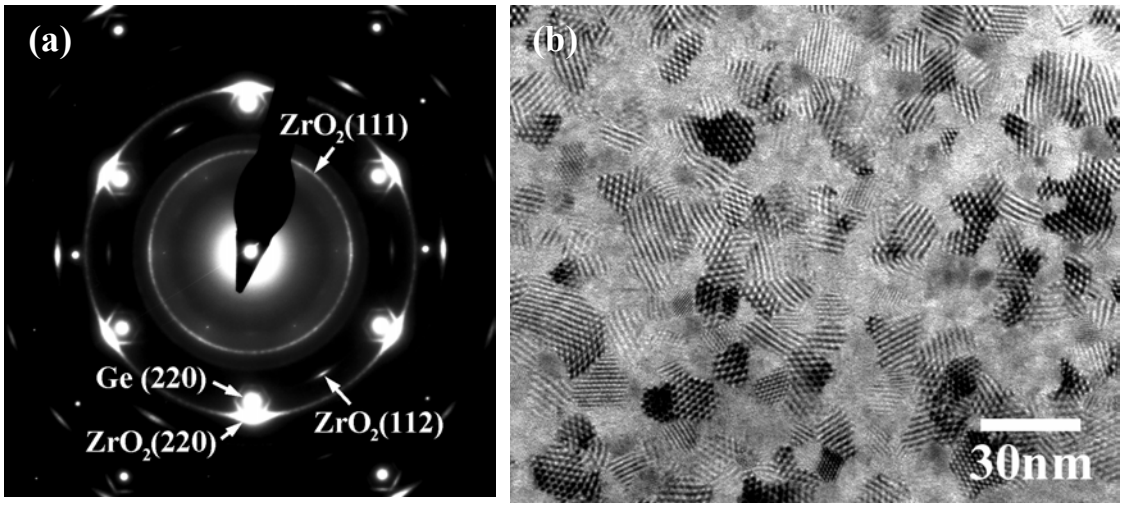

Figure 4.8: (a) Selected area electron diffraction pattern showing the corresponding epitaxial relationship and (b) bright-field plan-view image of 6.8 nm ZrO_2/Ge (111).

every 10 planes in the cross-sectional image indicates that the compressive misfit strain of the ZrO_2 film is almost fully relieved by misfit dislocations.

For further confirmation, ~ 6.8 nm-thick ALD-ZrO_2 was deposited on HF-last Ge (111) wafers and analyzed using cross-sectional TEM imaging as shown in Figure 4.7. Consistent with the results on the Ge (100) surface, a locally epitaxial growth habit can be seen on Ge (111) as well. Figure 4.8 displays the electron diffraction pattern and also the plan-view image showing lots of distorted Moiré fringes caused by the local epitaxial growth of ZrO_2 on Ge (111) substrate. According to indexing results obtained from the electron diffraction pattern, a (111) Ge // (111) ZrO_2 and [111] Ge // [111] ZrO_2 epitaxial relationship was obtained similar to the (100) Ge substrate case.

In order to verify the absence of an interfacial germanium oxide, XPS analysis using sputter depth profiling was performed. Results are shown in Figure 4.9 (a). A 90° take-off angle was used to maximize the depth examined and the Ge *3p* feature was monitored because the Ge *3d* signal overlaps with the Zr *4p* signal. As the sputtering etch time increases, a significant increase of the peak associated with the Ge substrate, and a simultaneous decrease of the Zr peak were observed (not shown here). However,

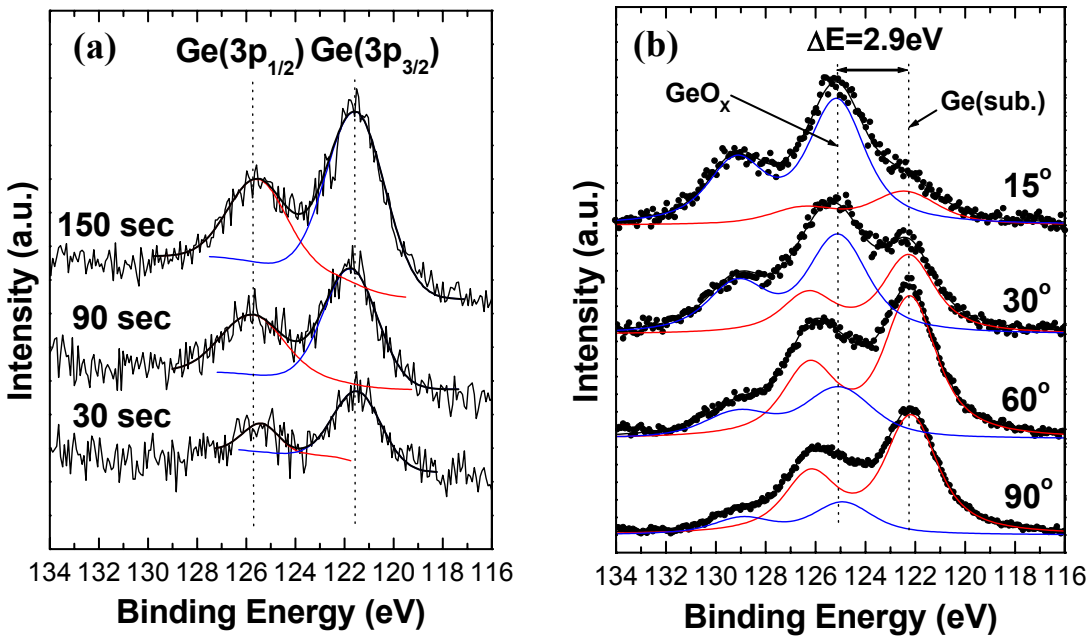

Figure 4.9: X-ray photoelectron spectrum and peak fitting results for the Ge *3p* feature: (a) 5.5 nm ZrO_2/Ge specimen for several sputter etch times and a 90° detection take-off angle, and (b) 1.5 nm ZrO_2/Ge specimen with different detection take-off angles.

no higher binding energy peaks, which might correspond to Ge-suboxide or $ZrGeO_x$ (zirconium germanate), were detected. As a comparison, a thinner ZrO_2 (~ 1.5 nm) layer on HF-last Ge was also analyzed using an angle-resolved XPS technique by varying the take-off angle of generated electrons from 15° to 90° to modulate the information depth. A significant amount of Ge-related interfacial layer was observed as shown in Figure 4.9 (b), which is believed to be caused by the significant oxygen diffusion across relatively thin ZrO_2 dielectric layer due to the absence of a capping layer, and subsequent oxidation after the sample was exposed to air at room temperature. Decreasing the take-off angle increases the relative contribution from the uppermost layers to the spectrum. This caused signals from the interfacial region corresponding to Ge-related sub-oxides or germanate phases to become predominant in the low-angle spectra.

4.3.2 Electrical properties

High frequency C-V measurements were performed on epitaxially grown ALD-ZrO_2 on Ge samples using circular capacitor patterns with Pt electrodes. As shown in Figure 4.10, a significant amount of frequency dispersion was observed even after series resistance correction using the two frequencies correction method,[18] and a very large hysteresis (> 200 mV) was observed across the entire frequency range. Perhaps due to the high density of dangling bonds[19] leading to high interface state density, the high frequency C-V curves from Ge (111) substrate exhibits a more distorted shape than the C-V curves from Ge (100) samples. After scanning the voltage from inversion to the accumulation condition, the C-V curve shifted along the positive axis during the reverse scan as a consequence of electron trapping. This was consistent with substrate electron injection from the n-type Ge. This significant electron trapping ($3\times10^{12} \sim 3.5\times10^{12}$ (/cm^2) for Ge (100) specimens) and frequency dispersion are believed to originate either from the large areal density of interfacial dislocations (~ 7×10^{12} (/cm^2) for a Ge (100)

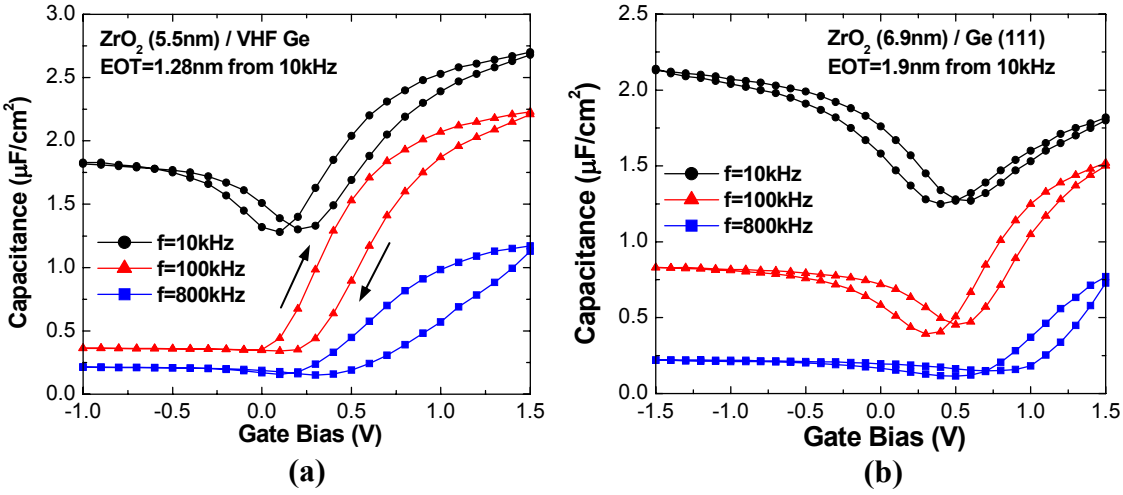

Figure 4.10: CV characteristics of (a) Pt/5.5 nm ZrO_2/n-type Ge (100) after forming gas anneal and (b) Pt/6.9 nm ZrO_2/n-type Ge (111) before forming gas anneal.

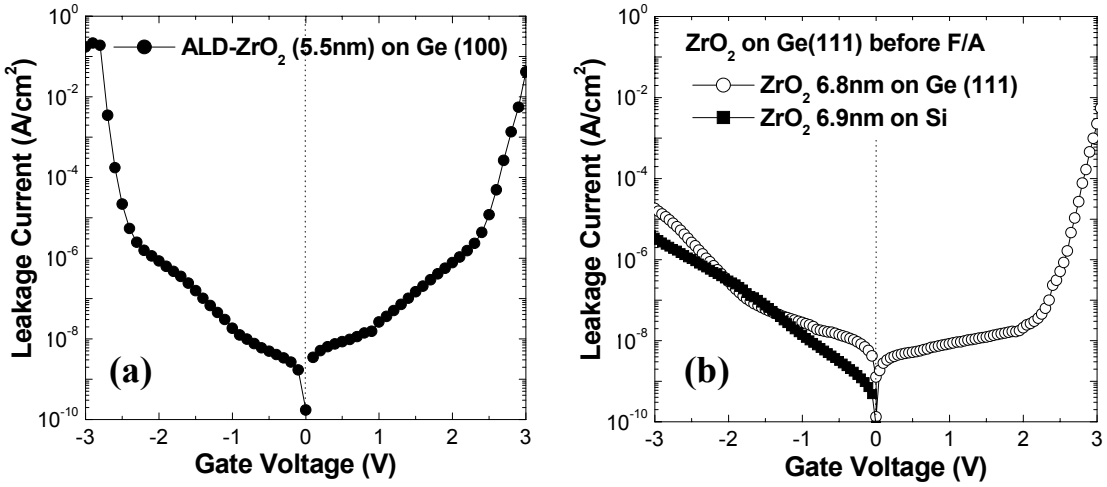

Figure 4.11: Leakage current characteristics of (a) a Pt/5.5 nm ZrO_2/n-type Ge (100) stack and (b) a Pt/6.8 nm ZrO_2/n-type Ge (111) stack for both bias polarities. Applied voltage is defined as positive when the top Pt electrode is positively biased.

specimen) due to the relatively large lattice mismatch or from the significant interface state density due to the weak Ge-O bonds compared to Si-O bonds. With decreasing measurement frequency, the inversion capacitance was observed to increase significantly. This may be attributed to either an increase in minority carrier generation due to the diffusion of impurities from the gate dielectric into the substrate, or to the interaction of interface slow states resulting from the large number of interfacial dislocations. Although the exact evaluation of the equivalent oxide thickness is impossible because of the significant frequency dispersion, an EOT of ~ 1.3 nm and ~ 1.9 nm for ZrO_2 on Ge (100) and Ge (111) samples, respectively, can be extracted from the 10 kHz C-V data, without any quantum-mechanical corrections.

Figure 4.11 shows the room temperature leakage current behavior of the ZrO_2 on Ge (100) and Ge (111) samples measured for both bias polarities. Although a large number of interface defects and low angle grain boundaries exist in these films, the measured leakage current density for significantly lower EOT is slightly higher than that achieved using ZrO_2 gate stacks on Si substrate with similar physical thickness. These excellent leakage current characteristics suggest that other crystalline high-κ metal oxides

with closer lattice match to Ge may be good candidates for epitaxial high-κ/Ge MOS devices. Moreover, optimization of the interface structure through process changes that may reduce the interfacial dislocation density is expected to improve the electrical properties of these high-κ/Ge gate stacks.

4.4 ALD-ZrO_2 and HfO_2 growth on Ge with different surface cleaning

As discussed in the previous section, the ALD growth of ZrO_2 on Ge surface without any passivation layer resulted in poor CV properties exhibiting large frequency dispersion, significant hysteresis, and abnormal inversion region capacitance behavior. In this section, several surface passivation methods were employed and characterized to improve the electrical properties of Ge-MOS capacitors with high-κ gate dielectrics.

4.4.1 ALD-ZrO_2 on Ge with different surface cleaning

Three different surface passivations (HF cleaning, deionized (DI) H_2O rinsing, and chemical oxide) were used on n-type Ge wafers and the resulting electrical properties were compared using ALD-ZrO_2 as a gate dielectric layer. Figure 4.12 shows the corresponding C-V characteristics with different surface conditions after a forming gas anneal (400°C, 30min). Regardless of the surface treatments, all the samples exhibited similar C-V behavior, i.e., high frequency dispersion, large hysteresis, and abnormal inversion capacitance. Although the exact mechanisms causing these anomalous C-V characteristics are not understood, the root source is believed to be either the significant number of interfacial defects originating from the poor interfacial bonding configuration or the diffusion of metal impurities from the gate dielectric into the substrate. As a passivation and a diffusion barrier layer for Ge-based MOS devices, Ge-oxide is not a

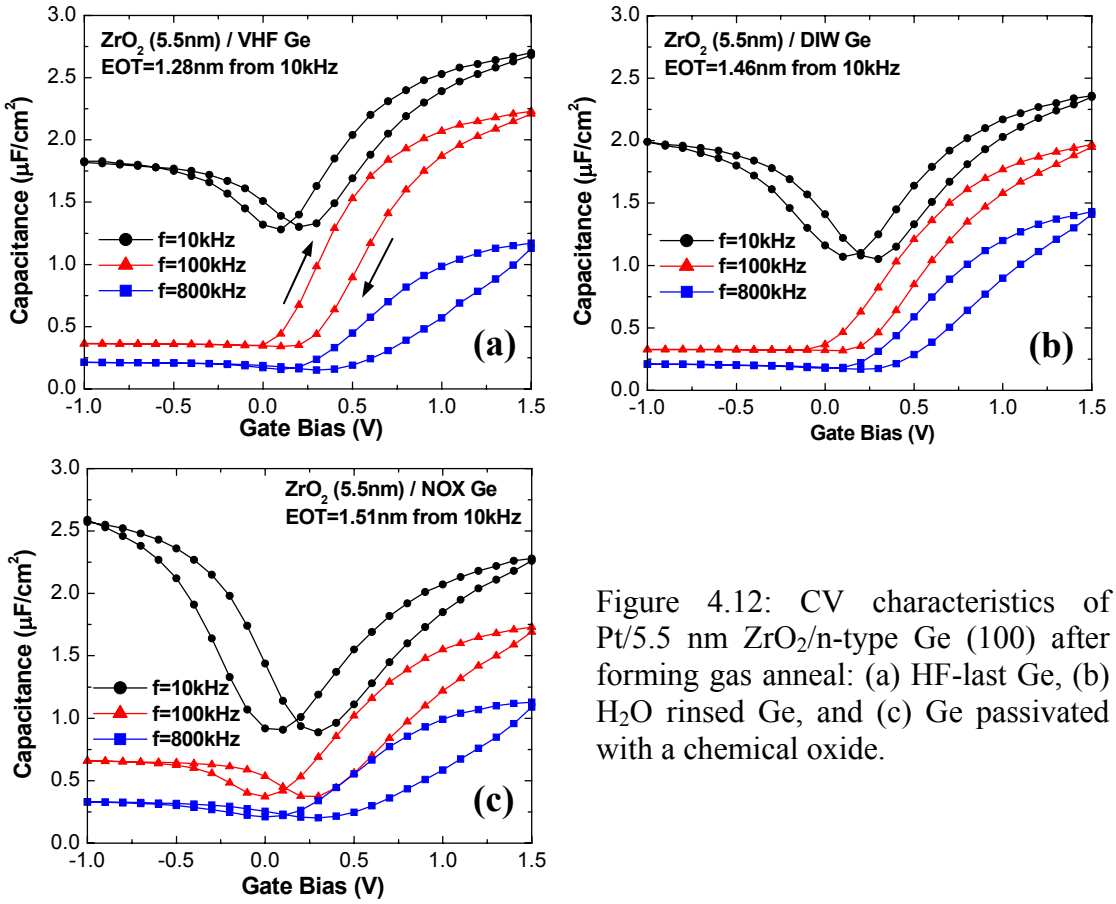

Figure 4.12: CV characteristics of Pt/5.5 nm ZrO_2/n-type Ge (100) after forming gas anneal: (a) HF-last Ge, (b) H_2O rinsed Ge, and (c) Ge passivated with a chemical oxide.

suitable choice. The EOT of HF-cleaned Ge, H_2O-cleaned Ge, and chemical oxide passivated Ge measured from 10 kHz data were 1.28, 1.46, 1.51 nm, respectively. The increase of EOT with the different cleaning methods was consistent with the amount of residual oxide layer on top of each Ge sample.

As described in the previous section, ALD-ZrO_2 deposition on HF-last Ge surface resulted in local epitaxial growth without any noticeable interfacial layer. Because H_2O rinsing can also remove GeO_2 effectively,[14] the possibility of epitaxial growth of ZrO_2 on H_2O treated sample was investigated using cross-sectional TEM. Figure 4.13 shows a thickness series of ALD-ZrO_2 films deposited on H_2O-cleaned Ge samples. Although it is difficult to resolve the thin interfacial oxide through TEM analysis due to the small contrast difference between ZrO_2 and Ge-related oxides, it is believed that sub-

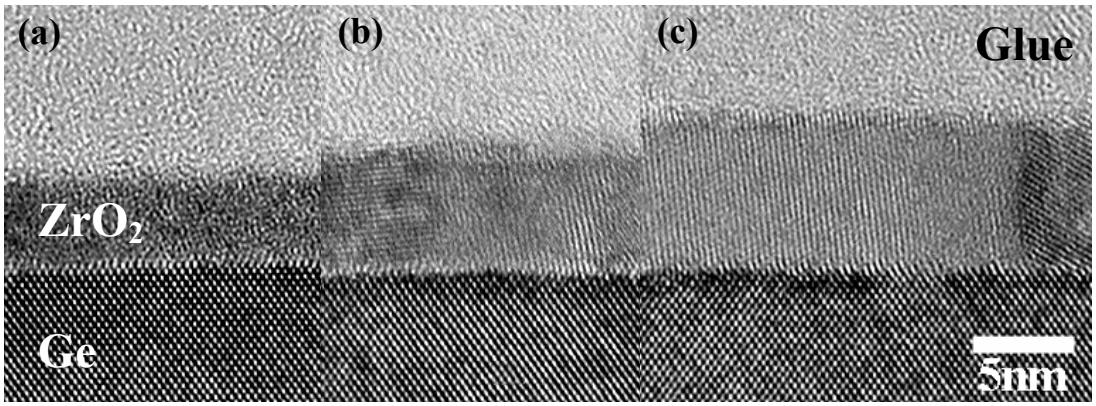

Figure 4.13: Cross-sectional high resolution TEM images of ALD-ZrO_2 films on H_2O-cleaned Ge substrates with different thicknesses: (a) 3.9 nm, (b) 5.7 nm, and (c) 7.5 nm.

nanometer-thick interfacial oxide exists considering the EOT difference between DI-rinsed and HF-cleaned samples. Also, a HfO_2 film, which has a higher atomic mass, grown on H_2O-cleaned Ge confirmed the existence of the thin interfacial oxide (0.3 ~ 0.4 nm). No apparent epitaxial relationship was observed throughout the different thicknesses of ALD-ZrO_2 films grown on H_2O-cleaned Ge, in contrast to the ZrO_2 on HF-last Ge case. Because the H_2O rinsing cannot remove the GeO_x phase efficiently as discussed in Section 4.2.3, it is plausible that a thin GeO_x layer, which possibly remained after H_2O cleaning or formed during the air-exposure, may inhibit the epitaxial growth of the ZrO_2 film.

The leakage current densities of three samples having different surface preparations were measured at both polarities, and compared with those of Si MOS capacitors having a similar physical ZrO_2 thickness (~ 5.5 nm) and a slightly higher EOT value as displayed in Figure 4.14. For the samples with a negligible amount of interfacial oxide layer (HF-cleaned and H_2O-cleaned Ge), the magnitude of leakage current density scaled with the CV-measured EOT values. However, ALD-ZrO_2 on Ge with a significant amount of interfacial Ge-oxide showed a slightly higher leakage current considering the high EOT and total physical thickness. This indicates the relatively poor electrical quality of Ge-oxides (or a possible metal germanate phase) and suggests the need for a

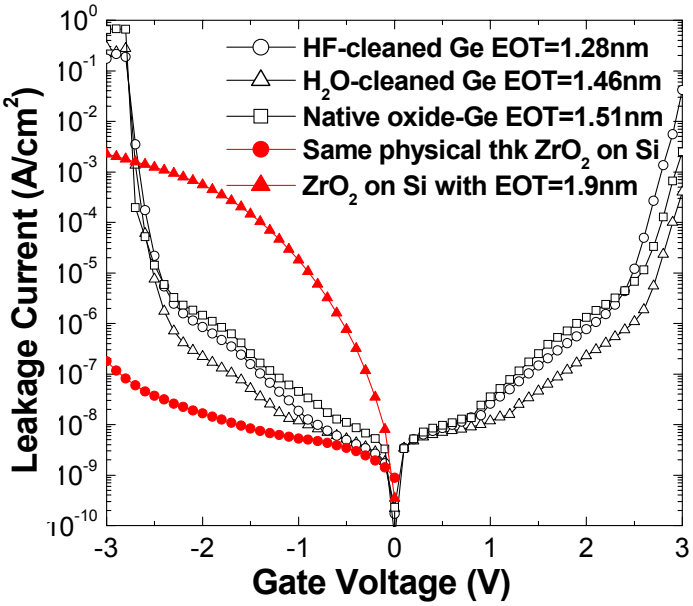

Figure 4.14: Leakage current characteristics of Ge MOS capacitors after forming gas anneal (400°C, 30min) with different surface treatments.

high quality diffusion barrier having a low density of interfacial defects on the Ge substrate. Compared with the leakage current behavior of Si samples having the identical physical thickness of ZrO_2, all the Ge samples exhibited a slightly higher leakage current, again indicating the need for a high quality interfacial layer on Ge substrate. However, compared with Si samples with a larger EOT, Ge capacitors showed promising leakage current behavior at much lower EOT.

4.4.2 ALD-HfO_2 on nitrided Ge surfaces

The absence or poor quality of the interfacial passivation layer on Ge prior to high-κ deposition consistently resulted in poor electrical properties as characterized using C-V measurements. It is well known that the incorporation of nitrogen into gate dielectrics, such as SiO_2[20] or high-κ dielectrics[21] can improve the dielectric integrity and

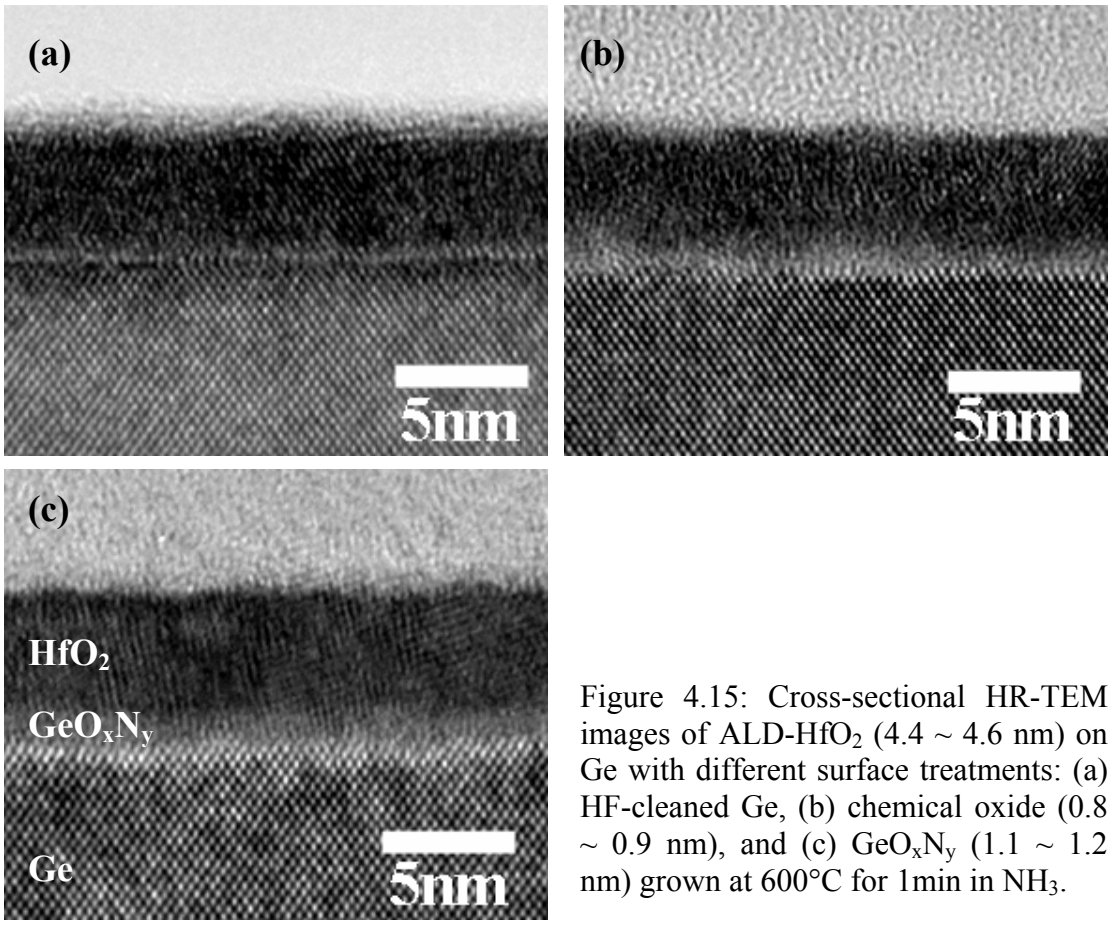

Figure 4.15: Cross-sectional HR-TEM images of ALD-HfO_2 (4.4 ~ 4.6 nm) on Ge with different surface treatments: (a) HF-cleaned Ge, (b) chemical oxide (0.8 ~ 0.9 nm), and (c) GeO_xN_y (1.1 ~ 1.2 nm) grown at 600°C for 1min in NH_3.

also inhibit impurity diffusion either from the gate dielectric or from the top gate electrode. In this experiment, Ge-oxynitride was incorporated into the Ge MOS structure through direct nitridation of the Ge substrate for use as a thermally stable interfacial layer and diffusion barrier. After removing any native oxide on Ge substrate using cyclic rinsing between 50:1 HF solution and DI water,[22] the samples were nitrided for 1 min at various temperatures (500°C ~ 700°C) in NH_3 ambient using an AG4108 RTP system followed by 3 ~ 4 nm-thick HfO_2 deposition. Similar fabrication and characterization procedures as with the Si-based capacitors were followed.

Figure 4.15 shows a cross-sectional TEM image of $HfO_2/GeO_xN_y/Ge$ structure compared with HfO_2 upon otherwise passivated Ge. The HF-cleaned Ge sample had negligible interfacial oxide due to the instability of Ge-oxides as confirmed in the

previous experiments using ZrO_2 dielectric. Also, a relatively thinner (0.8 ~ 0.9 nm) interfacial oxide remained in the case of HfO_2 deposition on Ge substrate having a chemical oxide compared to HfO_2 on Si substrate (1.4 ~ 1.5 nm interfacial layer). The interface between the HfO_2 film and the interfacial layer (chemical oxide) exhibited worse roughness than the HfO_2/SiO_2 case. (See Figure 4.15 (b)) It is believed that the uneven dissociation of Ge-oxide or the partial reaction between HfO_2 and Ge-oxide could occur during the moderately high ALD deposition temperature and lead to increased roughness. For the nitrided sample, a uniform 1.1 ~ 1.2 nm-thick interfacial GeO_xN_y layer was observed, as shown in Figure 4.15 (c). This layer may block chemical interactions between the deposited HfO_2 film and the substrate more effectively than a Ge-oxide layer.

In order to optimize the nitridation conditions used for Ge, C-V characteristics on Pt/ALD-HfO_2/GeO_xN_y/Ge MOS structures with two different nitridation temperatures (600°C and 700°C) were obtained before and after forming gas annealing (Figure 4.16). Before the forming gas anneal (300°C, 30min), the Ge MOS sample nitrided at 600°C exhibited very low CV hysteresis and frequency dispersion compared to the one nitrided at 700°C. Although a significant density of slow states exist near the conduction band edge within the Ge bandgap, an outstanding improvement of C-V characteristics was achieved through the NH_3 nitridation of the Ge surface before the high-κ deposition. Higher nitridation temperatures resulted in a significant increase in the capacitance signature of these slow states and an increase of the capacitance in the inversion bias regime, which is qualitatively different from the previously observed continuous increase and saturation of inversion capacitance in Ge MOS structures without surface nitridation. According to the XPS study which will be discussed in the following section of this chapter, the N incorporation into the GeO_xN_y linearly increased with nitridation temperature. The nitrided layer is believed to act as a diffusion barrier or a passivation layer improving the defect densities originated from the poor quality of Ge-related oxides. However, the oxynitride layer may generate other trap levels, to which the observed slow states can be attributed. The high density of N-related defects has also been observed in Si-nitride directly deposited on Si substrates.[23,24]

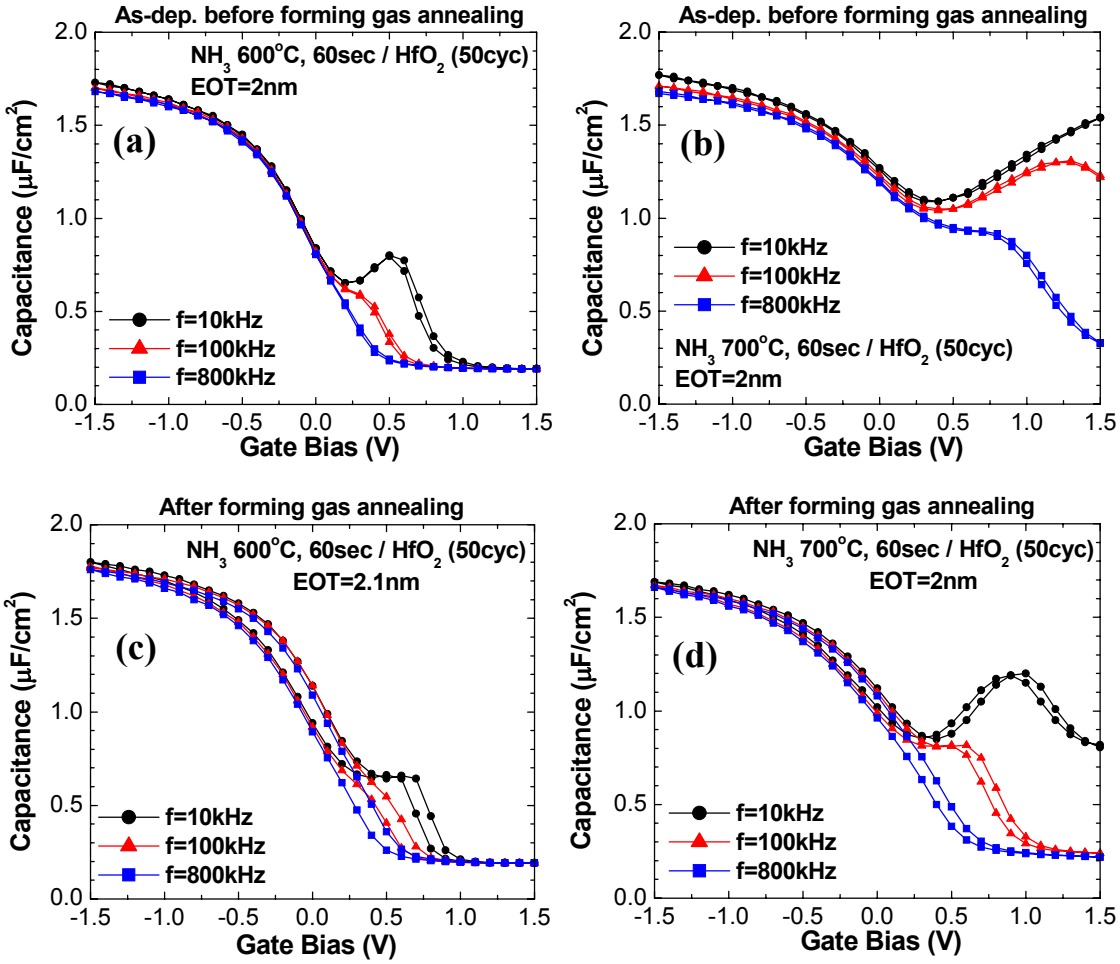

Figure 4.16: C-V characteristics of Pt/HfO_2/Ge capacitors before/after forming gas anneal with different nitridation temperatures: (a) 600°C and (b) 700°C nitridation before forming gas anneal, (c) 600°C and (b) 700°C nitridation after forming gas anneal.

As already well-established in Si-based MOS technology, a forming gas annealing improves the C-V characteristics with respect to the interface states (including the slow states), however, a large hysteresis was observed from high-κ/nitrided Ge stacks after this anneal, independent of the nitridation temperature. Recent preliminary studies using high-κ films grown by ALD and the UV-O_3 oxidation technique showed that lower forming gas annealing temperatures and N_2 annealing did not deteriorate the C-V characteristics of Ge MOS capacitors.[25] Therefore, it is expected that hydrogen exposure

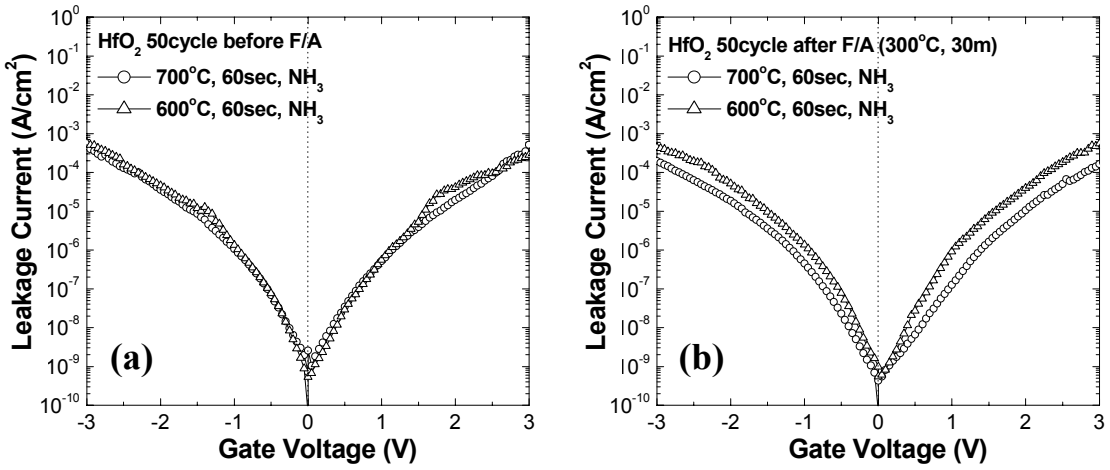

Figure 4.17: Leakage current characteristics of Pt/HfO_2/Ge capacitors with different nitridation temperatures: (a) before and (b) after a forming gas annealing (300ºC, 30min)

of the nitride layer is playing a significant role in Ge MOS structures, although the detailed mechanism is not understood.

Figure 4.17 shows the leakage current densities of ALD-grown HfO_2 films on Ge substrates nitrided at different temperatures before and after a forming gas annealing. Although there were significant differences in C-V characteristics for the different nitridation temperatures, the leakage current densities were independent of nitridation temperature for both polarities and were similar to or even lower than those of ALD-HfO_2 films deposited on Si substrates having identical EOT.

4.4.3 XPS and MEIS study of GeO_xN_y with different nitridation temperatures

In order to investigate the role of the interfacial GeO_xN_y layer formed by nitridation of HF-cleaned Ge substrate in an NH_3 ambient, medium energy ion scattering (MEIS) analysis was used. The MEIS technique is a lower energy version of Rutherford

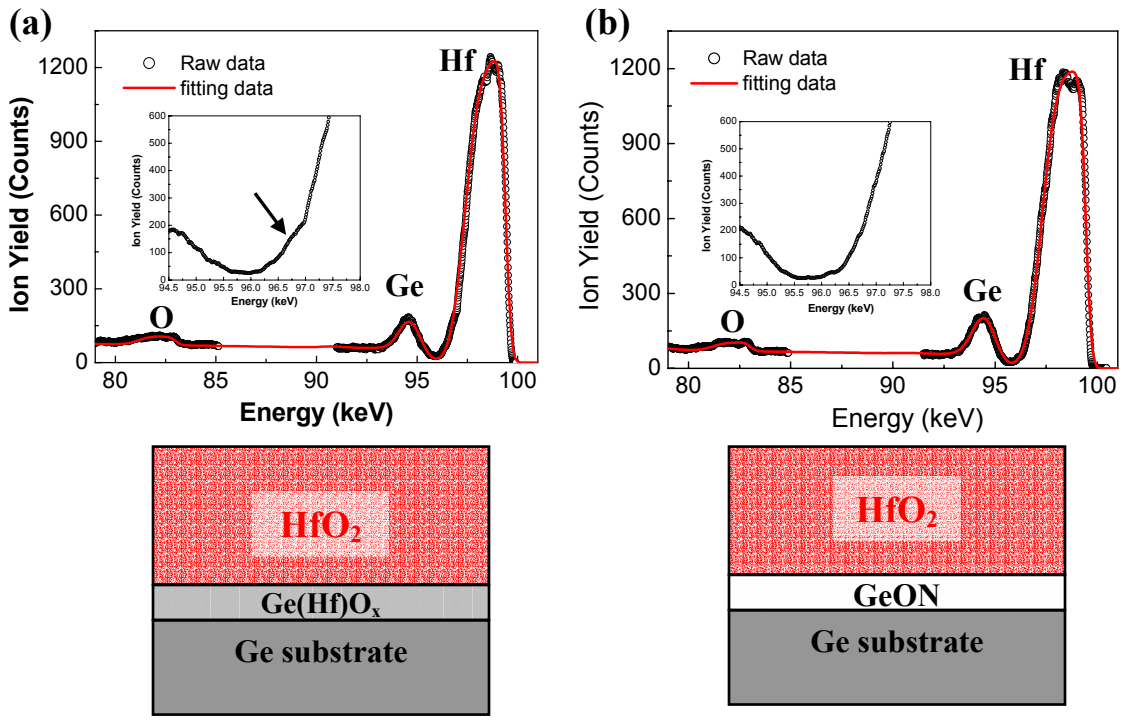

Figure 4.18: MEIS spectra with fitted curves and the corresponding model structure of (a) HfO_2 on Ge substrate with chemical oxide and (b) HfO_2 on Ge substrate nitrided at 600°C for 1 min in NH_3 ambient after cyclic HF-stripping.

backscattering in which the energy and angular distributions of scattered ions are used to obtain detailed information about atomic structure and composition in the top 5 – 20 nm of the sample.[26]

Two samples with ~ 4 nm-thick ALD-HfO_2 films were deposited onto two different Ge (100) substrates: one with chemical oxide passivation and the other nitrided at 600°C in NH_3 for 1 min after cyclic HF stripping. MEIS analysis was performed with a 100 keV proton beam in a detector alignment so as to reduce the contributions from the crystalline Ge substrate, allowing deconvolution of spectra into contributions from the HfO_2 layer, Ge-containing underlayer, and Ge substrate. The incident ions were directed along the $[11\bar{1}]$ direction in $(1\bar{1}0)$ plane and the scattered ions were along the [001] direction with a scattering angle of 125°. Quantitative depth profiles for different species were extracted with a resolution of less than 0.5 nm in the near-surface region.

Figure 4.18 shows the measured MEIS spectra and the fitting results for both samples. The overall shapes of both spectra were similar except for a difference in the lower energy edge of the Hf signal as shown in the insets of Figure 4.18. This corresponds to the interfacial layer under the HfO_2 film. For the HfO_2 sample on Ge with a chemical oxide, a distinct shoulder which is believed to be caused by intermixing between Hf and GeO_x was observed even though no post-thermal treatment was performed after the sample preparation. On the contrary, no significant amount of Hf atoms in the interfacial oxide (GeO_xN_y) was observed within the MEIS detection limit (< 5 at%). Although there is no clear mechanism to explain the improvement of electrical characteristics of HfO_2/nitrided Ge MOS capacitors, the blocking of Hf out-diffusion into the Ge substrate as observed in MEIS could be a significant contributor to the improvement in properties.

The amount of incorporated nitrogen and its binding status in the GeO_xN_y layer with different nitridation temperatures were studied using XPS analysis. Cyclic HF-

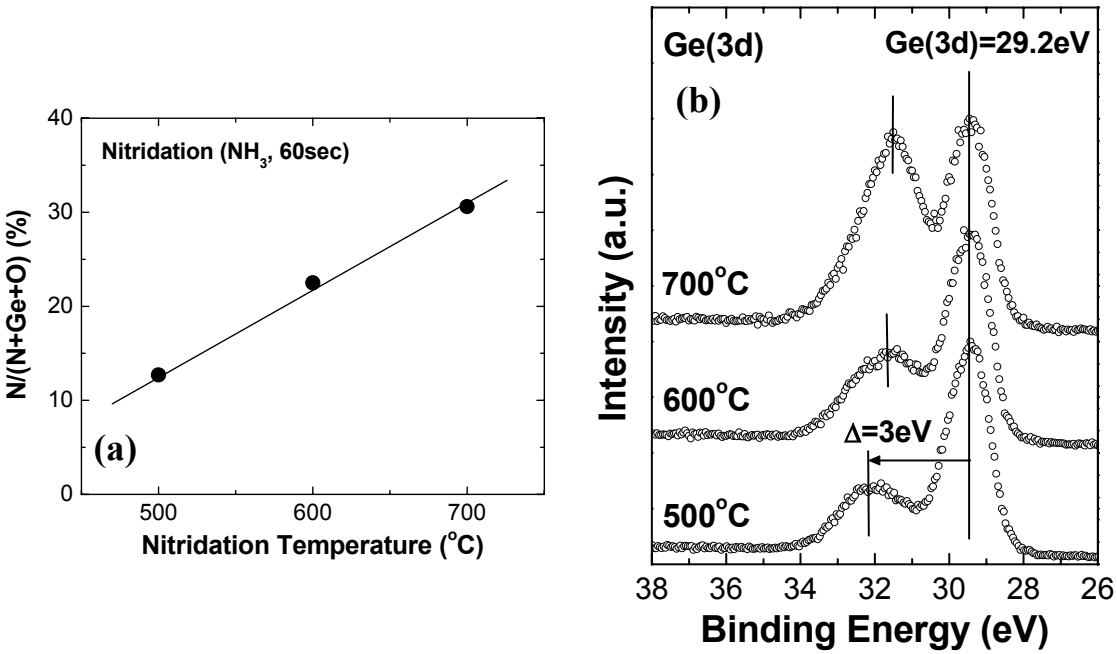

Figure 4.19: (a) Relative atomic concentration of N and (b) Ge *3d* XPS spectra as a function of nitridation temperatures.

water cleaned Ge samples were nitrided at various temperatures for 1 min, and analyzed without a capping layer using a Surface Science Instruments S-Probe (Al K_α x-ray source) and the undulator-radiation beamline (8A1) of a Pohang Light Source (PLS) in Korea. In both cases, the photoelectrons were detected at a take-off angle of 90˚ with respect to the sample surface to maximize the information depth and also the signal intensity. Figure 4.19 shows the relative concentration of N in the GeO_xN_y layer including the surface carbon-related oxygen layer formed due to the exposure to air during the sample transfer and the variation of the Ge *3d* signal as a function of nitridation temperatures. The relative concentration of N with respect to Ge and O was between 10 and 30 atomic %, and linearly increased with the nitridation temperature. A distinct shift of the Ge *3d* feature coming from the Ge-related oxides to the lower binding energy side was observed with increasing nitridation temperature, which indicates the change of the dominant Ge-O or Ge-N bonding configuration and its charge state.

For detailed analysis of the charge states and bonding configuration of Ge and N, an XPS using a synchrotron X-ray source having an energy resolution less than 0.1 eV, which is equipped with a high performance photoelectron analyzer (SCIENTA-200), was used on the same samples. The binding energy was calibrated with reference to the position of bulk Si $2p_{3/2}$ levels at E_b = 99.2 eV for each photon energy. The energy of incident photons was fixed at 200 eV providing a high photoionization cross-section for Ge *3d* and N *1s*. Gaussian-Lorentzian line shapes were used for the deconvolution of the measured peaks after a standard Shirley background subtraction.

Figure 4.20 displays the measured Ge *3d* core level spectra with different nitridation temperatures (500°C ~ 700°C) and the fitted curves. Since there can be many possible combinations of Ge-O and Ge-N binding depending on the number of bonded atoms in the case of GeO_xN_y, the fitting was performed by assuming the existence of only four different charge status (Ge^0, Ge^{+1}, Ge^{+2}, Ge^{+3}, and Ge^{+4}) as is the case in SiO_2.[27] With increasing nitridation temperature and the subsequent increase of N content, the fitting peaks located at the positions associated with Ge^{+2} and Ge^{+3} sharply increased compared to the other peaks. Zanatta *et al.*[28] investigated the change of Ge-N bonding status with different amounts of nitrogen in Ge_3N_4 using an XPS technique and reported the gradual

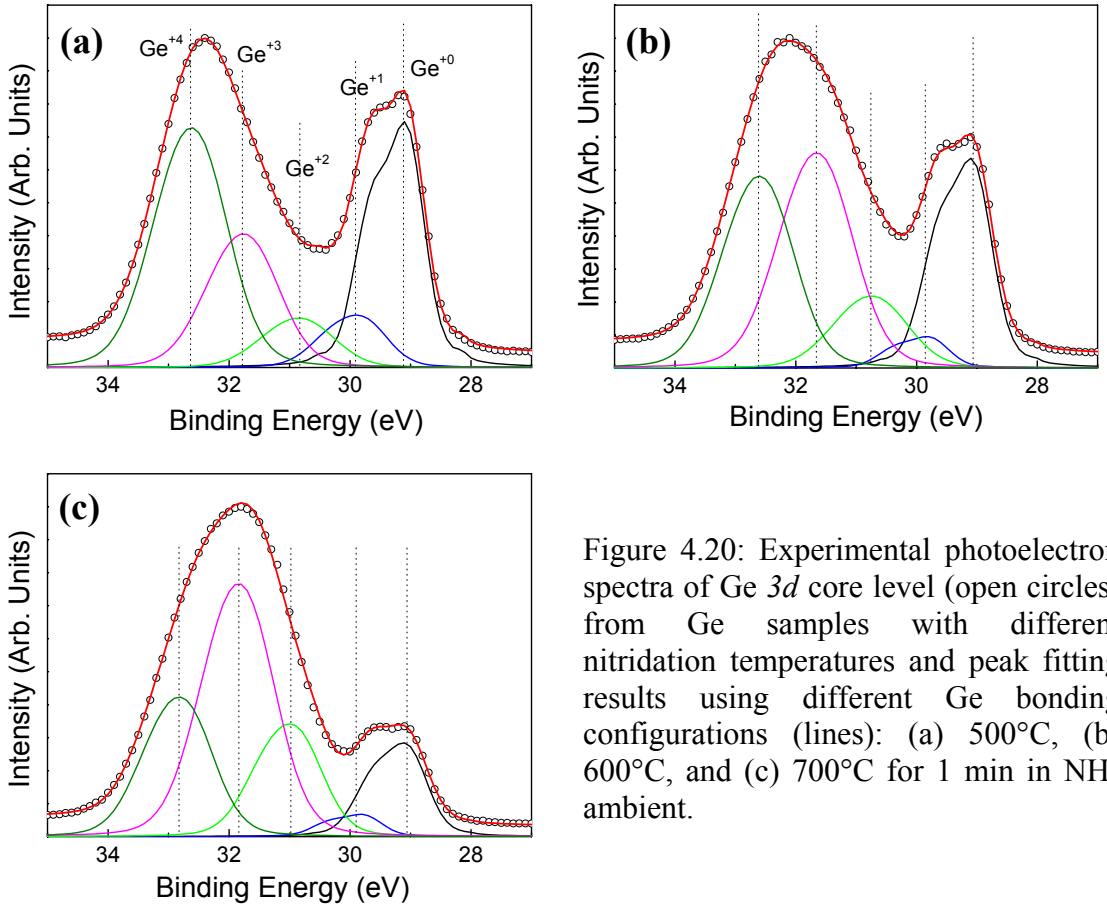

Figure 4.20: Experimental photoelectron spectra of Ge *3d* core level (open circles) from Ge samples with different nitridation temperatures and peak fitting results using different Ge bonding configurations (lines): (a) 500°C, (b) 600°C, and (c) 700°C for 1 min in NH_3 ambient.

increase of the Ge *3d* binding energy up to ~ 3 eV from the reference Ge^0 with increasing N content. This reflects the change in the number of bonded N atoms. The simulated position of Ge^{+3} peak in this work exactly matches with their results and corresponds to the Ge unit being bonded to four N atoms.

The measured N spectra also confirmed these results as shown in Figure 4.21. Due to the lack of experimental or theoretical data for binding energy of N with different configurations, the observed peaks were assigned based on the binding energies of N obtained from Si-oxynitrides.[29,30] Although a small contribution from higher binding energy features (N-GeO_2 at 402 eV and N-Ge_2O at 400 eV) was observed, the major signal located at lower binding energy (~ 397.9 eV) came from N in Ge_3N_4. With increasing nitridation temperature, the N signal coming from Ge_3N_4 increased linearly,

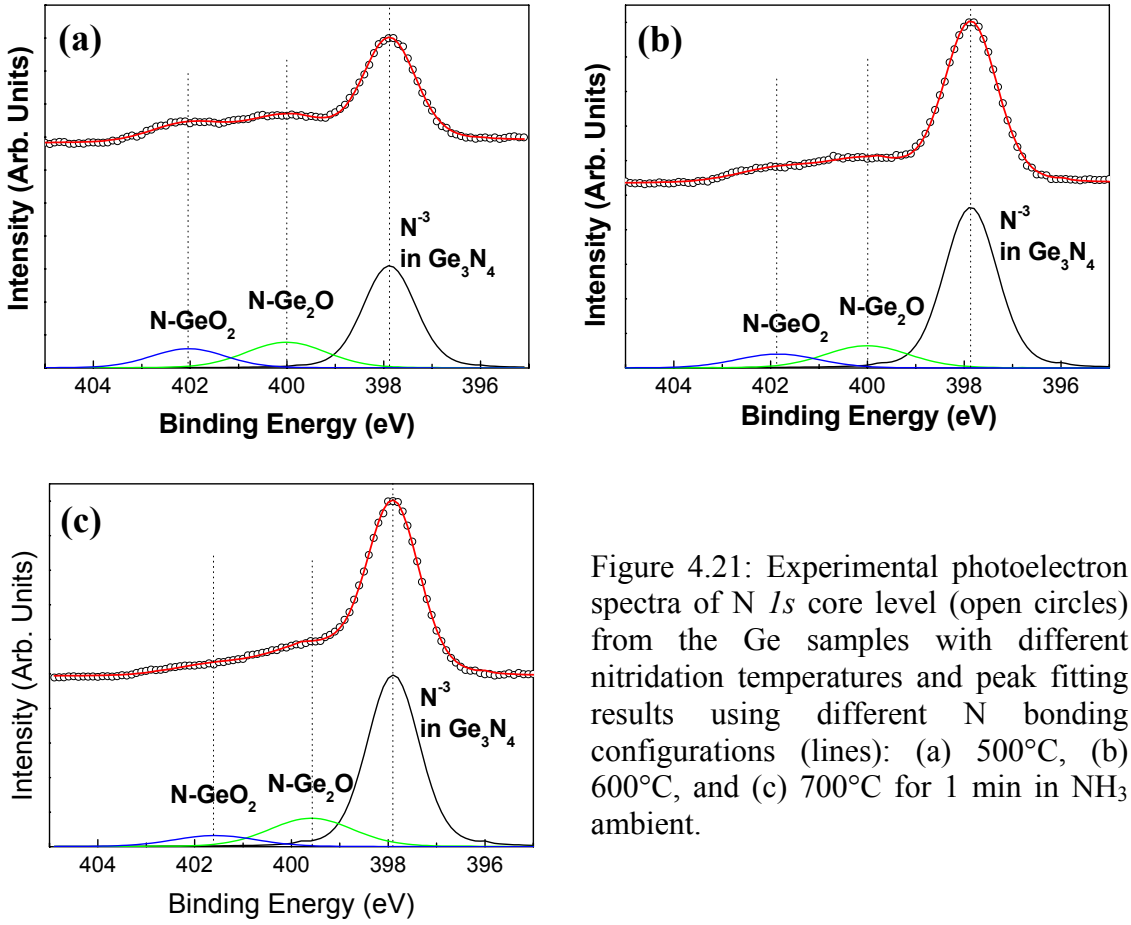

Figure 4.21: Experimental photoelectron spectra of N *1s* core level (open circles) from the Ge samples with different nitridation temperatures and peak fitting results using different N bonding configurations (lines): (a) 500°C, (b) 600°C, and (c) 700°C for 1 min in NH_3 ambient.

while other N peaks having Ge and O bonds were found to decrease in relative intensity. This result is consistent with the previous fitting results for Ge *3d* peaks from films prepared at different nitridation temperatures.

4.5 Summary

In this chapter, the deposition and characterization of ALD-ZrO_2 and HfO_2 dielectric films deposited on Ge substrates having different surface passivation conditions were discussed. High-κ dielectric deposition processes for gate dielectric preparation on Si surfaces generally result in the unavoidable and uncontrolled formation of a thin

interfacial oxide layer. However, ALD-grown ZrO_2 films on Ge (100) and (111) substrates cleaned with HF were found to produce local epitaxial growth ((001) Ge // (001) ZrO_2 and (111) Ge // (111) ZrO_2, respectively) without a distinct interfacial layer. Relatively large lattice mismatch (~ 10 %) between ZrO_2 and Ge produced a high areal density of interfacial misfit dislocations.

H_2O cleaning or chemical oxide passivation of Ge substrates before the high-κ deposition yielded poor electrical results, possibly due to the existence of Ge-oxides having poor electrical properties. C-V measurements showed large hysteresis and abnormal inversion capacitance. However, the leakage current densities measured from these samples were comparable to or even lower than those of Si MOS capacitors of the same EOT. Rapid thermal nitridation of the HF-last Ge surface at 600ºC using NH_3 effectively passivated the surface defects and significantly improved the electrical properties. Although the detailed mechanisms of the effect of N on the electrical behavior of high-κ/Ge stacks are not known at this time, synchrotron XPS and MEIS studies confirmed the existence of Ge-nitride bonding and that the layer behaved as a diffusion barrier for metal species from the metal oxide dielectrics into the Ge substrates.

References

[1] L. Huang, J. O. Chu, S. A. Goma, C. P. D'Emic, S. J. Koester, D. F. Canaperi, P. M. Mooney, S. A. Cordes, J. L. Speidel, R. M. Anderson, and H.-S. P. Wong, IEEE Tran. Electron Devices **49**, 1566 (2002).

[2] C. O. Chui, H. Kim, D. Chi, B. B. Triplett, P.C. McIntyre, and K. C. Saraswat, Tech. Dig. – Int. Electron Devices Meet. **2002**, 437 (2002).

[3] H. Shang, H. Okorn-Schmidt, K. K. Chan, M. Copel, J. A. Ott, P. M. Kozlowsi, S. E. Steen, H.-S. P. Wong, E. C. Jones, and W. E. Haensch, Tech. Dig. – Int. Electron Devices Meet. **2002**, 441 (2002).

[4] C. O. Chui, S. Ramanathan, B. B. Triplett, P. C. McIntyre, and K. C. Saraswat, IEEE Electron Device Lett. **23**, 473 (2002).

[5] W. P. Bai, N. Lu, J. Liu, A. Ramirez, D. L. Kwong, D. Wristers, A. Ritenour, L. Lee, and D. Antoniadis, Tech. Dig. VLSI Symp. **2003**, 121 (2003)

[6] J. J. Ebers, Proc. IEEE **40**, 1361 (1952).

[7] J. D. Plummer, M. D. Deal, and P. B. Groffin, *Silicon VLSI Technology: Fundamentals, Practice and Modeling* (Prentice Hall, New Jersey, 2000).

[8] W. E. Beadle, J. C. C. Tsai, and R. D. Plummer, *Quick Reference Manual for Silicon Integrated Circuit Technology* (John Wiley & Sons, New York, 1985).

[9] S. M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981).

[10] S.- I. Takagi, Tech. Dig. VLSI Symp. **2003**, 115 (2003).

[11] M. Lundstrom, IEEE Electron Device Lett. **18**, 361 (1997).

[12] I. Barin and O. Knacke, *Thermochemical Properties of Inorganic Substances* (Springer, Berlin, 1977).

[13] K. Prabhakaran, F. Maeda, Y. Watanabe, and T. Ogino, Appl. Phys. Lett. **76**, 2244 (2000).

[14] K. Prabhakaran and T. Ogino, Sur. Sci. **325**, 263 (1995).

[15] *CRC Handbook of Chemistry and Physics* (CRC press, Boca Raton, 1989).

[16] H. Kim, C. O. Chui, K. C. Saraswat, and Paul C. McIntyre, Appl. Phys. Lett. **83**, 2647 (2003).

[17] M. Copel, M. Gribelyuk, and E. Gusev, Appl. Phys. Lett. **76**, 436 (2000).

[18] K. J. Yang and C. Hu, IEEE Trans. Electron Devices **66**, 1500 (1999).

[19] F. J. Grunthaner and P. J. Grunthaner, Materials Science Reports **1**, 65(1986).

[20] M. M. Moslehi and K. C. Saraswat, IEEE Trans. Electron Devices **32**, 106 (1985).

[21] M. R. Visokay, J. J. Chambers, A. L. P. Rotondaro, A. Shanware, and L. Colombo, Appl. Phys. Lett. **80**, 3183 (2000).

[22] T. Deegan and G. Hughs, Appl. Surf. Sci. **123**, 66 (1998).

[23] V. Misra, H. Lazar, M. Kulkarni, Z. Wang, G. Lucovsky, and J. R. Hauser, Mater. Res. Soc. Symp. Proc. **567**, 89 (1999).

[24] G. Lucovsky, Y. Wu, H. Niimi, V. Misra, and J. C. Philips, Appl. Phys. Lett. **74**, 2005 (1999).

[25] K.- I. Seo and C. O. Chui, private communication (2003).

[26] A. C. Diebold, D. Venables, Y. Chabal, D. Muller, M. Weldon, and E. Garfunkel, Materials Science in Semiconductor Processing **2**, 103 (1999).

[27] G. Hillinger and F. J. Himpsel, Appl. Phys. Lett. **44**, 93 (1984).

[28] A. R. Zanatta and I. Chambouleyron, Phys. Status Solidi B **193**, 399 (1996).

[29] G.-M. Rignanese, A. Pasquarello, J.-C. Charlier, X. Gonze, and R. Car, Phys. Rev. Lett. **79**, 5174 (1997).

[30] G. F. Cerofolini, A. P. Caricato, L. Meda, N. Re, and A. Sgamellotti, Phys. Rev. B **61**, 14157 (2000).

Chapter 5

Nanolaminates and Metal Electrodes

5.1 Nanolamnates using ALD-ZrO_2 and HfO_2

Beyond single layers of the candidate high-κ gate dielectric materials, nanolaminate structures composed of multiple layers of different metal oxides have been widely investigated for application in high performance transistors and also for dynamic random access memory (DRAM) capacitor applications. Kukli *et al.*[1,2] demonstrated excellent electrical properties with low leakage current and increased permittivity using the Ta_2O_5-ZrO_2 and Ta_2O_5-HfO_2 systems grown by atomic layer epitaxy. Additionally, Zhang *et al.*[3] reported the superiority of ZrO_2-HfO_2 nanolaminate structures compared to the Ta_2O_5-ZrO_2 and Ta_2O_5-HfO_2 systems. More recently, a thermally stable Al_2O_3-HfO_2 nanolaminate system was investigated for integrated capacitor applications by Cho *et al.*[4] However, detailed microstructural characterization of metal oxide nanolaminate films and the effects of the layer deposition sequence on the final film microstructure have received limited attention to date.

In this section, nanolaminate structures containing ALD-ZrO_2 and HfO_2 layers were fabricated with different deposition sequences and also with different individual layer thicknesses. Microstructural evolution of nanolaminates having different starting layers (ZrO_2 or HfO_2) was studied by transmission electron microscopy (TEM) and

atomic force microscopy (AFM).[5] Possible mechanisms responsible for the observed microstructures of the films were investigated.

5.1.1 Microstructures of ZrO_2 - HfO_2 alloy films

As described in Chapter 3, the as-grown microstructures of ZrO_2 and HfO_2 thin films deposited by ALD on Si substrates are significantly different: polycrystalline (tetragonal) and amorphous, respectively. However, due to the similarity of their equilibrium crystal structure and materials properties (electronic structure, lattice constants, and bonding coordination numbers), ZrO_2 and HfO_2 films are expected to exhibit a full range of solid solubility, as shown in the equilibrium phase diagram[6] for this binary system, shown in Figure 5.1. In this phase diagram, the cubic-phase field was

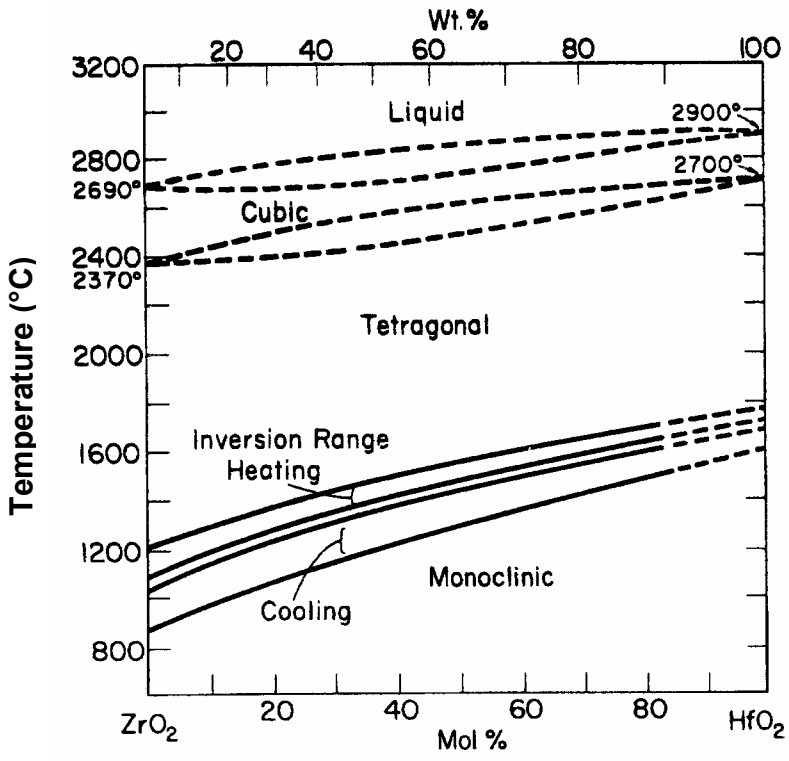

Figure 5.1: Reported[6] temperature-composition phase diagram of the ZrO_2-HfO_2 system.

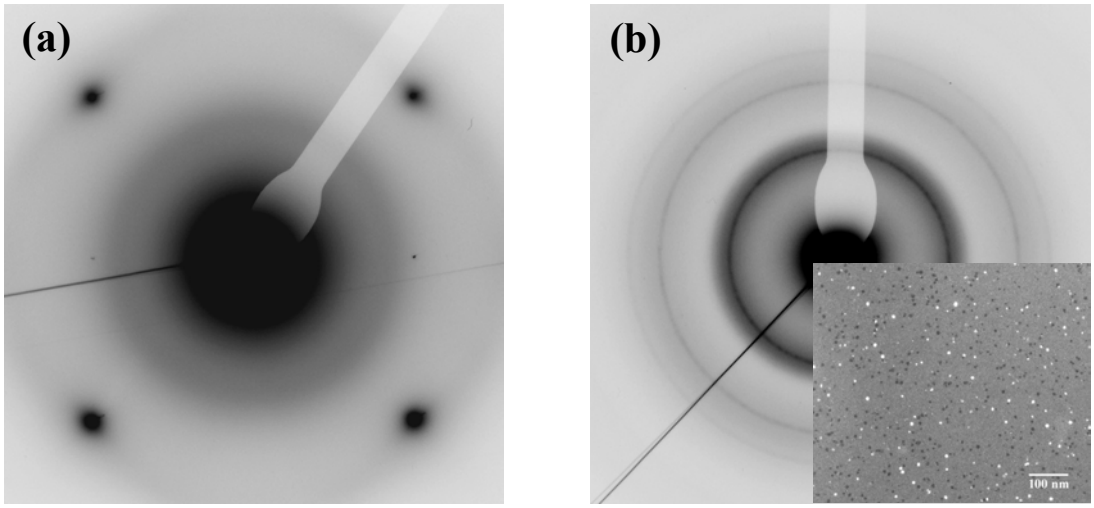

Figure 5.2: Microstructural analysis of ZrO_2-HfO_2 alloy films stacked in thin layers (0.5 ~ 0.6 nm individual layer thickness): (a) SADP of alloy film starting with HfO_2 and ending with ZrO_2, (b) SADP and dark field image (inset) of alloy film starting with ZrO_2 and ending with HfO_2.

included because tetragonal-cubic inversion was reported, and also the experimentally determined monoclinic-tetragonal inversion was presented as a solid line with the start and finish of the heating and cooling. Because the growth rates of ZrO_2 and HfO_2 can be accurately controlled with sub-monolayer precision by ALD processing, it is possible to make a nearly-complete ZrO_2-HfO_2 alloy film by alternately depositing each metal oxide.

In order to investigate the effect of the starting material on the final microstructure of alloy films, some of the samples were fabricated with different starting species. Each alternating ZrO_2 and HfO_2 layer was deposited for 10 cycles, which corresponds to 0.5 – 0.6 nm film thickness for the ALD conditions used, and the total number of blayers was 4. In most experiments, an even number of metal oxide layers was deposited; therefore, the starting and ending materials were different metal oxides.

Figure 5.2 shows TEM plan-view images and also selected area electron diffraction patterns obtained from alloy films having different sequences. The alloy film which started with an amorphous HfO_2 layer and ended with a crystalline ZrO_2 layer exhibited an amorphous structure as seen in Fig. 5.2 (a); however, a mixed structure

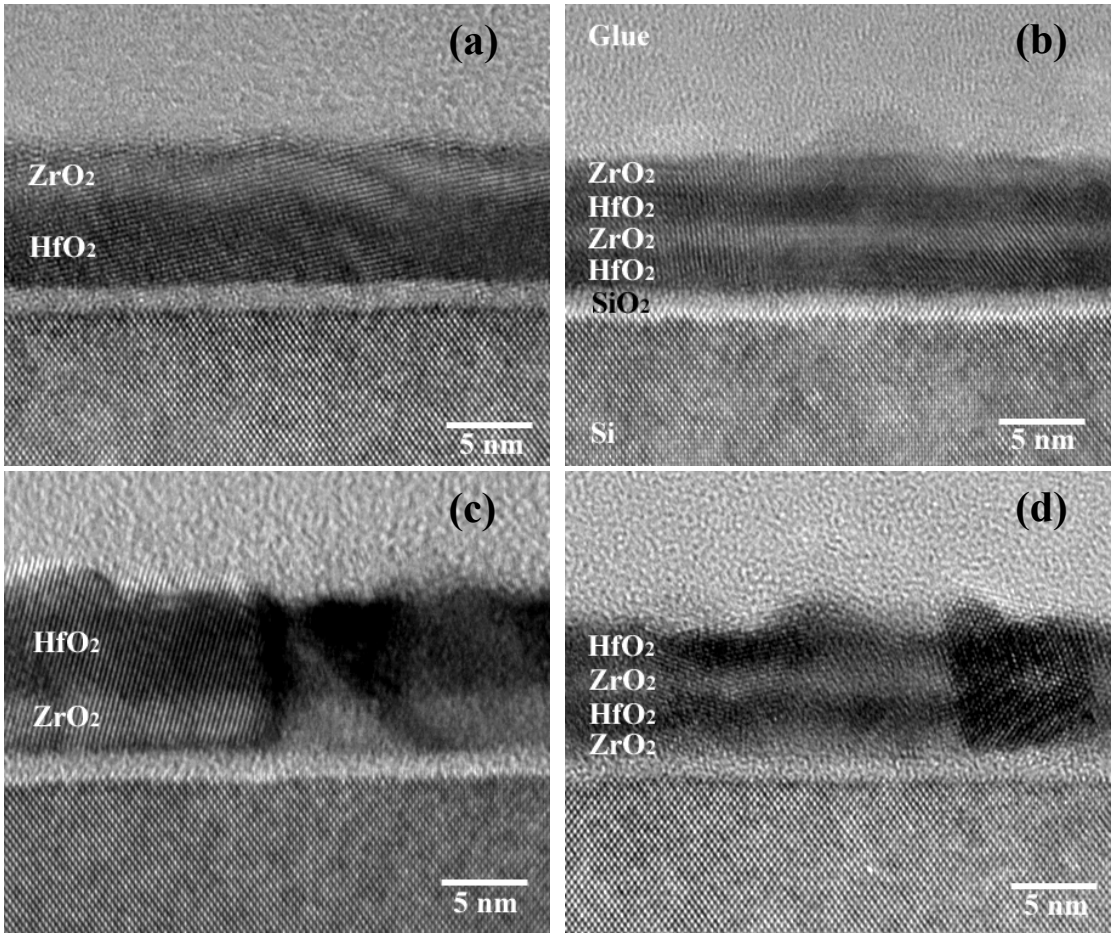

Figure 5.3: Cross-sectional high-resolution TEM images of various nanolaminates having even numbers of layers with different deposition sequences: (a) HfO_2 + ZrO_2, (b) 2×(HfO_2 + ZrO_2), (c) ZrO_2 + HfO_2, and (d) 2×(ZrO_2 + HfO_2).

composed of both amorphous and crystalline regions was observed by changing the layer sequence (Figure 5.2 (b)). It is believed that the microstructure of the starting layer plays a key role in the final microstructure of the alloy film. Because each layer in the deposited sequence has a thickness comparable to one unit cell, the structure of each layer is strongly influenced by the presence of nearby interfaces and templating effects from underlying layers. In the case of the alloy started with HfO_2, it is believed that the initial HfO_2 template, which has a strong tendency to be amorphous in thin ALD films, effectively suppresses the crystallization of the subsequent ZrO_2 layer during the

following deposition cycles. However, in the case of the alloy film that began with a ZrO_2 layer, the tendency of this metal oxide to form as a crystalline film produced a distribution of crystalline seeds embedded in an amorphous alloy matrix. Indexing of the selected area electron diffraction pattern revealed only a tetragonal phase as shown in Figure 5.2 (b). This demonstrates the significant role played by the initial layer because, of these two metal oxides, only ZrO_2 exhibits a tetragonal phase in the as-deposited state, as described in Chapter 3.

5.1.2 Microstructures of ZrO_2 - HfO_2 nanolaminates

Nanolaminate samples having a finite thickness for each layer were made in order to investigate the microstructural changes that occur during deposition of different layer sequences. Figure 5.3 shows representative cross-sectional TEM images obtained from samples having different layer sequences and numbers of layers. The total number of layers was fixed at two or four so that the starting and ending layers were different for all the samples. Although ZrO_2 and HfO_2 should form a complete solid solution at equilibrium according to the bulk phase diagram, a clear interface with no TEM-detectable evidence of inter-mixing between each layer was observed for the ALD deposition conditions (T_{dep} = 300°C) employed in our experiments. All of the samples with bilayer thickness greater than approximately 2 nm exhibited TEM lattice images and electron diffraction patterns that were consistent with fully crystalline nanolaminates. Lattice fringes in the cross-sectional images were typically found to extend across the entire film thickness. Within each grain, a layer-to-layer epitaxial relationship was observed as a consequence of the close lattice constant match between ZrO_2 and HfO_2. For nanolaminate samples that started with a ZrO_2 layer, significantly greater surface roughness was observed. The starting layer was the parameter found to have the most significant effect upon overall roughness.

Figure 5.4 shows AFM images measured on two different nanolaminate samples having different deposition sequences. The total number of bilayers is either 1 or 2. The RMS (Root Mean Square) roughness value obtained from 1 μm x 1 μm AFM scans was ~ 0.3 nm for the sample in which the first layer deposited was HfO_2 and the final layer was ZrO_2. However, as shown in the TEM pictures previously, the nanolaminates started with ZrO_2 and ended with HfO_2 consistently showed higher RMS surface roughness of 0.4 ~ 0.6 nm.

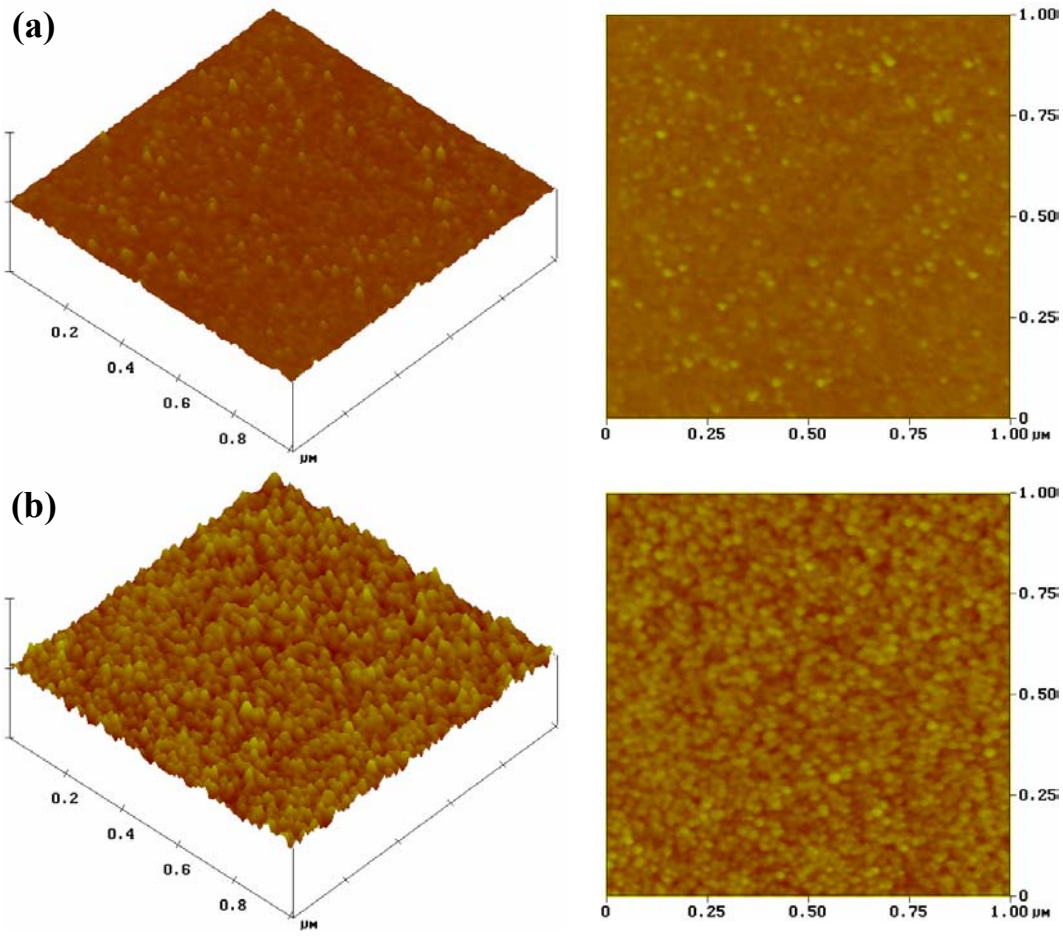

Figure 5.4: Two- and three-dimensional AFM images of nanolaminates with different stacking sequences: (a) samples started with HfO_2 and capped with ZrO_2 (m×(HfO_2 + ZrO_2)), and (b) samples started with ZrO_2 and capped with HfO_2 (m×(ZrO_2 + HfO_2)). Here m is the number of bilayers, either 1 or 2.

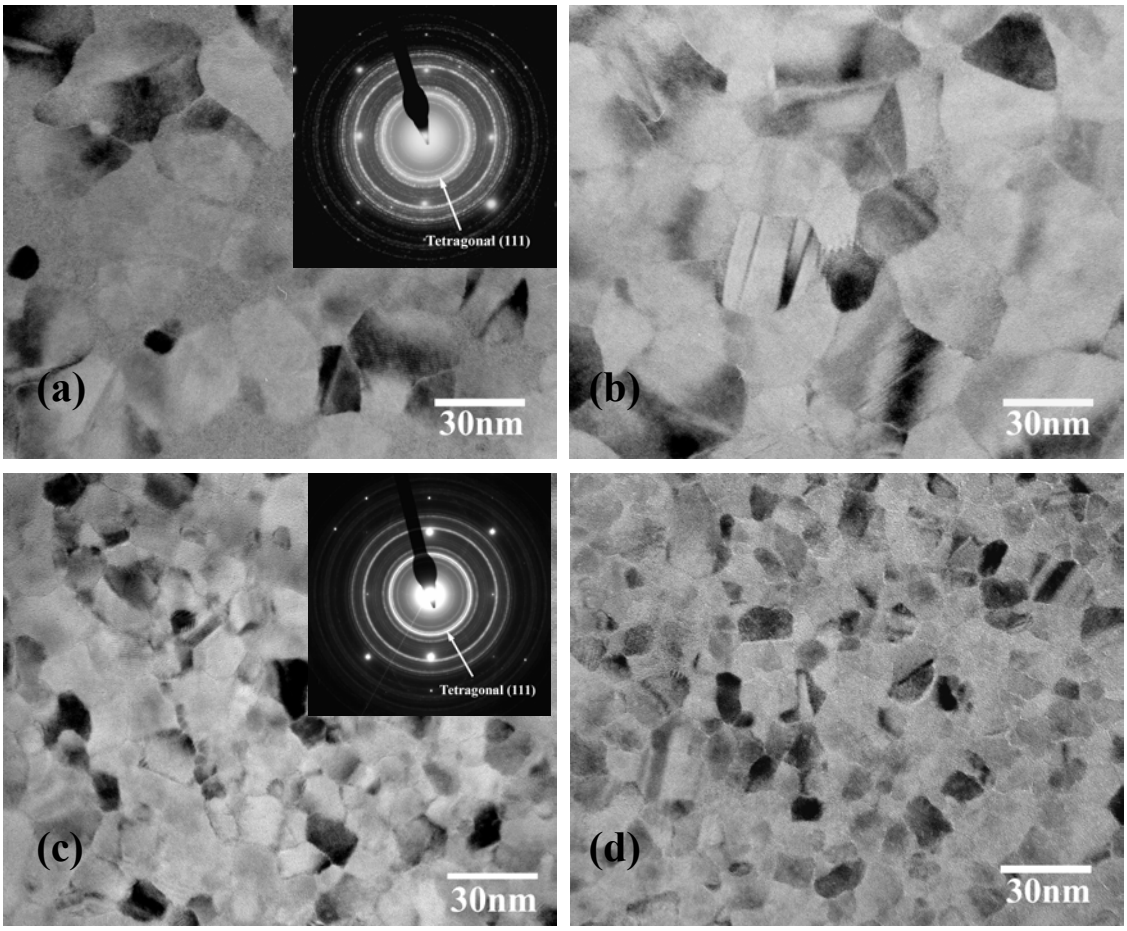

Figure 5.5: Bright field TEM images and SADP of various nanolaminates having even numbers of layers with different deposition sequences: (a) HfO_2 + ZrO_2, (b) 2×(HfO_2 + ZrO_2), (c) ZrO_2 + HfO_2, and (d) 2×(ZrO_2 + HfO_2).

Bright field TEM imaging and diffraction analysis were performed on the nanolaminate samples composed of an even numbers of layers (Figure 5.5). All the nanolaminates prior to thermal annealing consisted of mixed crystalline phase having both tetragonal and monoclinic electron diffraction signatures, regardless of the sample structure. This result is consistent with the previous phase analysis of single-layer HfO_2 films crystallized by post-deposition thermal annealing (Chapter 3). Although the crystalline phases are identical, the grain sizes of nanolaminates with different sequences

are significantly different as shown in the bright field TEM images. In the case of nanolaminates beginning with a ZrO_2 layer, the average grain size was ~ 10 nm. However, a much larger average grain size, > 30 nm, was observed in the nanolaminates initiated with a HfO_2 layer deposition. Differences in the respective grain size distributions are also apparent in the diffraction patterns. A smoother and more continuous diffraction ring was measured from ZrO_2-first nanolaminates, which had a smaller average grain size.

5.1.3 Model: dependence of nanolaminate microstructure on starting and capping material

The different final grain size and surface roughnesses of nanolaminates with different stacking sequences are most likely attributable to the influence of either the initial or the final layer material. The microstructure of the starting layer can change that of the subsequent material by acting as a growth template. Conversely, the final capping layer may have a different surface energy that can lead to capillary instability of the total laminate stack, thus changing the microstructure and surface roughness. In order to elucidate the role of these possible effects, several nanolaminate samples having odd number of layers were synthesized. Figure 5.6 shows cross-sectional TEM images of samples that started and ended with deposition of the same material. These results indicate that the morphology of the nanolaminate is determined by the starting layer material and not the ending layer.

Based on the microstructural characterization of ZrO_2/HfO_2 nanolaminate structures with different stacking sequences, a qualitative microstructural evolution model for ZrO_2/HfO_2 nanolaminates grown by ALD is shown in Figure 5.7. As a single layer, ALD-ZrO_2 has a tendency to be poly-crystalline with a tetragonal phase, whereas ALD-HfO_2 tends to be amorphous as-deposited. When each layer thickness is less than a certain critical film thickness (~ one unit cell in thickness), the total laminate stack has a strong tendency to be amorphous regardless of the microstructure of the starting material.

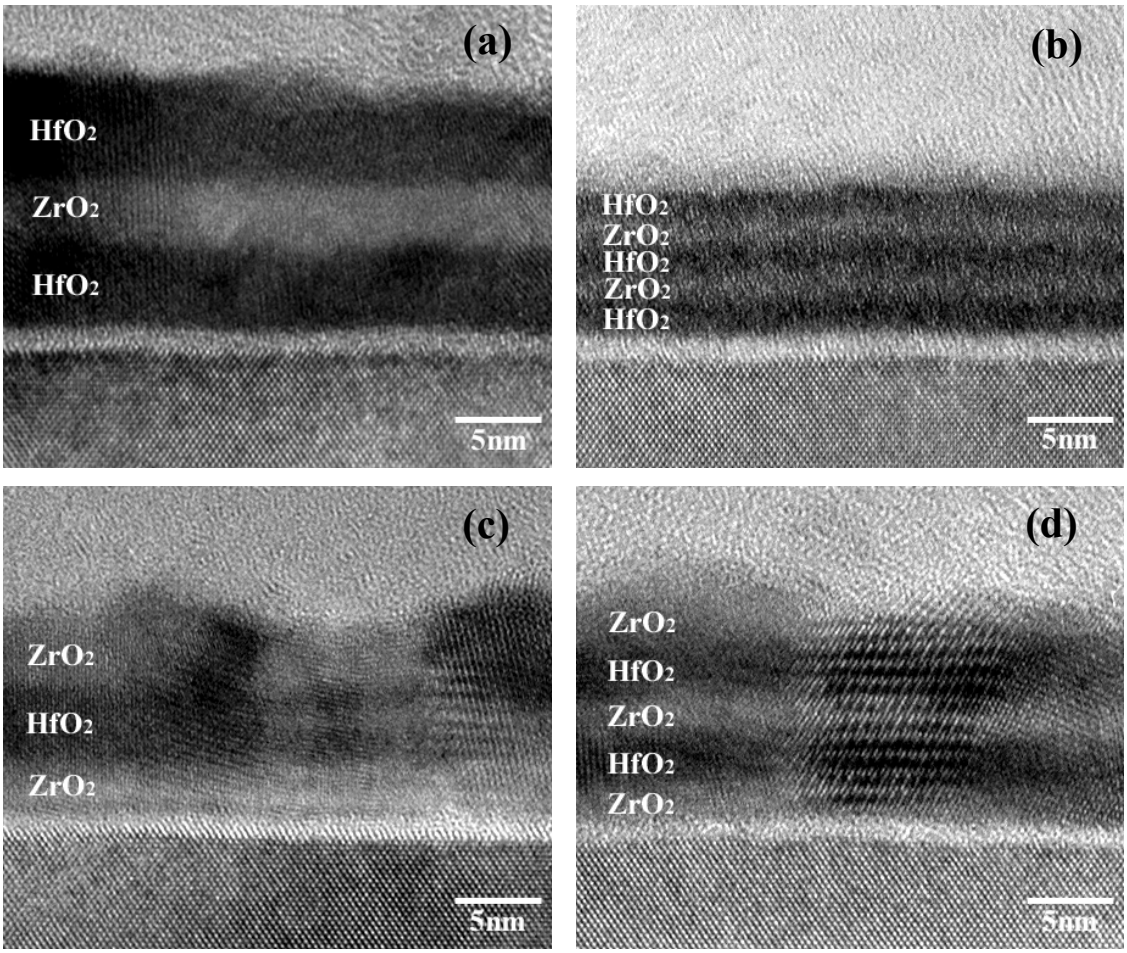

Figure 5.6: Cross-sectional high-resolution TEM images of various nanolaminates having odd numbers of layers with different deposition sequences: (a) HfO_2 + ZrO_2 + HfO_2, (b) 2×(HfO_2 + ZrO_2) + HfO_2, (c) ZrO_2 + HfO_2 + ZrO_2, and (d) 2×(ZrO_2 + HfO_2) + ZrO_2.

Although the alloy films (bilayer period < 2 nm) that began with a ZrO_2 layer exhibited a distribution of crystalline tetragonal-phase seeds, the majority of film volume was amorphous.

For larger layer thicknesses, the microstructure of the starting template layer determines the final microstructure of the nanolaminate stack. As shown Figure 5.7, if the layer sequence starts with amorphous HfO_2, the following crystalline ZrO_2 acts as a template for crystallization of the underlying HfO_2. Relatively sparse nucleation and

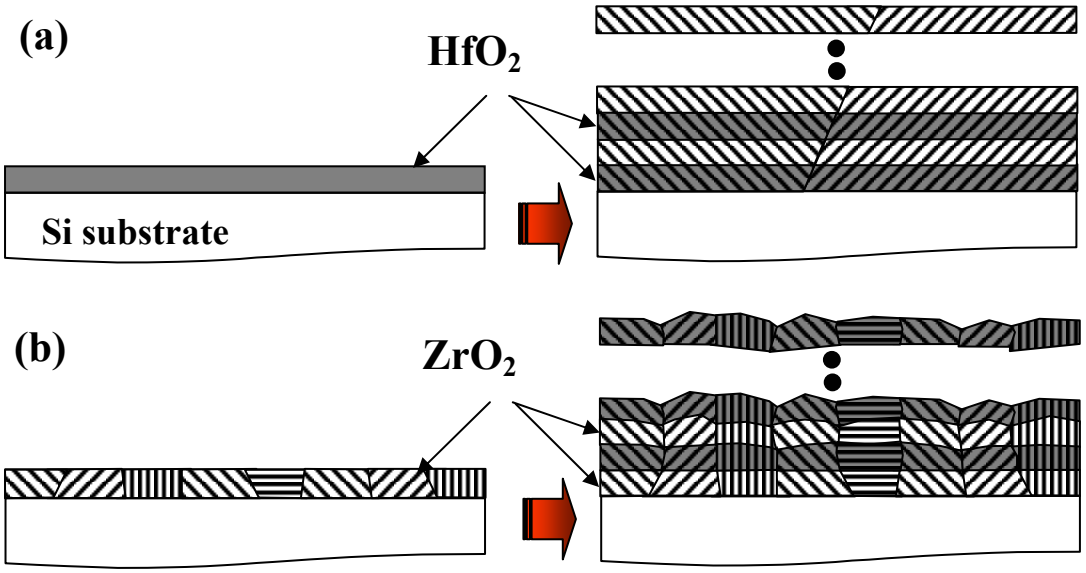

Figure 5.7: Proposed model for microstructural evolution of ZrO_2-HfO_2 nanolaminates with different stacking sequences: (a) initially-amorphous HfO_2 layer is crystallized during the subsequent crystalline ZrO_2 deposition to give smooth films and large, (b) nano-crystalline ZrO_2 roughens and generates small grain sized epitaxial HfO_2 deposition.

recrystallization of HfO_2 during this process result in a large-grained nanolaminate in which the average grain size is significantly greater than that observed in single-layer ALD-ZrO_2 films. If the starting material is already nanocrystalline, such as ALD-ZrO_2, the following HfO_2 layer tends to grow epitaxially on top of each small ZrO_2 grain in the starting layer. Compared to the initial atomically smooth amorphous template and the subsequent crystallization process, the nanocrystalline ZrO_2 template results in increased surface roughness as within-grain epitaxial growth occurs during the subsequent steps of the ALD process.

5.2 ALD-ZrO_2 and HfO_2 with reactive metal electrodes

Deposition of a metal oxide film on a Si substrate is often accompanied by the growth of a thin SiO_2-containing interfacial layer that results from oxidation of the Si surface.[7] The interface layer forms because the metal oxide layer must generally be deposited in an oxygen-rich ambient in order to achieve the correct metal-to-oxygen stoichiometry. Furthermore, ALD, one of the most promising methods for controlled deposition of ultra-thin metal oxides onto Si, requires a high density of surface sites for precursor adsorption as discussed in Chapter 1.[8] Experimentally, it is found that a SiO_2-based surface passivation provides an ideal template for ALD of high-κ metal oxides on Si.[9] It is, therefore, common practice to passivate the Si surface with a high-quality SiO_2 film of known thickness prior to metal oxide deposition by ALD. The interface layer, whether intentionally added or formed as a result of metal oxide deposition itself, can have a profound effect on the behavior of the metal oxide/interface layer/Si structure. Because capacitances in series add in reciprocal fashion, the dielectric properties of the interface layer can dominate the characteristics of the entire gate stack, thus limiting the scaling benefits of incorporating the high-κ layer in the device. For this reason, there is great interest in developing approaches for reducing the thickness of the interface layer and, perhaps, eliminating it entirely.

In this section, a method is introduced to remove the SiO_2-based interface layer after deposition of HfO_2 and ZrO_2 gate dielectrics on Si substrates, and the resulting metal oxide/Si interface structures and electrical properties are described. This approach makes use of the thermodynamic properties of reactive metals which can dissolve large amounts (> 10 atomic %) of oxygen without forming a new oxide phase. It is shown that Ti is a suitable metal for this purpose. By depositing thin films of Ti onto a stable metal oxide film which has a high permeability for oxygen, the interface layer between the metal oxide film and Si substrate can be altered and, in some cases, removed. Oxygen ions from the interface layer diffuse across the continuous HfO_2 and ZrO_2 dielectric layers and dissolve into the Ti overlayer at temperatures near 300 K. Silicon atoms

initially in the interface layer appear to be reincorporated in the surface of the Si substrate as the SiO_2-based interface decomposes.

5.2.1 Electrical properties

Firstly, ~ 3.9 nm-thick ZrO_2 and ~ 3.6 nm-thick HfO_2 films were grown on Si substrates passivated with chemical oxides (~ 1.5 nm). After high-κ film deposition, the dielectric stacks were capped with metal top electrodes. Top electrode materials investigated included Pt (50 nm), Al (100 nm) and Ti (30 nm). A thin film of Pt (50 nm) was used to cap the reactive Ti metal electrodes to prevent its subsequent oxidation on exposure to air. The metal overlayers were deposited by e-beam evaporation at room temperature. MOS capacitor samples were studied electrically using capacitance-voltage (CV) and current-voltage (IV) analysis both before and after a 300°C, 4% H_2/96 % N_2 forming gas anneal.

Comparison of CV plots obtained from Ti/high-κ/Si capacitors to those of

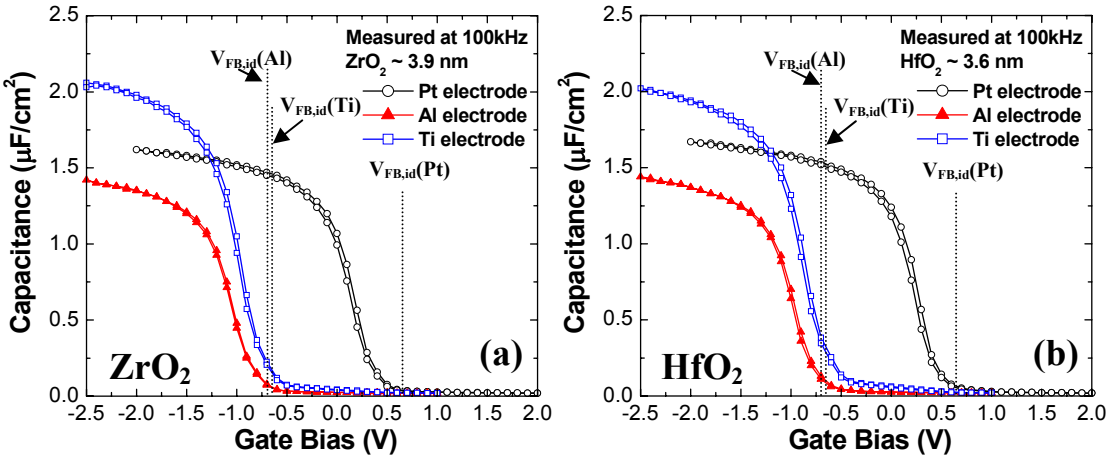

Figure 5.8: C-V data obtained from Al-, Pt- and Ti-electroded (a) ZrO_2 and (b) HfO_2 high-κ capacitors on p-type Si substrates after 300°C, 30 min forming gas anneal; measurements were taken at 100 kHz frequency and both bias sweep directions are shown.

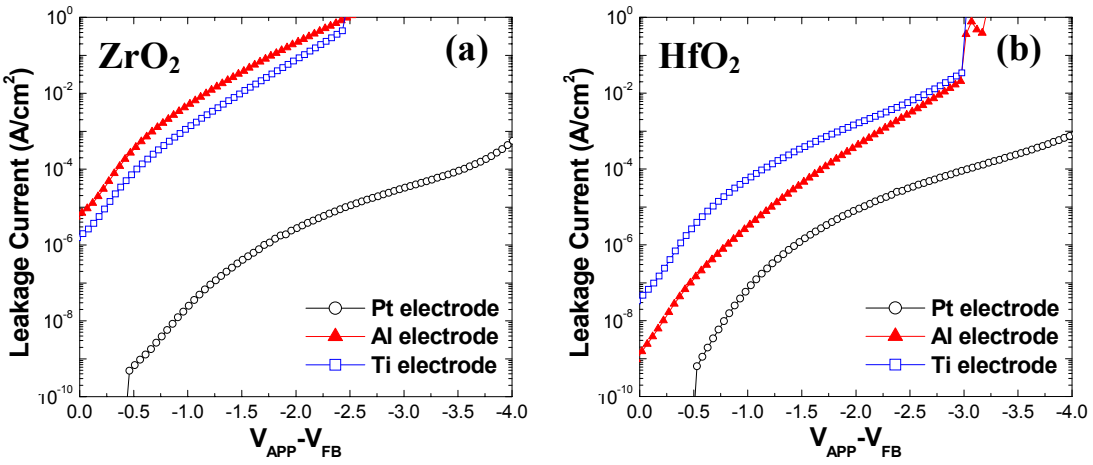

Figure 5.9: J-V data measured from Al-, Pt- and Ti-electroded (a) ZrO_2 and (b) HfO_2 high-κ capacitors on p-type Si substrates after 300°C, 30 min forming gas anneal; gate voltage shown is referenced to the flat band voltage for each electrode material.

Pt/high-κ/Si and Al/high-κ/Si capacitors after forming gas anneal (Figure 5.8) indicates that the capacitance density of the Ti-electroded capacitors was significantly higher even though all capacitor sets were processed identically except for the identity of the gate electrode. The capacitance-derived equivalent oxide thickness (EOT), proportional to the inverse of the gate capacitance density, is by extension smaller for Ti-electroded high-κ capacitors than for otherwise-identical Pt-electroded samples. This EOT difference was also observed, with similar magnitude, for as-deposited Ti-electrode capacitors which were not given a forming gas anneal. The EOT values extracted directly from the accumulation capacitance of the Ti-electroded capacitors (without quantum mechanical corrections) were 1.6 nm for ZrO_2 and 1.7 nm for HfO_2 dielectric layers. In contrast, the Pt-electroded EOT values were ~ 2.1 nm for ZrO_2 and HfO_2. In the case of Al-electroded capacitors, EOT values were much larger (2.4 ~ 2.5 nm) for both ZrO_2 and HfO_2 and this is believed to be caused by the interfacial reaction between high-κ dielectric and Al electrode, which will be discussed in the following sections.

In addition to the variations in accumulation capacitance density among samples in Figure 5.8, the Al- and Ti-electroded capacitors exhibit CV curves which are shifted with respect to the Pt-electrode data. This shift in flat band voltage is in good

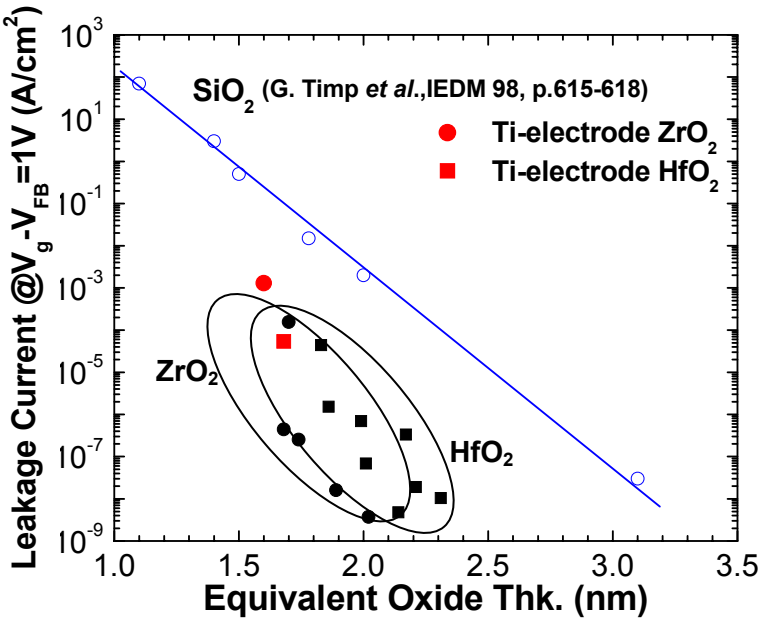

Figure 5.10: Leakage current densities of Pt-electroded ZrO_2 and HfO_2 high-κ capacitors on p-type Si substrates after 400°C, 30 min forming gas anneal as a function of electrically measured equivalent oxide thickness (EOT); leakage current density was measured at $|V_{APPLIED}-V_{FB}| = 1$ (V). For comparison, the leakage current density of Ti-electoded ZrO_2 and HfO_2 high-κ capacitors are displayed.

quantitative agreement with the differences in the reported workfunctions of Al and Ti compared to that of Pt. The theoretically-predicted[10] ideal flat band voltages of the Al-, Ti- and Pt-electroded capacitors are -0.71 V, -0.66 V and +0.66 V, respectively, as shown in Figure 5.8. The CV data in Figure 5.8 show both bias sweep directions, and there is minimal hysteresis for the CV characteristics obtained.

Leakage current densities measured across the metal electrode/high-κ/Si capacitors after the forming gas anneal are shown in Figure 5.9. As a result of the smaller equivalent electrical thickness and the smaller barrier height of Ti/high-κ/Si stacks, their leakage current densities are consistently higher than those of the Pt/high-κ/Si capacitors. For Al-electroded capacitors, relatively high leakage currents were measured due to the decrease of the barrier height and the increase in the number of the trapping sites formed by interfacial reaction, which will be discussed in the next section. In terms of the absolute value of their leakage current densities, the Ti-electroded

capacitors are quite promising. The Ti/HfO_2/Si samples, with EOT = ~ 1.7 nm, have a leakage current density of ~ 5×10^{-5} A/cm^2 at 1 V from the flat band condition. This current is four orders of magnitude smaller than that measured across high-quality SiO_2 films of the same EOT[11] (Figure 5.10), due to the larger physical thickness of the high-κ layer compared SiO_2 of the same EOT, minimizing direct band-to-band tunneling conduction. In addition, Ti-electroded ZrO_2 and HfO_2 exhibit comparable leakage current densities with those of Pt-electroded ZrO_2 and HfO_2, as shown in Figure 5.10.

5.2.2 Microstructural characterization

In order to verify the possible reaction promoting removal of the interfacial oxide layer by incorporation of a reactive metal electrode, microstructural characterization using high resolution TEM and annular dark field STEM performed on cross-sectioned samples were obtained. Figure 5.11 shows the cross-sectional HR-TEM images of ZrO_2 and HfO_2 with Al electrode after forming gas annealing. A thin ~ 0.8 nm-thick reacted layer was clearly seen in the case of the Al/ZrO_2 interface (Figure 5.11 (a)). Although accurate thermodynamic data for metal oxides with different phases and thin film forms are not available, an approximate guideline can be estimated through analysis of thermodynamic data for bulk materials. This data suggests the possibility of reaction between the Al electrode and ZrO_2 high-κ layer. The greater thermodynamic stability of Al_2O_3 relative to its metal in comparison to Zr/ZrO_2[12] may explain the apparent reactivity of the Al/ZrO_2 samples, although further work is required to unambiguously identify the low-average atomic number phase formed at Al/ZrO_2 interface. This interfacial reaction may also account for the large leakage current density and also the higher EOT values of the Al/ZrO_2/Si capacitors if, as expected, the reacted layer has a low dielectric constant. In the case of the Al/HfO_2 stack, although no interfacial layer was evident in the cross-sectional TEM image (Figure 5.11 (b)), the existence of a reacted layer is likely due to the similar thermodynamic properties of HfO_2 and ZrO_2. Additionally the increase in EOT is similar for both HfO_2 and ZrO_2 with Al electrodes.

The reason for the low EOT value of the Ti-electroded capacitors is evident in both high resolution TEM and annular dark field STEM. The TEM images in Figure 5.12 compare the layer structures present in Ti-electroded gate stacks with ZrO_2 and HfO_2 dielectrics. The amorphous, light contrast layer, which is present at the dielectric/Si interface in the Al-electroded sample (Figure 5.11), was substantially thinned and,

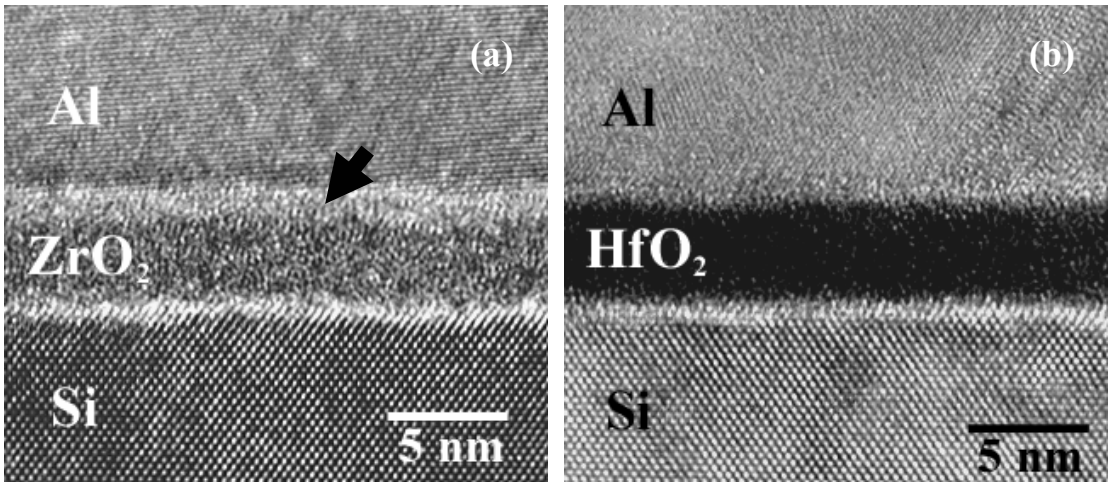

Figure 5.11: Cross-sectional HR-TEM images of (a) ZrO_2 and (b) HfO_2 dielectrics with Al metal electrode after a forming gas annealing (300°C, 30min). The arrow indicates the ~ 0.8 nm-thick reacted layer (Al_2O_3).

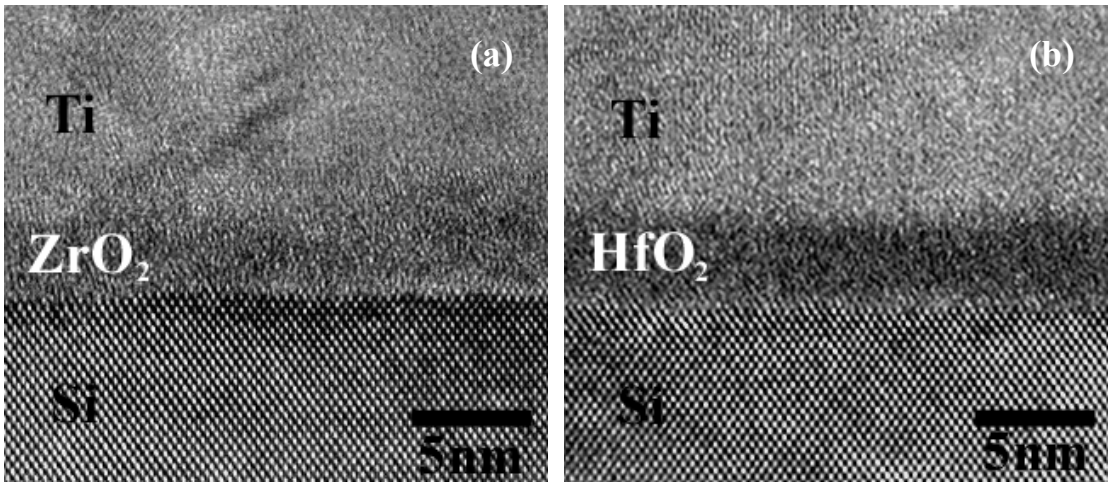

Figure 5.12: Cross-sectional HR-TEM images of (a) ZrO_2 and (b) HfO_2 dielectrics with Ti metal electrode after a forming gas annealing (300°C, 30min).

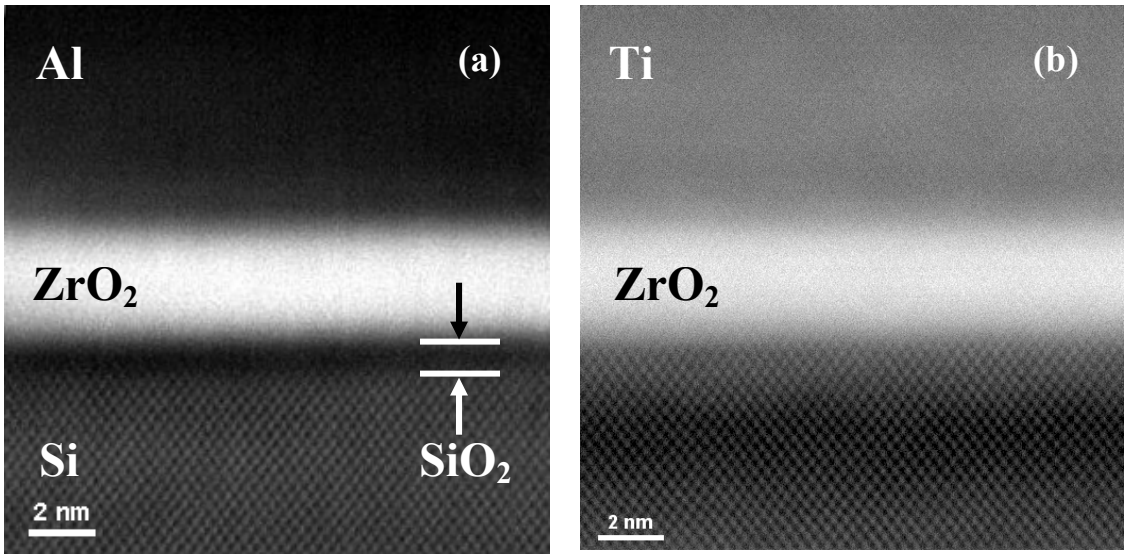

Figure 5.13: High-angle annular dark field image of (a) Al-electroded and (b) Ti-electroded ZrO_2 gate stacks after 300°C, 30 min forming gas anneal.[13]

possibly, removed entirely from the Ti-electroded samples. In addition, a distinct difference in the contrast exists between the high-κ dielectric films electroded with Al versus Ti, suggesting a possible chemical change in the high-κ dielectrics.

A similar result was obtained from STEM/EELS studies of the Al- and Ti-electroded ZrO_2 gate stacks.[13] High angle annular dark field (HAADF) imaging in STEM is much more sensitive to the average atomic number of species viewed in specific regions of an electron-transparent foil than conventional TEM.[14] Therefore, the annular dark field contrast gives a directly-interpretable image of local composition variations. The HAADF image of the Al-electroded ZrO_2 sample in Figure 5.13 (a) shows the typical dark contrast band associated with the low-average atomic number, SiO_2-based interface oxide present between the high-κ film and Si substrate. Its thickness is similar to that of the chemical oxide present on the Si substrate surface prior to ALD growth of the high-κ layer. In addition, a thinner dark-contrast band is visible at the Al/ZrO_2 interface, which is also confirmed in the previous high resolution TEM images.

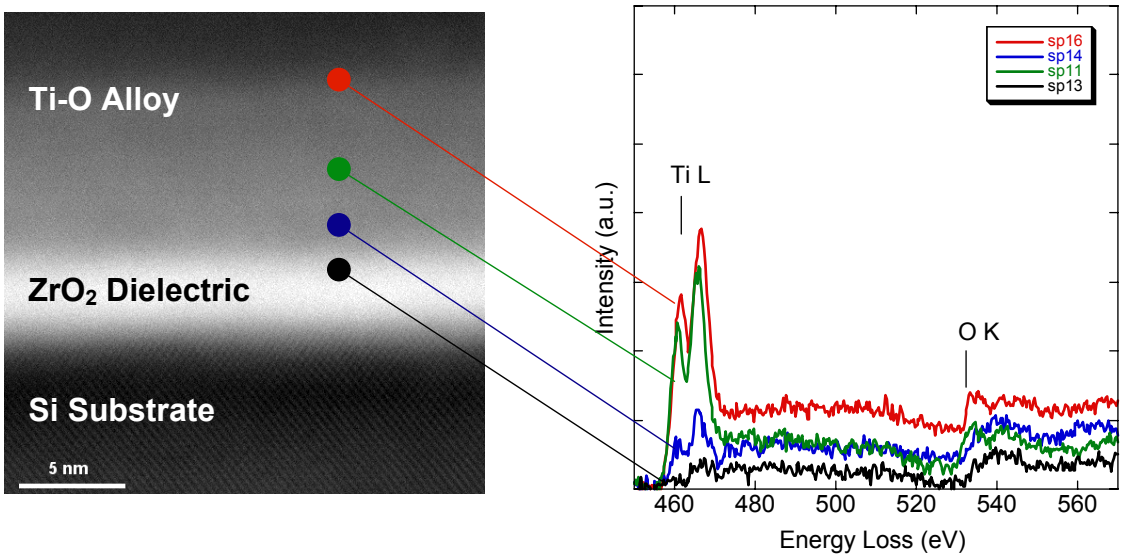

Figure 5.14: High-angle annular dark field image (left) and accompanying local EELS spectra obtained from Pt/Ti/ZrO_2/Si gate stacks after 300°C, 30 min forming gas anneal.[13]

In contrast to the Al-electrode results, the HAADF image of the Ti-electroded sample in Figure 5.13 (b) shows the absence of a dark contrast interfacial region in the Ti/ZrO_2/Si capacitor structure. No evidence for a low atomic number interface layer is found in the Ti-electroded gate stacks. EELS spectra (Figure 5.14 (right)) obtained from the same region indicate that a significant oxygen concentration is present in the Ti overlayer and that no Ti is detected at the ZrO_2/Si interface.

5.2.3 Thermodynamic analysis for a Ti-electroded gate stack

A thermodynamic driving force exists for decomposition of the SiO_2 interface layer in these structures and incorporation of the liberated oxygen atoms into the Ti overlayer. The overall chemical reaction for this process can be written as follows:

$$\frac{C}{2}SiO_2 + Ti \rightarrow \frac{C}{2}Si + TiO_C \qquad \text{Equation (5.1)}$$

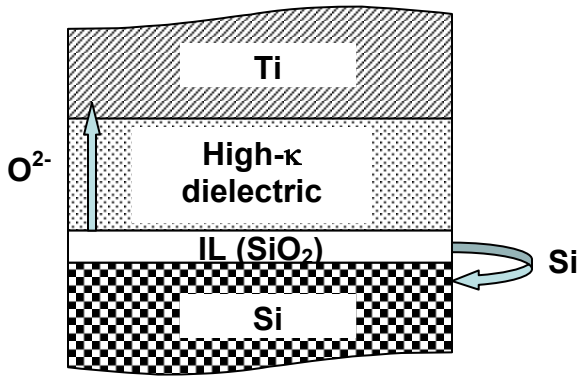

Figure 5.15: Schematic diagram showing the proposed process of oxygen ion diffusion across the ZrO_2 layer and incorporation of Si into the substrate surface during interfacial SiO_2 decomposition.

where TiO_C is the Ti-O alloy overlayer. In reaction (5.1), the Si atoms are assumed to reincorporate in the underlying single crystal substrate during decomposition of the interfacial layer. This is consistent with previous TEM observations, which failed to detect any evidence of a defective Si layer at the metal oxide/silicon interface of the Ti-electroded capacitors. Using published data for the Gibbs free energy of formation of SiO_2 from its elements[15] and the equilibrium oxygen vapor pressure above Ti-O alloys of varying stoichiometry,[16] one can show that the standard Gibbs free energy change associated with reaction (5.1) is large and negative for all values of *C* up the oxygen solubility limit in α-Ti ($C < 0.49$).[17] Reaction (5.1) experiences a strong driving force to proceed for all temperatures of interest in semiconductor processing. Similar large thermodynamic driving forces exist for other interface layer and metal overlayer combinations in the limit that the metal is initially highly pure. However, the Ti overlayer is special because of its very large capacity for dissolving oxygen compared to most metals.

The ability of Ti films to decompose native silicon oxide layers onto which they are directly deposited has previously been demonstrated.[18,19] The reaction has been reported to occur via low temperature dissolution of oxygen into the Ti overlayer, similar

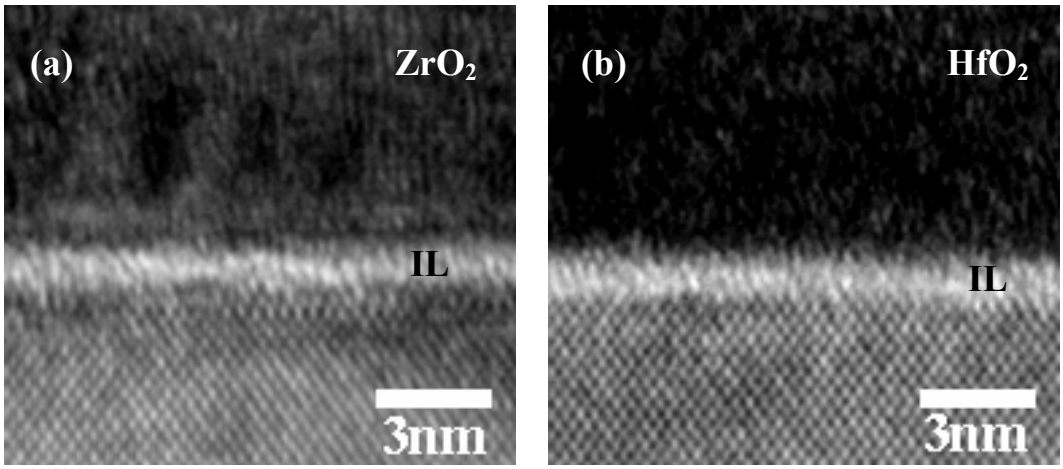

Figure 5.16: Cross-sectional HR-TEM images of (a) thick-ZrO_2 and (b) thick-HfO_2 dielectrics with Ti metal electrode after a forming gas annealing (300°C, 30min).

to reaction (5.1). However, in the case presented here, the decomposition of SiO_2 and dissolution of oxygen requires oxygen ion diffusion across a high-κ metal oxide layer that is interposed between the Ti and the oxidized Si surface. This process is depicted schematically in Figure 5.15.

Oxygen ion diffusion in metal oxides, such as ZrO_2 and HfO_2, is typically mediated by oxygen vacancies. However, grain boundary diffusion may be significant in fine-grained polycrystalline samples such as our ALD-ZrO_2 thin films.[20] Diffusion of oxygen along percolative paths of high excess volume is also possible in thin amorphous films, such as the ALD-HfO_2 films used in our experiments. Although the experimental results obtained to date do not allow us to quantify the relative contributions of these oxygen transport mechanisms to the process of interface layer decomposition, it is evident that the kinetics of oxygen diffusion is quite rapid, even at temperatures near 300 K. For a maximum diffusion time on the order of minutes and a metal oxide film thickness of 4 nm, an oxygen diffusivity across the metal oxide films of order 10^{-14}–10^{-16} cm^2/s can be estimated for the ALD-ZrO_2 and ALD-HfO_2 films. If oxygen transport is mediated by vacancy counter-diffusion (from the Ti/metal oxide interface to the metal oxide/interface layer interface), then the diffusivity of oxygen vacancies would have to be

of similar magnitude. To the authors' knowledge, the oxygen vacancy diffusivity in amorphous HfO_2 and undoped tetragonal ZrO_2 has not yet been measured; however, data from yttria-stabilized cubic zirconia is available.[21,22] When extrapolated to 300 K, these reported results are consistent with an oxygen vacancy diffusivity of order 10^{-16} cm^2/s, close to the lower bound of the range of diffusivities estimated from our own observations.

TEM studies of otherwise-identical ALD films of 12 – 15 nm thickness with Ti electrodes indicated that a low-atomic number amorphous layer of ~ 0.8 nm thickness (half of the original chemical oxide thickness) was present at the high-κ/Si interface after the 300°C forming gas anneal as shown in Figure 5.16. These observations indicate that the rate of interface layer decomposition can be slowed appreciably by increasing the distance over which oxygen must diffuse to reach the Ti overlayer.

In addition to decomposition of the SiO_2 interface layer, dissolution of oxygen into the Ti electrode layer will remove oxygen from the interposed metal oxide film. Such oxygen loss may contribute fixed charge and bulk trap states to the dielectric. Zirconia and structurally-similar metal oxides are prone to oxygen deficiency through formation of oxygen vacancies under conditions of low oxygen activity. Insight into possible electrode-induced reduction of the high-κ film can be obtained by careful analysis of the electrical data. Oxygen vacancies are generally donor-type charged defects in metal oxides and would be expected to produce positive fixed charge in oxygen-deficient high-κ films. Because the reduction reactions which produce oxygen vacancies also produce electrons as charge-compensating species,[23] metal oxide films with substantial oxygen deficiency are also found to exhibit a significant frequency dispersion and large loss-factor resulting from their enhanced electronic conductivity.[24]

The fixed charge present in the dielectric stacks can be estimated from the flat band voltage measured by CV analysis. The results obtained from both Ti-electroded and Pt-electroded high-κ capacitors are consistent with a net positive fixed charge density of $\sim 10^{12}$ cm^{-2}. This indicates that the presence of an oxygen-gettering Ti overlayer does not lead to a significant increase in the dielectric fixed charge over that present with less-

reactive, Pt-electrodes. The measured fixed charge areal density is consistent with a volumetric charge density of 10^{18} – 10^{19} cm^{-3} in the ALD-HfO_2 and ALD-ZrO_2, independent of electrode material.

Studies of the effect of oxygen stoichiometry on the behavior of high-κ metal oxide films grown by UV-O_3 oxidation of metal films by Ramanathan *et al.*[24] showed that MOS capacitor measurements will detect high leakage current densities and a pronounced frequency dispersion of the dielectric properties when significant oxygen deficiency (~ 10 atomic %) exists. The leakage current densities obtained in the present experiments on Ti-electroded metal oxide dielectrics are very low for the measured EOT, and minimal frequency dispersion was detected after correction of the CV data for the series resistance of the Si substrate (not shown).[25] The slight dispersion is almost identical in magnitude to that observed for identically-processed low-leakage Ti-electroded SiO_2 capacitors with 10 nm dielectric thickness, suggesting that is a property of the Ti-O electrode layer rather than the dielectric. It can be concluded, therefore, that any oxygen deficiency induced in the metal oxide dielectrics by their equilibration with the Ti electrode layer is too small to be detected in the present capacitor measurements.

As discussed in the Section 5.2.1, with the complete removal of the interfacial oxide, the EOT of Ti-electroded samples should decrease from the value measured for Pt-electroded devices by a factor of approximately 1.5 nm. However, the decrease of EOT obtained from CV curves was only 0.4 ~ 0.5 nm for both high-κ films. This more modest, but still significant, EOT reduction may result from several different factors. If all of the Si present in the initial interface oxide is epitaxially regrown onto the surface of the underlying Si substrate during interface layer decomposition, then it is reasonable to expect the formation of ~ 1.2 nm of undoped Si at the wafer which could contribute an EOT of ~ 0.4 nm to the interface layer-free gate stack. There remains another ~ 0.5 nm of expected EOT reduction that cannot be accounted for by the dissociation process of interface oxide alone. As shown in the HR-TEM images in Section 5.2.2, a brighter image contrast was observed in the Ti-electroded high-κ films. It is possible that a chemical change in the high-κ dielectric occurred during the dissociation of the

interfacial oxide causing a small reduction of the dielectric constant and accounting for the remaining EOT difference of ~ 0.5 nm. Possible chemical changes in the high-κ dielectric can arise from either reduction of the metal oxide film or incorporation of Si atoms liberated by the dissociation of interfacial oxide. More work is needed to fully understand the detailed mechanisms of Ti electrode-induced interface layer decomposition and to improve the efficiency of the EOT reduction through optimized post-deposition treatments.

5.3 Summary

Various alloy and nanolaminate structures composed of ALD-grown ZrO_2 and HfO_2 were fabricated and characterized. A relatively homogeneous alloy structure composed of ALD-grown layers of thickness similar to the lattice parameter of ZrO_2 and HfO_2 resulted in either completely amorphous films or an ensemble of crystalline seeds (tetragonal phase) in an amorphous matrix, depending on the identity of the starting layer. The effect of the microstructure of the starting layer material becomes increasingly important as the individual layer thicknesses increase. Nanolaminates in which the initial layer was amorphous HfO_2 became fully crystalline and had a relatively large grain size (mixed tetragonal and monoclinic phases) as a result of the templating effect of the overlying crystalline ZrO_2 layer. By changing the stacking sequences, nanolaminates having smaller grain sizes and larger surface roughness were obtained as a result of within-in grain epitaxial growth during the ALD process.

A promising new approach for engineering the thickness of the SiO_2-based interface layer between metal oxide films and silicon *after* deposition of the metal oxide layer was demonstrated. We have shown that a Ti overlayer, which exhibits a very high oxygen solubility, can effectively getter oxygen from the interface layer, thus decomposing SiO_2 and reducing the interface layer thickness in a controllable fashion. The kinetics of the process appears to be limited by the oxygen permeability of the

interposed metal oxide film. Electrical characteristics of low-EOT MOS capacitors fabricated in this manner are very promising. Negligible capacitance-voltage hysteresis and dispersion are observed and the leakage current densities are very low for the measured EOT values. This method for engineering the thickness of the interface layer between silicon and metal oxide films may be extendable to other materials systems and applications beyond MOS transistors.

References

[1] K. Kukli, J. Ihanus, M. Ritala, and M. Leskela, Appl. Phys. Lett. **68**, 3737 (1996).

[2] K. Kukli, J. Ihanus, M. Ritala, and M. Leskela, J. Electrochem. Soc. **144**, 300 (1997).

[3] H. Zhang and R. Solanki, J. Electrochem. Soc. **148**, F63 (2001).

[4] M.-H. Cho, Y. S. Roh, C. N. Whang, K. Jeong, H. J. Choi, S. W. Nam, D.-H. Ko, J. H. Lee, N. I. Lee, and K. Fujihara, Appl. Phys. Lett. **81**, 1071 (2002).

[5] H. Kim, P.C. McIntyre, and K. C. Saraswat, J. Mat. Res. **19**, 643 (2004).

[6] R. Ruh, H. J. Garrett, R. F. Domagala, and N. M. Tallan, J. Amer. Ceram. Soc. **51**, 23 (1968).

[7] J. M. Howard, V. Craciun, E. Essary, and R. K. Singh, Appl. Phys. Lett. **81**, 3431 (2002).

[8] M. Leskela and M. Ritala, Thin Solid Films **409**, 138 (2002).

[9] M. L. Green, M.-Y. Ho, B. Busch, G. D. Wilk, T. Sorsch, T. Conard, B. Brijs, W. Vandervorst, P. I. Räisänen, D. Muller, M. Bude, and J. Grazul, J. Appl. Phys. **92**, 7169 (2002).

[10] E. H. Nicollian and J. R. Brews, *MOS(Metal Oxide Semiconductor) Physics and Technology* (Wiley and Sons, New Jersey, 2003).

[11] G. Timp, K. K. Bourdelle, J. E. Bower, F. H. Baumann, T. Boone, R. Cirelli, K. Evans-Lutterodt, J. Garno, A. Ghetti, H. Gossmann, M. Green, D. Jacobson, Y. Kim, R. Kleiman, F. Klemens, A. Kornlit, C. Lochstampfor, W. Mansfield, S. Moccio, D. A. Muller, I. E. Ocola, M. I. O'Malley, J. Rosamilia, J. Sapjeta, P. Silverman, T. Sorsch, D. M. Tennant, W. Timp, B. E. Weir, Tech. Dig. – Int. Electron Devices Meet. **1998**, 615 (1998).

[12] C. H. P. Lupis, *Chemical Thermodynamics of Materials* (New York, North-Holland, 1983).

[13] S. Stemmer, H. Kim, C. Chui, P. C. McIntyre, and K. C. Saraswat (unpublished work).

[14] A. C. Diebold, A. Venables, Y. Chabal, D. Muller, M. Weldon, E. Garfunkel, Materials Science in Semiconductor Processing **2**, 103 (1999).

[15] I. Barin and O. Knacke, *Thermochemical Properties of Inorganic Substances* (Springer, Berlin, 1977).

[16] W. E. Wang and Y. S. Kim, J. Nuc. Mat. **270**, 242 (1999); K. L. Komarek, M. Silver, in *Thermodynamics of Nuclear Materials* (IAEA, Vienna, 1962), p. 749.

[17] L. Murray and H. A. Wriedt, *Phase Diagrams of Binary Titanium Alloys* (ASM International, Ohio, 1987)

[18] M. Liehr, F. K. LeGoues, G. W. Rubloff, and P. S. Ho, J. Vac. Sci. Technol. A **3**, 983 (1985).

[19] J. C. Barbour, A. E. M. J. Fischer, and J. F. van der Veen, J. Appl. Phys. **62**, 2582 (1987).

[20] U. Brossmann, R. Wurschum, U. Sodervall, and H. E. Schaefer, J. Appl. Phys. **85**, 7646 (1999).

[21] S. F. Palguev V. K. Gilderman, and A. D. Neujmin, J. Electrochem, Soc. **122**, 745 (1975).

[22] K. Sasaki and J. Maier, Solid State Ion. Diffus. React. **134**, 303 (2000).

[23] F. A. Kröger and H. J. Vink, Solid State Phys-Adv Res Appl **3**, 307 (1956).

[24] S. Ramanathan, D. A. Muller, G. D. Wilk, C. M. Park, and P. C. McIntyre, Appl. Phys. Lett. **79**, 3311 (2001).

[25] K. J. Yang and C. M. Hu, IEEE Trans. Electron Devices **46**, 1500 (1999)

Future Work

1 ALD-ZrO_2 and HfO_2 using different precursor systems

Although the ALD-grown metal oxides using Cl-based precursors showed excellent electrical properties, there are many concerns about the possible Cl contamination and handling problems associated with solid precursors. Therefore, new precursor systems using liquid metal-organic precursors are widely investigated to improve the dielectric properties of high-κ metal oxides. Still there is a problem with the poor electrical properties caused by the carbon contamination, and significant improvement could be achieved by using plasma-assisted ALD process. Thus, there are many research areas to be investigated and developed. Especially, the in-situ gate stack formation with ALD-grown metal electrode is an interesting topic for the future generation of MOS transistors.

2 High dielectric constant dielectrics on Ge substrate

It is of great interest to grow high-κ metal oxides on Ge substrates to improve the transistor speed. Although an extensive characterization and evaluation of Ge MOS devices with various surface passivation methods were performed in this thesis, a detailed understanding of the interface structures and the subsequent electrical properties was not

accomplished yet. Firstly, it would be most important to demonstrate the superiority of Ge-MOS transistors compared to the conventional Si-based transistors using a recently developed surface nitridation technique. Secondly, the understanding of the CV and IV characteristics, focusing on the electrical traps and interface states is also crucial for future development. Lastly, further optimization of surface treatments or development of new passivation methodology, such as the remote plasma nitridation would be needed.

3 Interface engineering using a reactive metal electrode

A promising new interface engineering technique using a reactive metal electrode was demonstrated in this thesis. The removal of an interfacial layer having a low dielectric constant has been demonstrated using a highly reactive metal electrode having high oxygen solubility. Although a significant decrease of EOT was verified, the additional expected decrease was not identified. Further characterization of the whole gate stack is needed to understand the detailed mechanism for the electrical properties. In terms of the practical point-of-view, a new fabrication process needs to be developed since Ti does not have a suitable workfunction for both NMOS and PMOS devices. One possible way would be to remove a Ti metal electrode via wet etching or dry etching technique after removal of interface layer, and to use other suitable metal as a gate electrode. Lastly, reliability of the gate dielectric and device characteristics should be confirmed in order for it to be included in CMOS transistors.

4 New applications of ALD for future nano-devices

Several possible applications of ALD-grown high-κ gate dielectrics to the new nano-scale devices and processes, such as the carbon nanotube transistors, the Ge-nanowire transistors, the metal-insulator-metal capacitors, and the area-selective ALD

using a self-assembled monolayer, were demonstrated in addition to the ones described in this thesis. More detailed understanding of the deposition kinetics and the properties on different surface conditions and chemical species are not fully understood and needs more optimization processes. In the case of area-selective ALD process, the integration process of the whole gate stack using the selectively deposited gate dielectric and metal electrode needs to be demonstrated.