HETEROEPITAXIAL GROWTH
OF RELAXED GERMANIUM ON SILICON

A DISSERTATION
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IN PARTIAL FULFILLMENT OF THE REQUIRMENTS
FOR THE DEGREE OF
DOCTOR OF PHILOSPHY

Ammar Nayfeh
June 2006

I certify that I have read the dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for a degree of Doctor of Philosophy.

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Paul McIntyre

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Stanford University, 2006

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Abstract

Germanium has a many advantages to silicon as a semiconductor material. Most importantly, Ge has a larger lattice mobility (hole and electron) compared to Si. The larger mobility provides a higher source injection velocity, which translates into higher drive current and smaller gate delay. In addition, the near-infrared photodetection and compatibility with Si technology of Ge-based materials, allow simultaneous fabrication of photodetectors and Si CMOS receiver circuits in a monolithically integrated fashion. The main disadvantage is that germanium based oxides are not stable and but rather soluble in water. But the inevitable shift to high-κ/metal gate has made Ge a serious option nevertheless. In order for the semiconductor industry to take advantage of the properties of Ge, heterogeneous integration of Ge and Si must be possible since using bulk Ge is not viable. However, Ge growth on Si is hampered by the large lattice mismatch (4%) between Ge and Si which results in growth that is dominated by "islanding" and misfit dislocations. The following thesis, investigates both the islanding and dislocation density issues

associated with this problem. A 90% reduction of surface roughness by hydrogen annealing is demonstrated accompanied with a theoretical model to explain these results. Using multi-steps of growth and hydrogen annealing, Ge layers on Si were achieved with dislocation density as low as $1x10^{7}cm^{-2}$ and R_{rms} surface roughness of 2.5nm. The method was patented and named, Multiple Hydrogen Annealing for Heteroexpitaxy" (MHAH). A complete experimentally based theoretical model is provided that explains these results. In addition, MOSCAPS, a pMOS transistor, and a MSM photodetector are fabricated on the MHAH-Ge substrates. Also high-κ/metal gate compatibility is demonstrated on MHAH-Ge. The electrical results indicate that MHAH-Ge approaches the electrical quality of bulk Ge. These results point to a promising step in achieving heterogeneous integration of a high mobility pure Ge channel transistor directly on Si using high-κ/metal gate which may be used in future technology nodes. Finally, MHAH-Ge can be used for fabrication of Germanium on Insulator (GOI) needed for very high performance Ge based transistors.

I dedicate this thesis

to my beautiful and loving wife,

Lama

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Chapter 1

Introduction

1.0 Motivation

The search for high mobility semiconductor materials, to help continue traditional silicon scaling, has lead researchers to investigate germanium. Germanium is ironically a step back from a historical perspective. Ge was once believed to be main semiconductor of choice, but as will be discussed in detail, Si became and remains today the dominant semiconductor. Yet recently, Ge has been given new life for possible inclusion in the Si CMOS transistor scaling path. However the idea of using bulk Ge is not realistic for the semiconductor industry due to many challenges. As a result, for Ge to be included in this scaling path, it is pivotal to develop new methods for heteroepitaxial Ge technology because Ge growth on Si is hampered by the large 4.2% lattice mismatch. The large mismatch results in growth that dominated by "islanding" and misfit dislocations, rendering the Ge layers obsolete. Consequently

the challenge for researchers is to overcome the mismatch and grow high quality Ge layers on Si that are not obsolete but rather suitable for possible CMOS integration.

1.1 Organization

Chapter 2 will focus solely on the main challenges of germanium on silicon growth. It will introduce the growth mechanism and two main consequences of the 4.2% lattice mismatch; islanding and dislocation formation. The physics of the islanding mechanism that leads to surface roughness and the mechanisms of dislocation formation will be discussed in detail.

Chapter 3 will focus on the surface roughness reduction mechanism by hydrogen annealing. The chapter will provide an overview of chemical vapor deposition (CVD) and the epitaxial growth process. Following the background, the hydrogen annealing experiment and results will be discussed. The characterization was done by Atomic Force Microscopy (AFM), and Scanning Electron Microscopy (SEM). Finally, a complete experimentally based theoretical model will be introduced to explain the surface roughness reduction.

Chapter 4 covers the entire germanium growth method developed that utilizes multiple steps of growth and hydrogen annealing and was thus named "Multiple Hydrogen Annealing for Heteroepitaxy, MHAH". The chapter will begin with a historical time-line of research in the area of germanium on silicon heteroepitaxy. After the background, the MHAH-Ge growth experiment and characterization results will be provided. The characterization was done by Transmission Electron Microscopy

(TEM), Atomic Force Microscopy (AFM), and Etch Pit Density (EPD). Finally, a complete experimentally based theoretical model for the MHAH method will be described.

Chapter 5 focuses on the electrical characterization of the layers. The chapter begins with MOS capacitor fabrication and CV characteristics obtained. Next the fabrication steps of the MHAH-Ge pMOS transistor and the electrical results obtained will be discussed. Following this, high-κ metal gate compatibility is demonstrated. Finally, fabrication of a Metal Semiconductor Metal (MSM) photodetector is described and the optical results obtained.

Finally, Chapter 6 summarizes the contributions of this work and provides recommendations for future research topics.

CHAPTER 2

Challenges in Germanium-Silicon Heteroepitaxy

2.0 Abstract

One of the most difficult and continuing research challenges in the semiconductor industry is the ability to grow high quality films using lattice mismatched materials, called *heteroepitaxy*. The germanium/silicon system has been extensively studied because of the many potential applications of Ge and advantages over Si. Below a critical thickness, the lattice-mismatch between Ge and Si causes the grown film to match the lattice constant of the underlying Si substrate and hence strain the layer. However, above a critical thickness, it is energetically favorable for the layer to create dislocations to relieve this strain. In addition, due to the lattice mismatch associated with the system, an alternative mechanism of strain relaxation,

islanding, often leads to rough layers. The following chapter will detail the main challenges of the Ge/Si heteroepitaxial system.

2.1 Why Germanium?

With continued scaling of Si CMOS technology, it is imperative to begin researching new materials, such as germanium. Before understanding the main challenges of germanium/silicon heteroepitaxy, it is important to understand why germanium is being considered as a possible semiconductor material. Germanium has many advantageous properties compared to silicon. Ge has higher bulk mobility for both electrons and holes. The lattice electron mobility is μ_n = 1417 cm^2/V-sec for Si and 3900 cm^2/V-sec for Ge. The lattice hole mobility is μ_p = 471 cm^2/V-sec for Si and 1900 for Ge. As a result, there is a 2.75 times increase in bulk electron mobility, and 4 times increase in bulk hole mobility in germanium as compared to silicon [1]. Table 2.1 shows the enhancement of the lattice mobility of germanium for both electrons and holes. This increase in bulk mobility should ideally correspond to an increase in surface mobility and an ultimate increase in the transistor performance. In addition to the increase in mobility, germanium's electron and hole mobility's are more symmetric compared to silicon. This will lead to smaller area pMOS devices in a CMOS inverter cell.

	Silicon	**Germanium**	**Mobility Enhancement**
Electron Mobility, μ_n	1417 cm^2/V-sec	3900 cm^2/V-sec	**2.75** ×
Hole Mobility, μ_p	471 cm^2/V-sec	1900 cm^2/V-sec	**4** ×

Table 2.1: Lattice mobility enhancement of germanium compared to silicon.

It is interesting to compare the two systems of Ge and Si in the ballistic limit. For ultra short channel devices in this limit, an electron travels from source to drain independent of scattering and thus I_{dsat} is no longer governed by V_{sat} [2-4]. Thus, during scaling, the I_{dsat} limit is governed by the thermal injection velocity (v_{inj}) [2-4]. Figure 2.1 is a plot of drift velocity versus electric field for various semiconductors. Figure 2.2 shows the band diagram at the source side of a standard MOSFET.

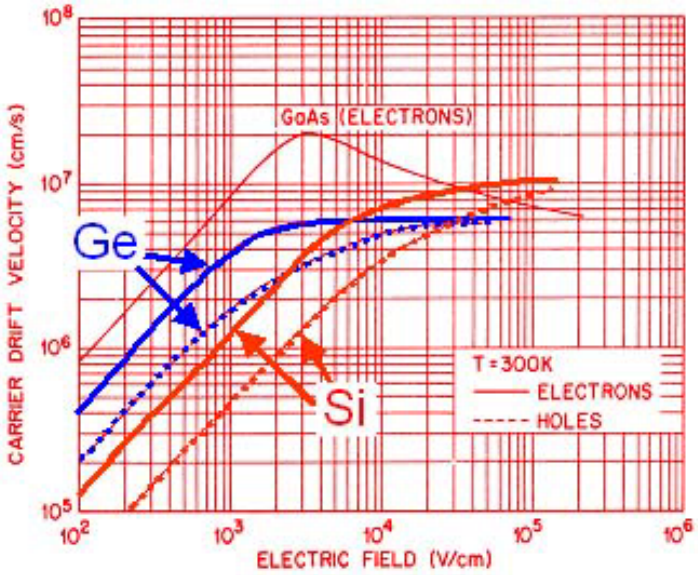


Figure 2.1: Carrier drift velocity (cm/s) versus electric field (V/cm) [1].

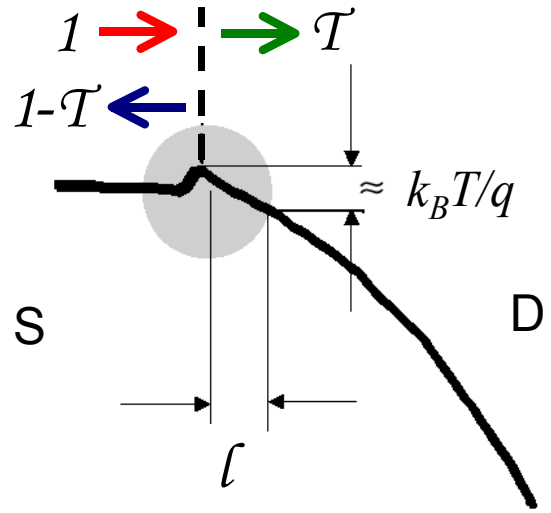


Figure 2.2: Band-Diagram from source to drain in the ballistic limit.

The drive of the device can now be calculated using the following set of equations derived from the band diagram above [4]. (More details of the derivation are found in the references).

$$\mathcal{T} = \frac{\lambda_0}{l + \lambda_0} \qquad 2.1$$

$$\lambda_0 \propto \tau_0$$

$$\propto \mu_{low-field}$$

$$\propto v_{inj}$$

$$\Downarrow$$

$$I_{DS} = W \times Q_{inv} \times v_{inj} \qquad 2.2$$

$$\Downarrow$$

$$\frac{C_{LOAD} V_{DD}}{I_{DS}} = \frac{L_{gate} \times V_{DD}}{(V_{DD} - V_T) \times v_{inj}} \qquad 2.3$$

In these equations λ is the reflection coefficient, τ is the mean time between scattering events, ν is the injection velocity, μ is mobility and Q_{inv} is the inversion charge density. From the equations above the effect of higher mobility on the drive and delay can be determined. Equation 2.1 indicates that the mobility and injection velocity are directly proportional [4]. Thus, to first order in the ballistic limit, a germanium device will have a large source injection velocity compared to a silicon device due to its higher mobility. Consequently, *Ge based ballistic devices will have higher source-drain current (performance) and a lower gate delay than Si based ballistic devices.* A recent PhD thesis written by a member of our group goes in much more detail about the advantages of Ge CMOS [5].

Another advantage of using germanium is its smaller band-gap, being around 0.6eV compared to 1.2eV for Si. Smaller band-gap leads to smaller threshold voltage hence to longer V_{dd} scaling, which is a major limitation in the scaling of Si devices. Also, the smaller band gap will lead to smaller contact resistance which will help the drive current of a MOSFET. However, one might point out that smaller band gap causes higher p-n junction leakage current and also band to band tunneling. Suppression of these leakage paths requires complicated transistor structures which are not the primary focus of this thesis.

In addition to the electrical advantages of Ge, there are material and process advantages. Firstly, Ge can be processed at very low temperatures and is thus a very suitable candidate for 3D integration. Secondly, there exists a lattice match between

Ge and GaAs, and thus high quality GaAs layer can be grown on Ge. This could lead to using Ge as a buffer layer to grow GaAs on Si.

2.1.1 Germanium as an Optical Material

One major advantage in using germanium is the potential applications in the area of optics. Si photodetectors are not efficient at wavelengths (1.3-1.55 μm) for medium- and long-haul optical fiber communications due to the inherent large bandgap of Si [6]. Germanium has been emerging as a viable candidate for integration with Si for low-cost transceivers to overcome the spectral limit. Figure 2.3 is the absorption coefficient versus photon energy highlighting the role Ge can play for telecom standards. Historically, III-V semiconductors were used to fabricate efficient photodetectors. Hybrid integration of III-V semiconductors on Si is costly and lacks adequate compatibility with Si process technology [6]. Due to compatibility of Ge with Si CMOS technology, researchers have focused on integration of SiGe and Ge photodetectors on Si [7-9]. Among photodetector structures, metal-semiconductor-metal photodetectors (MSM-PDs) have been attractive for receiver optoelectronic integrated circuits due to large device bandwidth, low capacitance and ease of integration with preamplifier circuits.

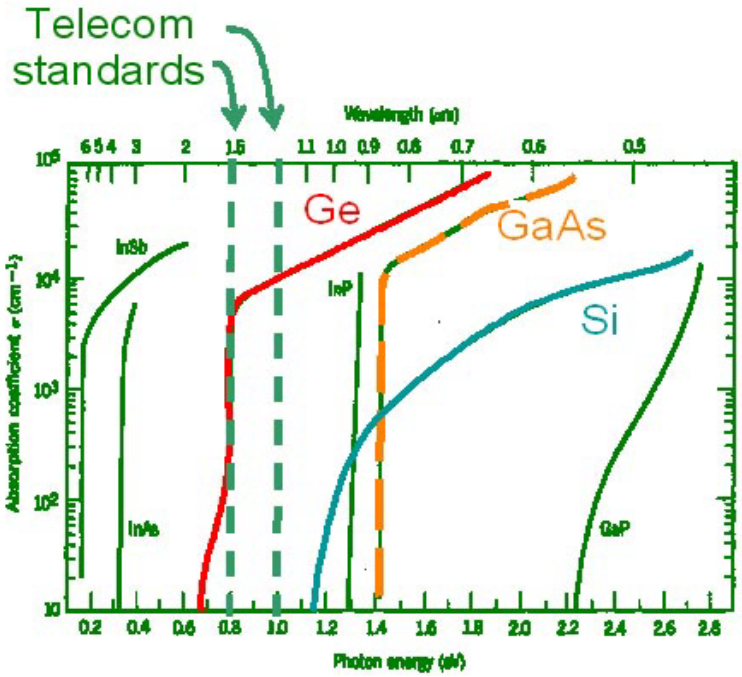


Figure 2.3: Absorption coefficient versus photon energy [1].

Relatively higher dark current (I_{dark}) associated with MSM-PDs can be suppressed using the incorporation of a wide bandgap layer [10] or asymmetric barrier electrode schemes [11]. Chapter 5 will highlight fabrication of MSM-PDs on our germanium on silicon layers.

2.1.2 Why Silicon?

Despite the advantages of germanium we discussed ***silicon remains the dominant semiconductor of the industry.*** In early development, the chemistry of

germanium was a critical factor despite the fact that Si was viewed desirable due to its wider band gap and its natural availability. For instance, the first transistor fabricated was in germanium [12-14] mostly due to the ease of Ge purification compared to Si, which has unavoidable oxygen and other contaminations resulting from the reaction between Si melt and quartz crucible. However, the chemistry of Ge oxide is a disadvantage. In order to fabricate a Metal Insulator Semiconductor (MIS) transistor, growth of a high quality stable oxide is a prerequisite. Unfortunately germanium oxides, GeO and GeO_2, are unstable and soluble in water, and thus cannot survive a fabrication process. On the other hand, thermally grown silicon dioxide, SiO_2, is stable and can be grown with very high quality. ***As a result, SiO_2 is the most important reason why Si dominates the semiconductor industry***. The first transistor fabricated using Ge was a discrete point contact transistor, and bipolar junction transistors have also been fabricated; however, a Ge field effect transistor has yet to be productized.

With the continued scaling of the gate oxide thickness to improve the current drive capability we are reaching a limit in which short channel effects become more dominant. The current leakage at the gate, I_g, has now become a significant factor [15]. The gate region of a MOSFET can be modeled as a capacitor with thickness t_{ox} and dielectric constant (κ) being material dependent. So the capacitance in mathematical form is,

$$C = \frac{\kappa \varepsilon_o}{t_{ox}} \qquad (2.4)$$

From this equation there are only two ways to increase gate control of a MOSFET, either decrease the t_{ox} as has been the case with SiO_2, or use a different material with a higher κ. κ is material dependent and typically ranges from 3-30 [16]. Until recently all the high-κ research has be focused on Si compatibility. However, there is now a push to try different semiconductor compatibility with high-κ. Our group, a few years back, published the first such work on high- κ on germanium [17]. Advanced semiconductor research has lead to solutions to some of the key issues. The dielectric issue can be solved by going to high-κ or by using, for research purposes, a stable germanium oxynitride. More details on germanium oxynitride will be described in chapter five, when the electrical devices fabricated are discussed.

In addition to fundamental problems there are some technology issues with germanium. One is that cost of germanium wafers is very high and the quality is sub-par due to the limited demand. Also, processing germanium can be a challenge due to the brittle nature of the wafer. All of these factors lead us to conclude that Si will continue as the main semiconductor of the CMOS industry. ***In order for Ge to be used in the semiconductor industry however, heteroepitaxial integration of Ge on Si is necessary.*** With this technology available it will open the door to many applications. Table 2.2 is a list of some of the potential applications. The next section will go over the main challenges of germanium-silicon heteroepitaxy.

Potential of Applications of Heteroepitaxial Germanium on Si Layers
• ***Ge CMOS*** – **Higher Mobility for High Performance** – **Low Temperature Processing for 3D applications**
• ***Germanium on Insulator (GOI)*** – **Alleviate high junction leakage** – **Higher Performance**
• ***Ge Photodetector (MSM)*** – **Optical Interconnects**
• ***Integration of Ge/Si/GaAs*** – **CMOS: Ge pMOS and Si nMOS** – **GaAs Growth on Ge for Laser's and LED's**
• ***GaAs CMOS*** – **Very High Mobility**
• ***Nanotechnology:*** – ***Ge nano-wire growth*** – ***Ge nano-particle fabrication***

Table 2.2: Potential applications of heteroepitaxial Ge technology.

2.2 Challenges

2.2.0 Background

If the lattice constants are the same, one can ideally grow very high quality films psuedomorphically, *without dislocations*. For example if one grows epitaxial-Si on an underlying Si substrate, the resulting growth will be high-quality single crystal

Si without dislocations. However, in order to grow two different materials with the same high quality, the lattice constant of the grown film must match the lattice constant of the underlying substrate [1]. By nature, there are different materials that have the same lattice constants, for example, GaAs/AlAs and Ge/GaAs. In those cases, high quality layers can be grown. In addition, in some cases one can match the lattice constants by using ternary alloys. Since GaAs and AlAs have the same lattice constant then the ternary alloy $Al_xGa_{(1-x)}As$ has the same lattice constant over the entire range of x. Thus one can choose the desired x, (or bandgap) then grow on a matched GaAs substrate [1].

2.2.1 Ge/Si: 4.2% Lattice Mismatch

In addition to the widespread use of lattice-matched epitaxial layers, advanced epitaxial growth techniques described in the following sections allow the growth of very thin (~100A) layers of lattice-mismatched crystals. If the mismatch is only a few percent and the layer is thin, the epitaxial layer growth with a lattice constant in compliance with that of the seed crystal. The resulting layer is in compression or tension along the surface plan as its lattice constant adapts to the seed crystal. Such a layer is called *pseudomorphic* because it is not lattice-matched to the substrate without strain. However if the epitaxial layer exceeds a critical thickness, t_c, which depends on the lattice mismatch, the strain energy leads to formation of defects called *misfit dislocations.* In our research, we want to grow high quality germanium layers on

silicon for the reasons specified in section 2.1. However, germaniums lattice constant is 5.6575Å while silicon is 5.4307 Å [1]. Thus the percent difference is

$$(5.6575Å - 5.4307Å)/ 5.4307Å * 100 = 4.1763\% \quad (2.5)$$

Lattice Mismatch between Germanium and Silicon

This difference is considered very large in the area of semiconductor heteroepitaxy and will have a negative impact on the layer quality. As one starts to grow Ge on Si, the new Ge layer will conform to the lattice spacing of the Si substrate. The Ge layer is now compressively strained as the lattice constant is reduced. So below a certain thickness, one can grow defect-free compressively stained Ge on Si. This thickness has been shown to be around 4-10 nm [18]. As one continues to grow thicker layers, it is energetically favorable to relieve the strain by forming dislocations at the Ge/Si interface [18]. In addition, the islanding can occur as an additional means of reducing the elastic strain energy of the film [18]. This leads to rough surfaces unsuitable for device applications. The next sections will detail the process of islanding and dislocations in germanium on silicon heteroepitaxy.

2.2 From Islanding to Surface Roughness

2.2.0 Three Growth Modes

In order to better understand the growth mechanism of germanium on silicon it is important to understand the physics of the process that governs nucleation and

growth. We can start by thinking about the classic problem: droplet of radius r, in contact with vapor. Figure 2.4 shows a 2D image of this situation [19].

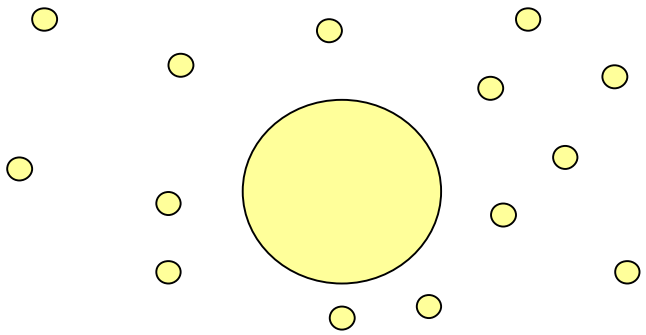


Figure 2.4: Classic problem of a droplet in contact with vapor

This system can be described by solving for the change in free energy,

$$\Delta G = \frac{4}{3}\pi r^3 \Delta G_V + 4\pi r^2 \gamma \qquad (2.6)$$

where ΔG_v is the change in free energy per unit volume and γ is the free energy change per unit surface [19]. ΔG_v can be given by

$$\Delta G_V = \frac{kT}{\Omega}\ln\left(\frac{P_V}{P_S}\right) = \frac{kT}{\Omega}\ln(1+S), \qquad (2.7)$$

$$\text{where } S = \frac{P_V - P_S}{P_S} \text{ is defined as the Supersaturation}$$

And,

Ω = atomic volume (volume per atom)
P_V = actual pressure in gas phase
P_S = Saturated vapor pressure at equilibrium
$P > P_S \rightarrow$ Supersaturated
$P = P_S \rightarrow$ Equilibrium
$P > P_S \rightarrow$ Undersaturated

Solving for ΔG on a surface shows the presence of both surface and line tension. The presence of surface tension always produces an activation barrier to nucleation of condensed phases. Figure 2.6 is a plot of E, the activation energy to nucleation, versus nucleation size. E^* denotes the activation barrier to nucleation.

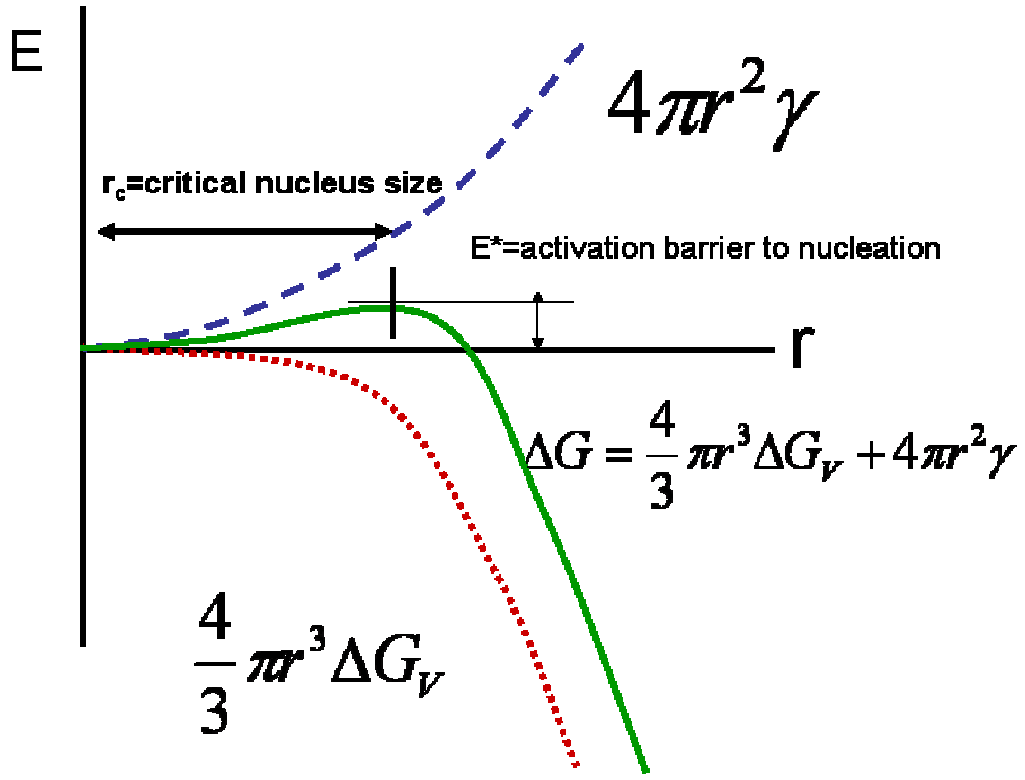


Figure 1.5: E (activation energy to nucleation) vs. nucleation size (r). An activation barrier E^* is evident.

As a result of the activation barrier, the three growth modes exist. These are island growth mode or what is called Volmer-Weber growth (VW), layer growth mode or Frank Van der Merwe (FVM), and Stanski-Krastanov (SK) growth (a combination of layer and island growth) [19]. The following is a brief description of the island growth, and the layer growth mode. SK growth will be described in greater detail in the next section, as this mode describes the germanium/silicon system. The following equation describes the change in free energy ΔG during nucleation of heterogeneous systems (B nucleation on A).

$$\Delta G = \gamma_{BV} - \gamma_{AV} + \gamma_{AB} \tag{2.8}$$

Where γ_{AV} is the change in surface energy between substrate (A) and total volume (V), γ_{BV} is the change in surface energy between growth material (B) and total volume(V), and γ_{BV} is the change in free energy between growth material (B) and substrate (A).

Island Growth Mode

In the island growth mode, the smallest stable clusters nucleate on the substrate and grow in three dimensions to form islands. This happens when the deposited atoms are more strongly bound to each other than to the substrate. This growth mode is typical of metal on insulators. Figure 2.6 shows a schematic cross section of the island growth mode [20]. In this mode the growing layer wants to minimize interface energy and its own surface energy so the layer "balls up" on the surface. Mathematically

speaking from equation 2.8 the following condition must hold true must hold true for islanding growth to take place.

$$\gamma_{AV} < \gamma_{BV} + \gamma_{AB} \qquad (2.9)$$

Using 2.8 and 2.9, ΔG will be >0 and thus the system wants to minimize the surface energy.

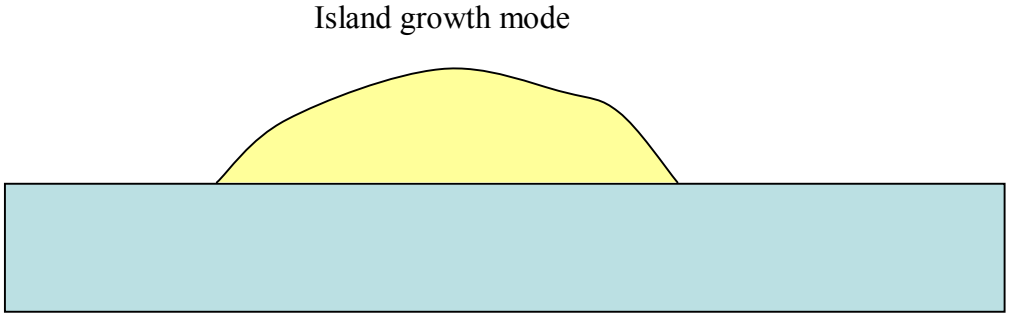


Figure 2.6: Cross section of islanding growth mode or sometimes called Volmer-Weber (VW) growth.

Layer Growth Mode

In the layer growth mode, the smallest stable clusters grow in two dimensions, resulting in the formation of planar sheets. In this growth mode, the atoms are more strongly bound to the substrate than to each other. An example of this growth mode is single crystal epitaxial growth of semiconductor films. The growing layer reduces the

surface energy, and wets the surface completely. The result is smooth layer on layer growth. Figure 2.7 is a cross section of layer growth showing the change in free energy condition [20]. Mathematically speaking from equation 2.8 the following condition must hold true must hold true for islanding growth to take place.

$$\gamma_{AV} > \gamma_{BV} + \gamma_{AB} \tag{2.10}$$

Using 2.8 and 2.10, ΔG will be <0 and thus the system wants to increase its surface energy.

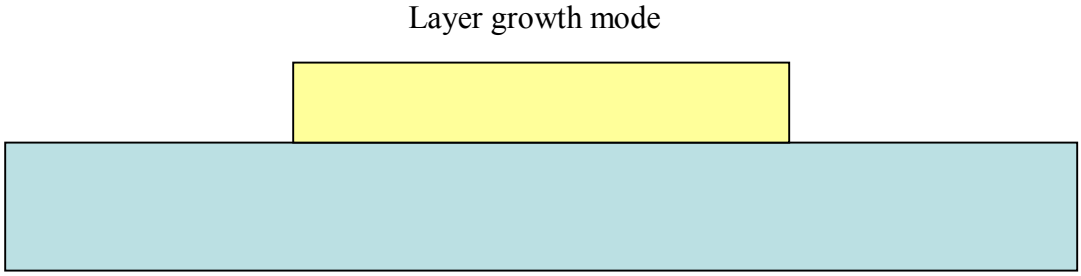


Figure 2.7: Cross section image of layer growth

2.2.1 Stranski – Krastanov (SK)

If the balance of forces changes during the growth, the first few layers will comprise a continuous, smooth film that usually has properties that differ from the bulk. The balance of forces, (equations 2.8-2.10), will change during the growth if the materials have a large lattice mismatch and the strain associated. This is due to the

influences of the surface and the interfaces and also the film structure, determined by the initial condensation process. The film growth process involves the processes of initial nucleation and subsequent film growth. Nucleation refers to the earliest steps of film growth where a sufficient number of vapor atoms or molecules condense on the substrate. Soon after exposure to the incident flux a uniform distribution of small highly mobile clusters or islands form. In SK growth islanding happens to relieve the misfit strain without an energetic barrier associated with forming dislocations. The clusters grow in size and density until the islands begin to merge in what is known as the coalescence phenomenon. Coalescence decreases the island density allowing further nucleation to occur. Coalescence continues until a connected network with unfilled channels and voids develops. Finally the voids are filled and a continuous film results. .

The Stranski-Krastanov (SK) growth mode describes the germanium silicon heteroepitaxial growth system. This growth mode is a combination of the island and layer growth modes. The balance of forces changes during the growth due to the lattice mismatch between Ge and Si. *It has been shown that the condition for SK growth is that the mismatch (ε) is between 3% < ε < 7%* [21]. In SK growth, there is an initial adsorbate wetting layer of characteristic thickness. After the formation of one or more monolayers, subsequent layer growth becomes unfavourable and island growth begins to relive the misfit strain. Then there is a sudden transition from 2d to 3d islands, known as the *SK-transition* [21]. The final layer consists of separated 3d island upon a (reduced) persisting wetting layer. Figure 2.8 is a 2D cartoon of

germanium on silicon growth. The wetting layer is exaggerated in the image to highlight the SK growth mechanism.

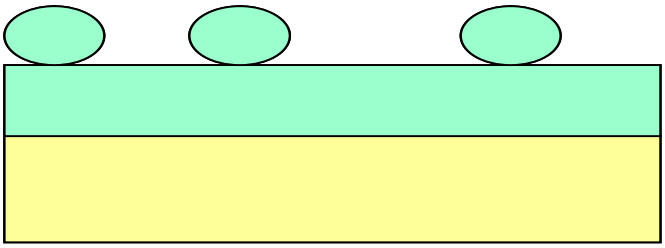


Figure 2.8: 2D diagram of germanium grown on silicon to highlight the SK growth mode.

Some examples of heteroepitaxial systems that follow the SK model are: Ge/Si, InAs/GaAs, PbSe/PbTe, CdSe/ZnSe, PTCDA/Ag. Finally, the SK growth mechanism can be used to grow self assembled quantum dots. The desired properties of them are: dislocation free, narrow size distribution, well-defined shape, and spatial ordering [22].

2.3 Dislocations

In addition to islanding associated with SK growth, germanium on silicon growth results in misfit dislocations that thread to the surface as threading dislocations. As described in the previous section, as the growth begins there is a thin wetting layer followed by islanding growth. Below the critical thickness, the germanium layer will be dislocation free and take the lattice constant of the underlying silicon layer. The critical thickness has been shown to be between 4-10nm for this system. However, this thickness will vary depending on the growth conditions. ***So as a result, germanium will be compressively strained by 4.2% below the critical thickness.*** Figure 2.9

shows a cross section and atomic view of germanium on silicon below the critical thickness. The cross section is shown as layer growth. However, depending on the growth conditions there may be islanding in this case.

As the deposited film gets thicker, atoms continue to be forced to a different lattice constant. The total strain energy increases linearly with thickness. Figure 2.10 is a cross section and atomic view of the germanium layer as the strain energy increases.

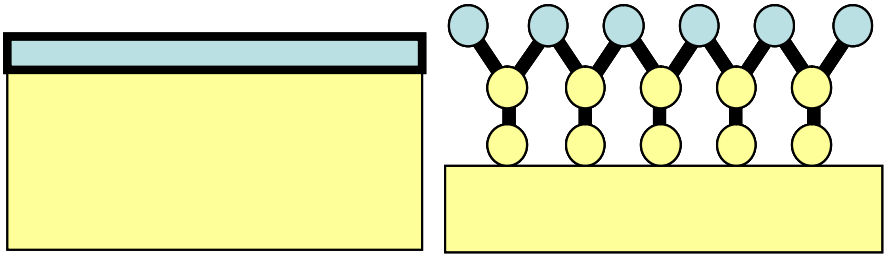


Figure 2.9: Cross section of germanium on silicon growth; Ge lattice is 4% bigger than Si, so the germanium is compressively strained by 4.2% below the critical thickness.

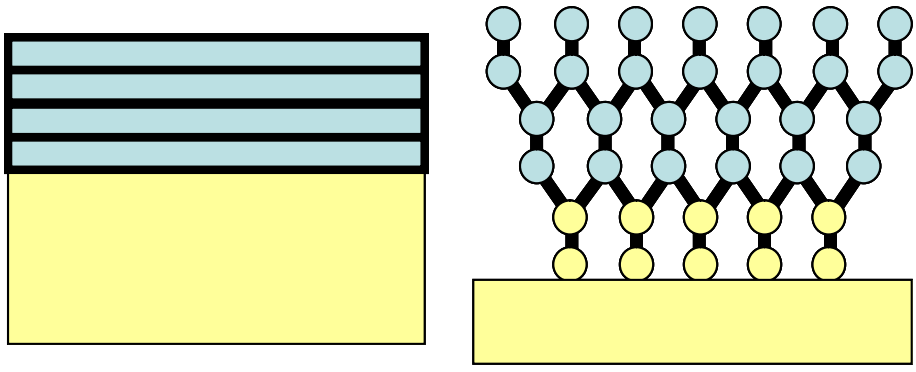


Figure 2.10: The total strain energy increases linearly with thickness

We can determine the strain energy by using the following relation

$$E_{strain} = \lambda \left(\frac{\Delta a}{a} \right)^2 At \tag{2.11}$$

where λ = biaxial elastic modulus, Δa = forced change in lattice constant, a = unstrained lattice constant, A = area and t = thickness of the film. As the growth continues, it becomes favorable to create defects in the film that allow the layer to adopt its relaxed lattice constant and relieve the strain. These defects are called misfit dislocations and are formed at the Ge/Si interface. Figure 2.11 is a cross section and atomic view of the germanium layer after the critical thickness and dislocations form.

There are two predominant dislocations in the Ge on Si system. Misfit-dislocations are introduced to relax the lattice mismatch between the layer and the Si substrate, and are typically confined to the interface between the layer and the Si substrate. They relax the lattice mismatch between the Ge layers and the Si substrate by introducing extra half plane of atoms. These misfit dislocations are confined to the interface between the Ge layer and the Si substrate and are energetically stable when the Ge thickness is larger than a critical thickness for misfit-dislocation formation. Threading dislocations are the by-product of the introduction of misfit-dislocations and do not relax lattice mismatch strain. Threading-dislocations are left in the layers because dislocations cannot end in a crystal. Dislocations have to either form a loop or terminate at a free surface. Since the layer surface is always the nearest free surface to the substrate, these threading dislocations typically thread from the layer-

substrate interface to the layer surface. The fact that devices are usually built close to the layer surface, threading-dislocations cannot be easily avoided and are a very important impediment in electrical devices. Threading-dislocations can reduce carrier lifetime, carrier mobility and compromise device reliability. Figure 2.12 is a cross sectional image of germanium as grown on Si highlighting the misfit/threading dislocations and surface roughness associated with SK growth [23].

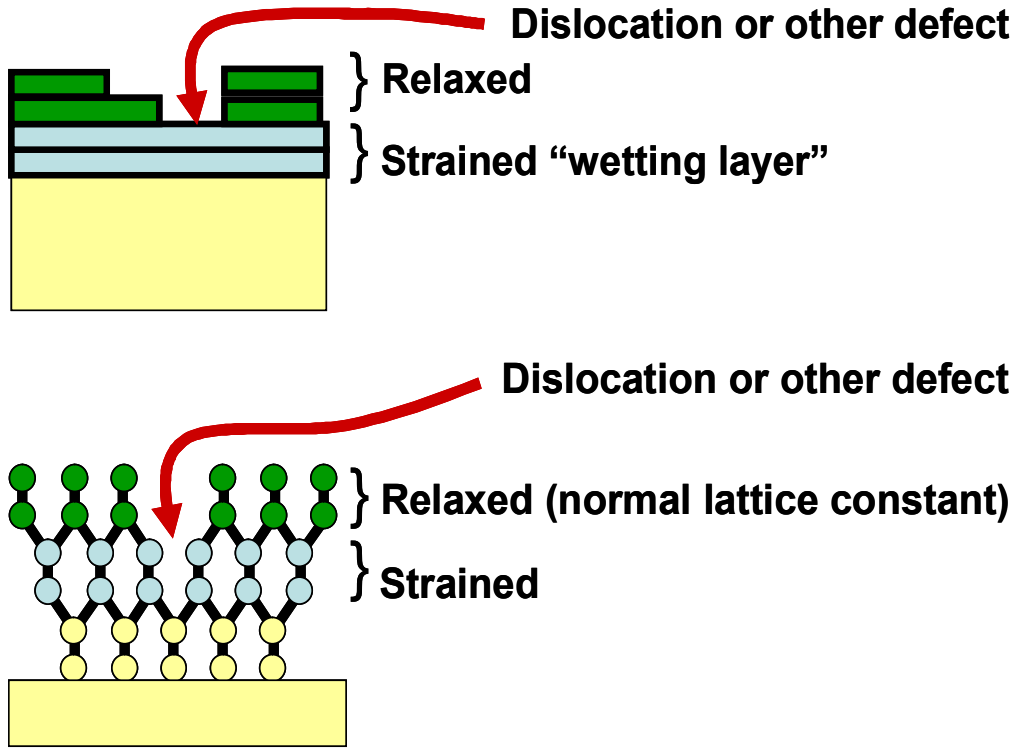


Figure 2.11: Cross Section and atomic view of germanium layer after critical thickness and dislocations have formed

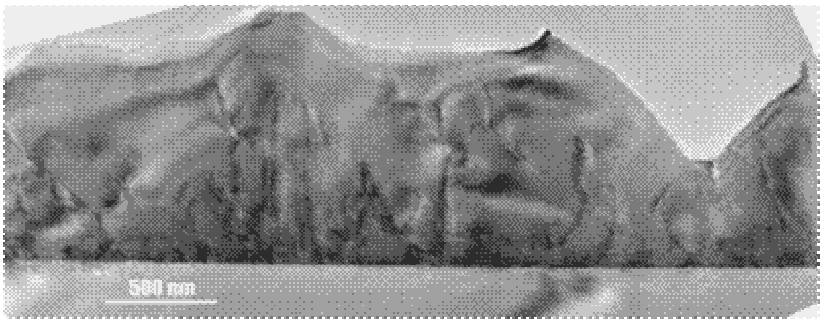


Figure 2.12: Cross section image of germanium layer grown on silicon showing misfit and threading dislocations

2.3.1 Threading Dislocation Density

There are two main ways to determine threading dislocation density: plan-view TEM and defect etching. Cross sectional TEM is an excellent way to study the defects in layer however it is difficult to quantify them due to the small viewing area. As a result, defect-etch and plan-view TEM are the most accepted and widely used methods for determining the threading dislocation density. Defect etching method, etches dislocations at a higher rate than the layer and thus etch pits appear visible using an optical microscope [24]. These etch pits are the dislocations and can be counted to determine threading dislocation density. In plan-view TEM dislocations appear as crystal imperfections in the lattice, and can thus be counted also. Threading dislocation density is reported as a density per cm^2. Typical values of threading dislocation density for the germanium on silicon system range from 10^{10} to 2×10^6 cm^{-}

[2]. The large range is due to the numerous methods published on growing germanium on silicon. Chapter 4 will include a timeline of research in germanium on silicon heteroepitaxy and describe more details about defect density determination.

2.4 Conclusion

As a semiconductor material, germanium has many advantageous over silicon both electrically and optically. Its higher intrinsic mobilities of both electrons and holes will allow high speed performance as channel length becomes shorter to the ballistic limit. In addition its band-gap will allow detection at wavelengths meeting the telecom industry standards. However, the lack of stable native oxide allows for Si to dominate the industry due to the high quality of SiO_2. Recent advances using high-κ and oxynitride on germanium has renewed interest in this area. However in order for germanium to become main-stream there needs to be an ability to grow high quality Ge layers on Si due to the many problems associated with bulk layers. The challenge is that there exists a 4.2% lattice mismatch between germanium and silicon which leads to growth that is dominated by dislocations and islanding. The islanding stems directly from the 4.2 % lattice mismatch in that the free energy at the surface continues to change as the growth proceeds resulting in a mix of layered and islanding growth (SK growth mechanism). The combination results in layers that are rough and unsuitable for any practical application. Misfit dislocations also form directly from the 4.2% mismatch and are generated to relieve the strain at the interface. In addition, these dislocations tend to thread through the substrate typically terminating at the top

surface where the devices are fabricated and are hence called threading dislocations. Chapter 3 and 4 will highlight the methods we employed to reduce the surface roughness and dislocations formed respectively.

CHAPTER 3

Surface Roughness Reduction

3.0 Abstract

As described in chapter two, there are two main challenges in growing germanium on silicon; large surface roughness due to islanding growth morphology and a large dislocation density that forms to relax the layer. The origin of both of these problems is the 4.2% lattice mismatch between germanium and silicon. In order to de-couple the two challenges, it was decided to research them separately with the ultimate goal of reaching one procedure to grow high quality relaxed germanium layers on silicon. This chapter will focus solely on the surface roughness reduction part of the research. It will start with an overview on Chemical Vapor Deposition Growth (CVD) and the experimental setup/equipment used in the Stanford Nanofabrication Facility (SNF). In addition, experimental basics of epitaxial growth will be discussed. This will lead to the hydrogen annealing experiment conducted and the results achieved. Finally, an experimentally based theoretical model for surface roughness reduction by hydrogen annealing will be presented.

3.1 Experimental Background

3.1.0 Chemical Vapor Deposition (CVD)

The ability to grow high quality films on semiconductors substrates is very important for many applications. The method used depends on the materials to be deposited. In semiconductor CMOS processing today some of the more popular materials needed are silicon, low temperature oxide (LTO), various dielectrics, germanium, or silicon-germanium. The method of choice used in all cases is chemical vapor deposition (CVD). In CVD, the film is produced by chemical reactions that take place on the substrate surface between reactant gases that are introduced into the deposition chamber [25]. On the other hand, physical vapor deposition (PVD), which is based on physical methods such as, evaporation or sputtering, is primarily used to deposit metals. In PVD, we produce the atoms which pass through a low-pressure gas phase and then condense on the substrate. In this work, PVD was used during Metal Oxide Semiconductor capacitor and transistor fabrication; this step will be discussed in chapter 5. All germanium growth for this work was done by CVD, and will be the discussed here in detail.

In CVD growth, the film producing reaction must take place on the surface of the substrate and not in the gas stream. This helps avoid any gas phase reaction that could deteriorate the film quality [25]. The Stanford Nanofabrication Facility CVD reactor used in this work is a “cold wall” reactor, in that the walls of the chamber are

not heated. Figure 3.1, taken from "Silicon VLSI Technology" by James Plummer, shows a common configuration of a cold-wall rector [25]. The wafers are heated by using a graphite susceptor which in turn is heated by RF induction. Since only the wafer and susceptor are heated, deposition on the reactor walls is minimized. On the other hand, to grow high quality low temperature oxide we use a "hot-wall", or Low Pressure CVD chamber. The growth is done at a low pressure with the wafers stacked upright.

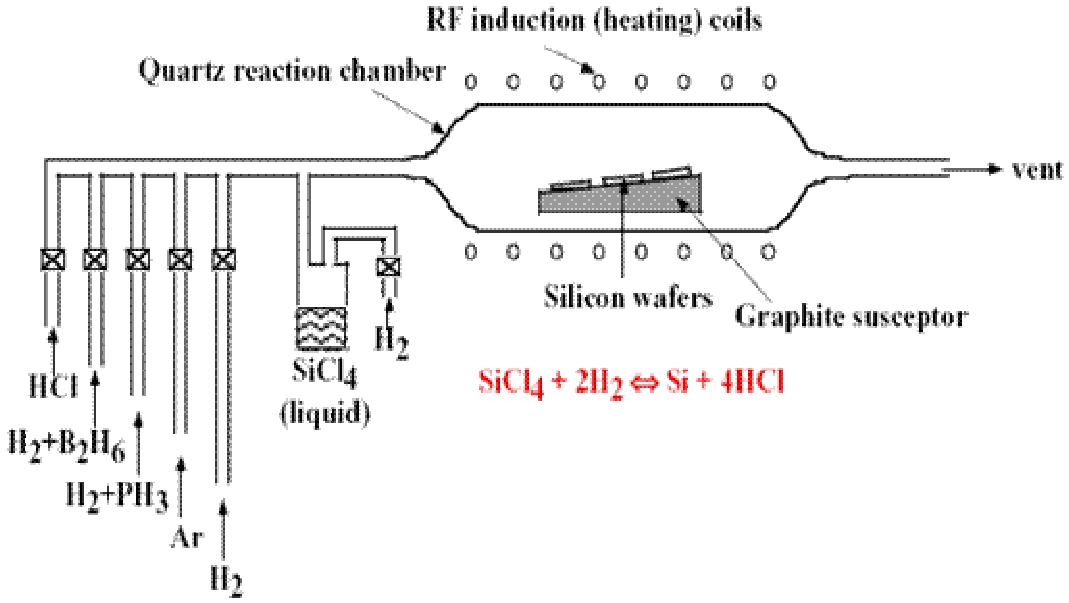


Figure 3.1: Common configuration of cold-wall reactor

The CVD growth process can be described by seven steps [25]. Figure 3.2 highlights these parts with arrows. First, the reactants are transported to the deposition region. Second, there is diffusion of the reactants from the gas stream through the

boundary layer to the wafer surface. Third, the reactants are adsorbed on the wafer surface. Fourth, chemical decomposition and reactions takes place on the surface accompanied with surface migration to attachment sites. Fifth, byproducts are desorbed from the surface. Sixth, the byproducts flow to the main gas stream by diffusion. Finally, a thermal process is used to force away the byproducts from the deposition region.

The next section will highlight the chemicals used for germanium deposition.

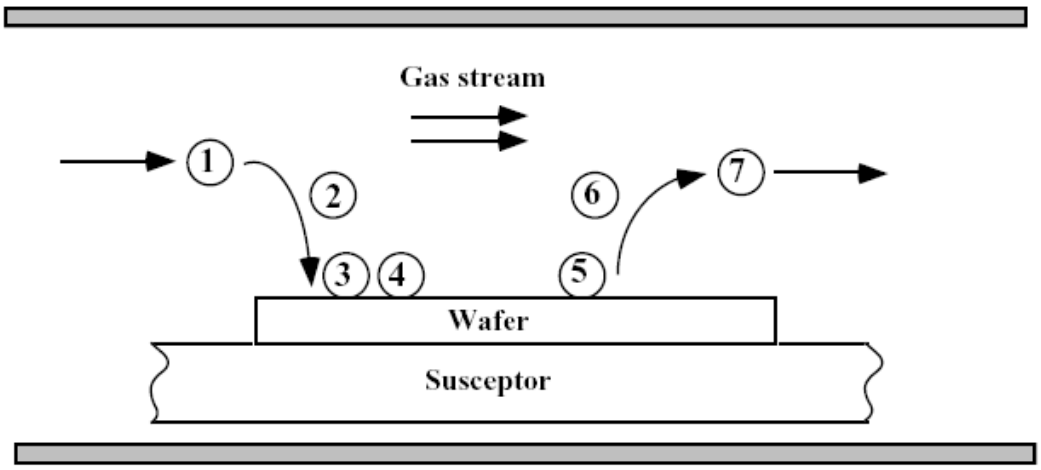


Figure 3.2: The seven parts of a CVD process.

3.1.1 Heteroepitaxial-Germanium Growth

In order to grow relaxed heteroepitaxial germanium layers on silicon, the proper gas is needed that would lead to the chemical reaction on the surface. Epitaxial

growth is unique in that the growth conditions are such that grown film takes the crystal lattice of the underlying surface substrate film. Ideally, the grown substrate will be single crystal if the underlying substrate is single crystal. For example, epitaxial silicon is grown by decomposing silane by the following reaction,

$$SiH_4 \longrightarrow Si + 2H_2$$

Similarly epitaxial germanium is grown by decomposition of germane by the following reaction,

$$GeH_4 \longrightarrow Ge + 2H_2$$

So as a result, heteroepitaxial growth of Ge on single crystal Si, should result in single crystal Ge.

Growth of single crystal Ge on Si depends strongly on the growth conditions used. One of the major variables in this growth process is temperature. The temperature needs to be high enough to allow for the chemical reaction to take place and to allow for the Ge atoms to arrange in a single crystal manner. For growing single crystal Ge layers, the typical growth temperatures for the proper reaction to take place on the surface ranges from 400°C to 600°C, with the higher temperature yielding the faster growth rate. Below 400°C temperature, the proper reaction may not take place and growth may result in polycrystalline Ge or even amorphous Ge. Apart from growth temperature the other variables that affect the growth are pressure and germane concentration. In order to get the best quality films, low pressure growth is needed. The germane concentration can be used to increase the growth rate of the layer. All of

these conditions may vary from chamber to chamber so it is important to characterize and optimize the chamber and growth prior to growth. In addition, a very clean surface is needed to get good epitaxial growth. If there is any contaminant or native oxide, epitaxial growth will not occur. The next section will detail the pre-cleaning step used in our experiments.

3.2 Experimental Procedure

3.2.0 Hydrogen Annealing

The idea to use hydrogen annealing to reduce the surface roughness of chemical vapor deposition based heteroepitixally grown germanium layers on silicon was motivated by work done on epitaxial silicon layers. In the work, *"Hydrogen annealed silicon-on-insulator",* Sato and Yonehara were able to reduce the surface roughness of bonded and etch-back silicon-on-insulator (BESOI) wafers from 10nm to less than 0.1nm by hydrogen annealing [26]. They attributed this to surface migration of Si atoms driven by surface energy minimization after removing native oxide. Figure 3.3 is a plot taken from reference [26] showing surface roughness reduction by hydrogen annealing. It is well established that the Si surface diffusion rate is exponentially dependent on temperature due to an activation barrier for diffusion [27].

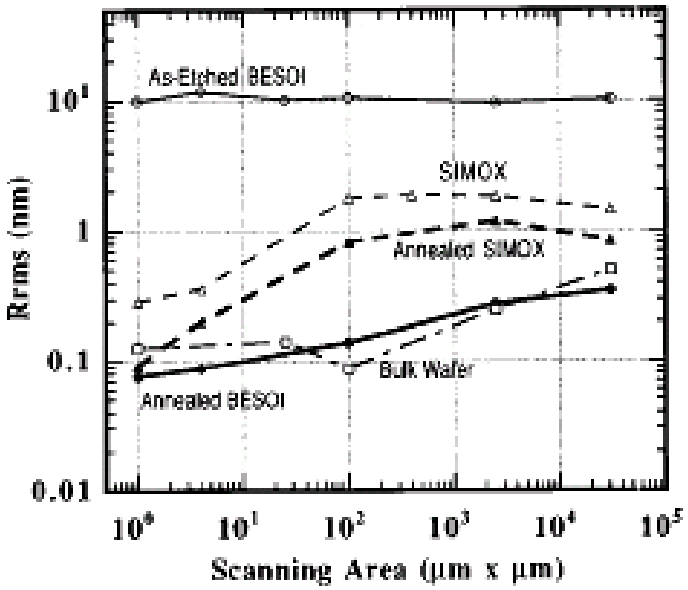


Figure 3.3: Surface Roughness, R_{rms}, reduction of as-etched BESOI from 10 to 0.1 nm by hydrogen annealing [26].

3.2.1 Experimental Recipe

In order to study the effect of hydrogen annealing on the surface roughness of germanium, an experiment was designed. The first step of the experiment is to produce a baseline rough germanium layer that can be used for hydrogen annealing experiments. As it turns out, the initial thickness of Ge eventually plays a very important role in the final layer achieved. More detail on this subject will be covered in the next section. It should be noted that all experiments for this project were done at Stanford nanofabrication facility (SNF) in the Center for Integrated Systems (CIS). Figure 3.4 is a picture of the ASM epitaxial reactor in the SNF.

Figure 3.4: Picture of the author working in the SNF lab near the ASM epitaxial reactor

In order to get high quality epitaxial growth, a very clean surface is needed. With this in mind, a standard pre-diffusion wafer clean is carried out. This clean is also required to keep the chamber at a clean level. The pre-diffusion clean is done at the WBDIFF diffusion bench in SNF [28]. The first step of the clean, sometimes called piranha, uses a 4:1 ratio of Sulfuric Acid (H_2SO_4) and Hydrogen Peroxide (H_2O_2) at around 80˚C for 10 minutes. This clean removes organics and gross contaminants like scribe dust. The H_2SO_4 reduces organics to carbon while the H_2O_2 oxidizes carbon to form CO_2.. After the clean, a dump rinse is done in dionized water (DI water) to clean the wafer of any chemicals and get it ready for the next clean. The next clean is a solution of 5:1:1 DI water, hydrochloric acid (HCL), and Hydrogen Peroxide H_2O_2, respectively. This is sometimes called the metallic or alkali clean. The alkali clean is done for 10 min at typically around 70˚C. It removes metallic

contaminants and alkali ions. The H_2O_2 oxidizes the surface while the HCl reacts with most metals to form soluble chlorides. Thus the alkali clean leaves a chemical oxide on the Si surface. After this clean, a DI water dump rinse is done to clean the wafer of any chemicals and get it ready for the next clean. The next and final clean is hydrofluoric acid (HF) or sometimes called an oxide clean/etch. In our case, a 50:1 dilute solution of HF is used. HF clean removes oxides from the wafer surface which is required for good epitaxial growth. It is important to use a fresh batch of HF to insure sufficient oxide etch. After the HF clean a DI water dump rinse is done which is followed by a final dump rinse followed by a spin dry. This completes the cleaning process. Table 3.1 shows the complete pre-epitaxial growth clean.

Step	**Clean Name**	**Chemicals**	**Time**	**Temp**	**Function**
1	Piranha	Sulfuric Acid H_2SO_4, Hydrogen Peroxide H_2O_2	10min	~80˚C	Removes organics and gross contaminants
2	Dump Rinse	Dionized Water	8min	Room	Cleans Wafer for before next clean
3	Alkali clean	5:1:1 DI water, Hydrochloric Acid (HCL), and Hydrogen Peroxide (H_2O_2)	10 min	~70˚C	Removes metallic contaminates and alkali ions
4	Dump Rinse	DIonized (DI) Water	8min	Room	Cleans Wafer for before next clean
5	Oxide Clean/Etch	50:1 dilute solution of Hydrofluoric Acid (HF)	30sec	Room	Removes Oxide
6	Dump Rinse	DIonized (DI) Water	8min	Room	Cleans Wafer for before next clean
7	Dump Rinse Spin Dry	DIonized (DI) Water/N2 Dry	8min	Room	Cleans and Dries wafer

Table 3.1: Complete pre-diffusion clean before epitaxial growth

It is important to immediately load the wafers into the reactor to insure no native oxide grows on the surface. After loading the wafer in the chamber, it is important to let it sit in the holding area for a short time before proceeding. During this time nitrogen is purged in the chamber driving out any additional moisture on the surface. At this time recipes can be created or modified with no safety hazard since the computer recipe functions is independent of the chamber control. After preparing the chamber the proper recipe is selected.

The first step in all growth recipes is to etch the chamber before the wafer is loaded in the deposition part of the chamber. This etch is standardized for all recipes and consists of nine steps. The chamber temperature is set to 1170°C and HCl is used to etch the chamber. After this etch is done, the temperature is dropped to the load temperature of 800°C and the wafer is loaded in the chamber. After the wafer is loaded, a high temperature hydrogen bake is used to etch any native oxide that will block epitaxial growth. The hydrogen bake temperature and time are variables that can be used depending on the growth needed. If one is growing very thin layers the selection of temperature becomes very critical. In some cases one may be limited in thermal budget depending on the underlying Si substrate and the features on the wafer. The standard temperature in the SNF reactor is from 950°C-1170°C for as little as 5min to as long as 20min. For very critical thickness and growth rates, a longer time and higher temperature are needed. In our case, we found through optimization that 950°C at 50sccm of H_2 for 5 minutes at a pressure of 80 Torr is sufficient to get good heteroepitaxial Ge growth on Si. It should be noted that the hydrogen bake

temperatures in the range of 800°C-850°C resulted in no epitaxial Ge growth, thus highlighting the importance of the hydrogen anneal.

After the hydrogen bake, the growth begins. The first step is deciding on the temperature for good heteroepitaxial growth. Our goal was to grow a layer relatively thick to do studies on the surface roughness. After many experiments, the optimal temperature and time were found to be 400°C for 15min. Therefore the next step is to ramp the temperature down from 950°C to 400°C in 300 seconds. Following that is a 90 second step to stabilize the growth conditions. Namely, the germane (GeH_4) gas is turned on using a 30sccm flow and the pressure is dropped to 10torr to slow down the growth rate to get a better quality Ge layer. With all these conditions met, a 200nm layer of Ge is achieved on Si that has a rough island-like surface. This was confirmed by cross sectional-SEM, AFM and TEM. More detail on the imaging will be presented in the following section on results. We note that the processed wafer as seen by the naked eye is very hazy and not reflective. This is an indication of the high surface roughness of the layer. Thus this is an optimal layer to do hydrogen annealing experiments. It should be noted that these layers were all grown with no doping. More details on the doping process will be presented in chapter 5 where we describe the electrical behavior of the devices fabricated. Table 3.2(a) and 3.2(b) show the growth recipe of the initial baseline Ge growth on Si [29,30].

	Step 1	Step 2	Step 3	Step 4
Step Name	Start	Heat 1	Heat 2	Etch 1
Duration	0.1	30	45	10
Token				
Center	1170	1170	1170	1170
Dep/Vent	VENT	VENT	VENT	VENT
N2/H2	20H	10HR	10H	10H
Rotation	0	25RU	25U	25U
HCLHI	0V	0V	20ER	20E
HCL	0V	0V	0V	0V
SiH4	0	0	0	0
German	0	0	0	0
V_pressure	ATM	ATM	ATM	ATM
Vent Match	0	0	0	0
P-Dill	0	0	0	0

	Step 5	Step 6	Step 7	Step 8	Step 9
Step Name	Etch 2	Etch 3	Cool	Homesus	TEMP ck
Duration	30	45	50	60	0.1
Token					
Center	1170	1170	800	800	850s
Dep/Vent	VENT	VENT	VENT	VENT	VENT
N2/H2	80HR	80H	80H	40HR	20H
Rotation	25D	25D	10RD	0	0
HCLHI	20E	20E	0V	0V	0V
HCL	500E	500E	0V	0V	0V
SiH4	0	0	0	0	0
German	0	0	0	0	0
V_pressure	ATM	ATM	ATM	ATM	ATM
Vent Match	0	0	0	0	0
P-Dill	0	0	0	0	0

Table 3.2: Chamber etch recipe before the wafer is loaded in to the chamber (steps 1-9)

	Step 10	Step11	Step 12	Step 13	Step 14
Step Name	LOAD	RAMP	BAKE	TEMP CK	STABDEP
Duration	0.1	0.1	2:00	300	90
Token					
Center	800	950S	950	400S	400
Dep/Vent	VENT	VENT	VENT	VENT	VENT
N2/H2	10H	42H	50HR	22H	22H
Rotation	0	35R	*SAME	*SAME	*SAME
HCLHI	0V	0V	0V	0V	0V
HCL	0V	0V	0V	0V	0V
SiH4	0	0	0	0	0
Germane	0	0	0	30	30
V_pressure	ATM	ATM	80	80	10
VentMatch	0	0	1	1	1
P-Dill	0	0	0	0	0

	Step 15	Step 16	Step 17	Step18	Step19	Step20
Step Name	DEPOSIT	POSTPRG	HOMSUS	UNLOAD	TMP RMP	END
Duration	15:00	45	15	.1	180	1
Token				UNLOAD		END
Center	400	400	400	400	800	800
Dep/Vent	DEPSOSIT	VENT	VENT	VENT	VENT	VENT
N2/H2	22H	20H	10HR	10H	20H	20H
Rotation	*SAME	10R	0	0	0	0
HCLHI	0V	0V	0V	0V	0V	0V
HCL	0V	0V	0V	0V	0V	0V
SiH4	0	0	0	0	0	0
Germane	30	0	0	0	0	0
V_pressure	10	ATM	ATM	ATM	ATM	ATM
VentMatch	1	0	0	0	0	0
P-Dill	0	0	0	0	0	0

Table 3.3: Initial baseline growth after wafer is loaded (Steps 10-20)

Now that the baseline recipe is complete, the hydrogen annealing experiment will follow. Five different hydrogen annealing temperatures (600 °C, 700 °C, 725 °C, 763 °C, and 825 °C) were carried out for 1 hr immediately following the baseline growth, at a pressure of 80 Torr. One wafer was left un-annealed for comparison. The 763 °C hydrogen bake temperature sample was chosen by taking the ratio of melting points between Si/Ge and multiplying the optimal annealing temperature from reference [26]. In order to complete this study, the hydrogen annealing part must be added to the baseline recipe. The annealing was done in-situ, without taking the wafer out of the chamber to avoid growth of a native oxide. So after the growth step at 400°C, the temperature is ramped up to the hydrogen annealing temperature. In addition, the pressure is also ramped from 10 Torr to 80 Torr. This was done because, if the pressure had been raised from 10torr to 80torr in one step, this would have produced stabilization errors, resulting in a system shut down. After the pressure and temperature were set, the hydrogen flow was increased to 50sscm and the annealing for 1hr was done. Table 3.4 shows the complete hydrogen annealing recipe. It should be noted that the initial layers were grown without any doping. The CVD reactor also gives us the ability to in-situ dope the layer. More details on the doping will be discussed further in chapter 5 when the electrical devices are discussed. The results of the hydrogen annealing experiment will be presented in the next section.

	Step 15	**Step 16**	**Step17**	Step 18
Step Name	DEPOSIT	**TEMP CHECK**	**BAKE**	POSTPRG
Duration	15:00	**5:00**	**60:00**	45
Token				
Center	400	**825S**	**825**	825
Dep/Vent	DEPSOSIT	**VENT**	**VENT**	VENT
N2/H2	22H	**22H**	**50HR**	20H
Rotation	*SAME	***SAME**	***SAME**	10R
HCLHI	0V	**0V**	**0V**	0V
HCL	0V	**0V**	**0V**	0V
SiH4	0	**0**	**0**	0
Germane	30	**0**	**0**	0
V_pressure	10	**80R**	**80**	ATM
VentMatch	1	**1**	**1**	0
P-Dill	0	**0**	**0**	0

Table 3.4: Modified growth recipe from table 3.3 with hydrogen annealing inserted after step 15

3.3 Results

We characterized the surface roughness of the grown germanium layers using atomic force microscopy (AFM) and cross-sectional high resolution scanning electron microscopy (HR-SEM). AFM measures surface topography on a scale from angstroms to 100 microns. The technique involves imaging a sample through the use of a probe, or a tip, with a radius of 20 nm. The tip is held several nanometers above the surface using a feedback mechanism that measures surface–tip interactions on the scale of nanometers. Variations in tip height are recorded while it is scanned repeatedly across

the sample, producing a topographic image of the surface. On the other hand, the electron microscope can magnify very small details with high resolving power, at levels up to 500,000 times, due to the use of electrons as the source of illumination. Due to the manner in which the image is created, SEM images have a characteristic three-dimensional appearance and are useful for judging the surface structure of the sample. SEM produces images by detecting secondary electrons, which are emitted from the surface due to excitation produced by the primary electron beam. In the SEM, the electron beam is scanned across the sample, with detectors building up an image by mapping the detected signals with beam position. Generally, transmission electron microscopy (TEM) resolution is about an order of magnitude better than the SEM resolution, however, because the SEM image relies on surface processes rather than transmission it is able to image bulk samples and has a much greater depth of view. So it can produce images that are a good 3D representation of the surface of the sample. TEM will be described in detail in chapter 4.

In order to quantify the surface roughness, 10 x 10 μm AFM sweeps were used to extract root-mean-square surface roughness (R_{rms}) and to view surface topology. Figure 3.5 shows the result of the topographical AFM images for the various temperature annealing. Included, above each picture, is the R_{rms} (nm) from the 10 x 10um scan. Clearly evident is the reduction in R_{rms} for the higher temperature anneals. For instance, the R_{rms} for the no anneal case is 25nm and for the 600°C case is 14nm. In fact, the wafer tends to appear more mirror like at the lower R_{rms} values. As the temperature is increased above 600°C the R_{rms} drops to 5nm at 700°C, 3nm at 763°C, and 2.5nm at 825°C.

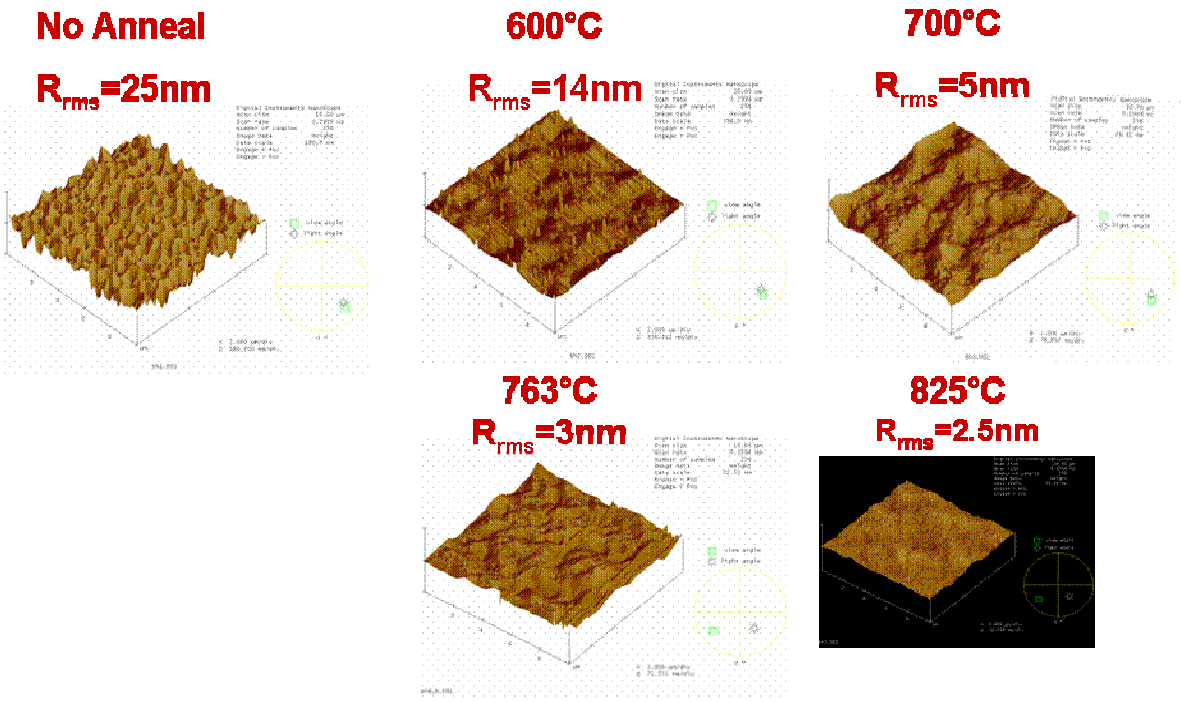


Figure 3.5: Topographical AFM images with R_{rms} value from 10µm x 10µm AFM scan showing 90% reduction in surface roughness

Figure 3.6 (a)-(b) is a tilted High Resolution Scanning Electron Microscopy cross section of the un-annealed sample along with the 825 °C annealed sample. The samples are mounted on a holder angled at 45° to the normal, thus making the cross section as well as the surface visible at the same time. This way the surface smoothing is visible along with the cross section of the layer. In the un-annealed sample image, clearly visible are islands of Ge and the surface roughness is very high as expected from the S-K growth model due to the lattice mismatch (R_{rms} ~25 nm). The surface appears continuous but with island-like with hills and valleys. However, the image of the annealed sample shows a reduction in surface roughness compared to the un-

annealed sample. The islands have flattened to the point where they no longer are visible in the image (R_{rms}~2.5 nm).

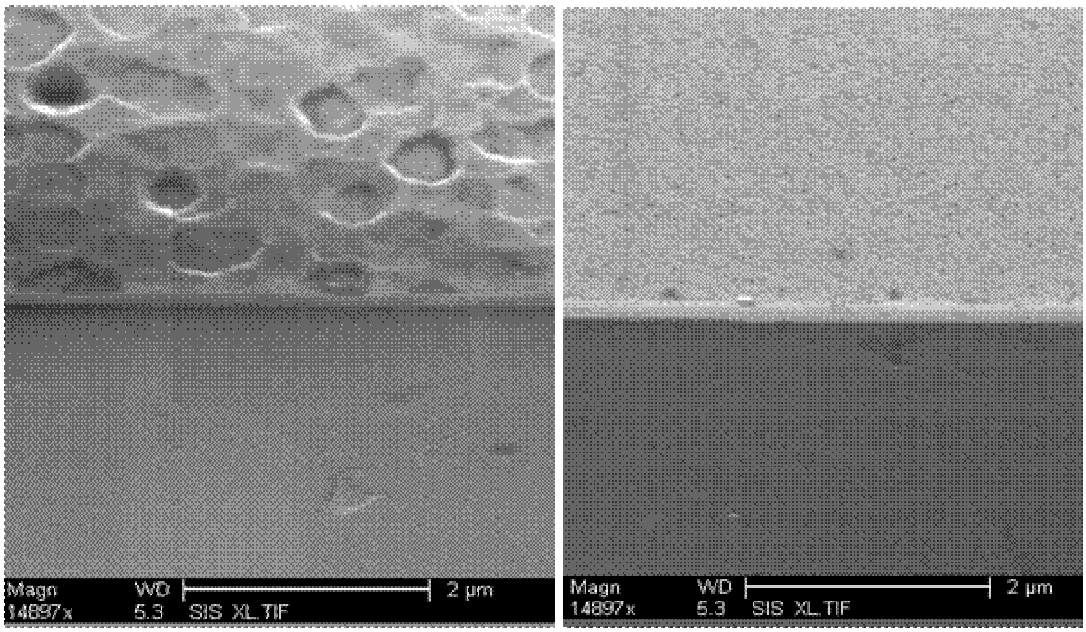


Figure 3.6: 45 degree cross sectional image of 600°C (left)/825°C (right) hydrogen annealing showing 90% reduction in surface roughness.

The temperature dependence of the R_{rms} reduction is shown in Figure 3.7 (right Y-axis) which plots the change of R_{rms} vs. Temperature, where change was defined as the difference between R_{rms} at annealing temperature and R_{rms} of the un-annealed case. Surface roughness reduction is clearly seen with a 90% reduction at 825 °C. The temperature dependence of the R_{rms} yields a tapering off effect where a large reduction exists in raising the hydrogen bake temperature from 600 °C to 700 °C, while a much smaller drop occurs in a further temperature increase from 700 °C to 800 °C. The curve shows that surface roughness is reduced asymptotically with increasing T, as one would expect for a thermally-activated process such as surface diffusion. At

higher temperature a larger fraction of atoms on the surface has sufficient thermal energy to overcome the barrier to hopping [29, 30].

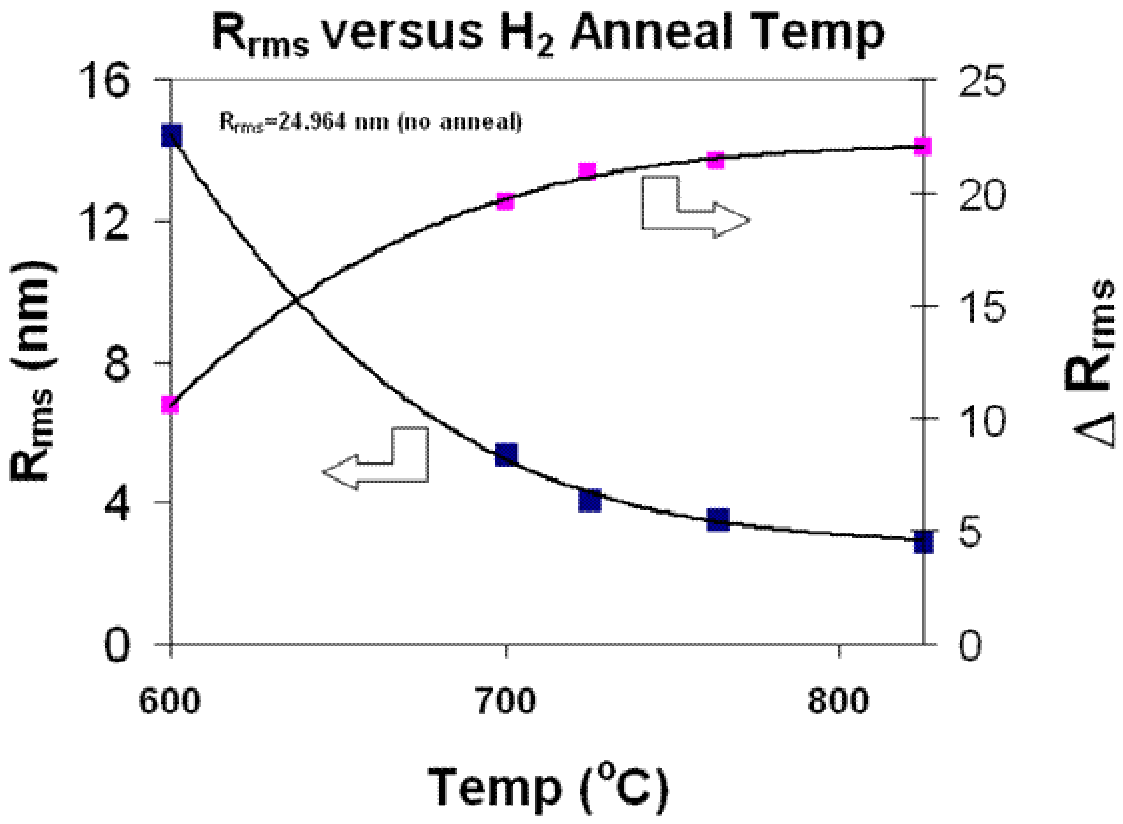


Figure 3.7: R_{rms} and ΔR_{rms} vs Temp of hydrogen bake showing tapering off effect

3.4 Surface Roughness Reduction Model (SRrM)

3.4.0 Base-line Ge layer

The following section describes an experimentally based theoretical model explaining the surface roughness reduction results obtained. It was found that the first step needed for surface roughness reduction to take place is growth of a germanium layer on silicon that is relaxed, and continuous with an island-like surface. There exist upper and lower limits to the initial thickness needed to achieve the necessary condition. The upper limit is defined by the surface roughness of the top layer due to the fact that the Ge layer may eventually coalesce to a smooth layer. However, this is dependent on the growth temperature and it is likely not to occur at such low temperatures. The lower limit is governed by the strain relaxation energy. For surface roughness reduction during subsequent post-deposition annealing, a relaxed Ge layer is required. Figure 3.8 is a cross sectional cartoon image showing the initial layer grown. As shown in the cartoon, dislocations have formed thus the layer is relaxed. The layer is very rough with R_{rms} value of 25nm as determined by AFM analysis in the previous section.

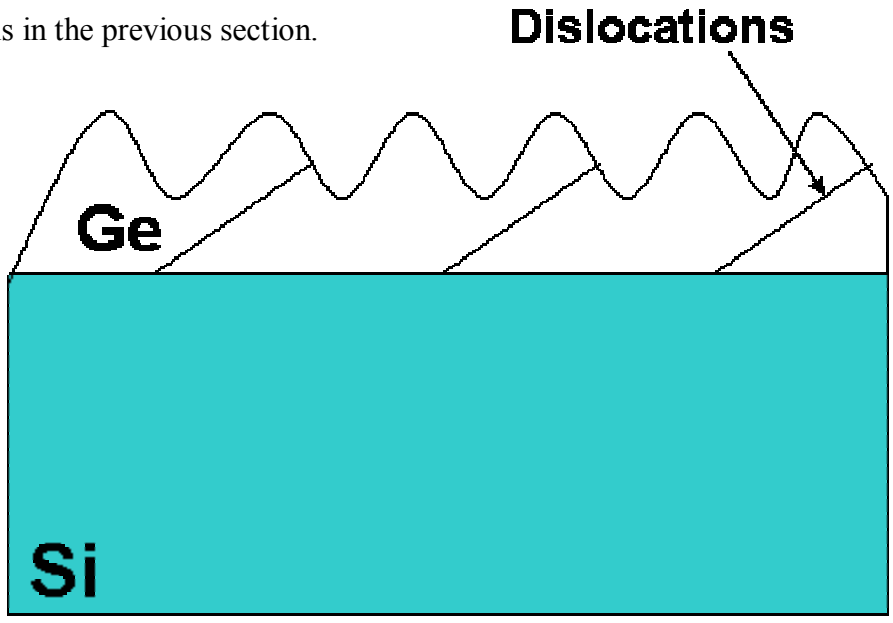


Figure 3.8: Cross sectional cartoon of initial baseline germanium layer

3.4.1 Hydrogen Annealing

The next step in the process is hydrogen annealing in the range of 600-825°C. During the annealing, germanium and hydrogen atoms are highly mobile since surface diffusion rates are exponential dependent on temperature. As a result, Ge-H bonds are not stable and H atoms on the Ge surface continually adsorb/desorb. In addition, the hydrogen ambient also plays a vital role in preventing any oxide formation on the surface that would essentially block Ge diffusion from taking place. The beneficial effect of H_2 annealing was confirmed experimentally by demonstrating that annealing in a nitrogen ambient, which likely contains a small oxygen impurity concentration, caused no change in surface roughness. Thus it was concluded that the presence of H in the growth process facilitates Ge surface diffusion. Figure 3.9 shows the various mechanisms taking place during hydrogen annealing.

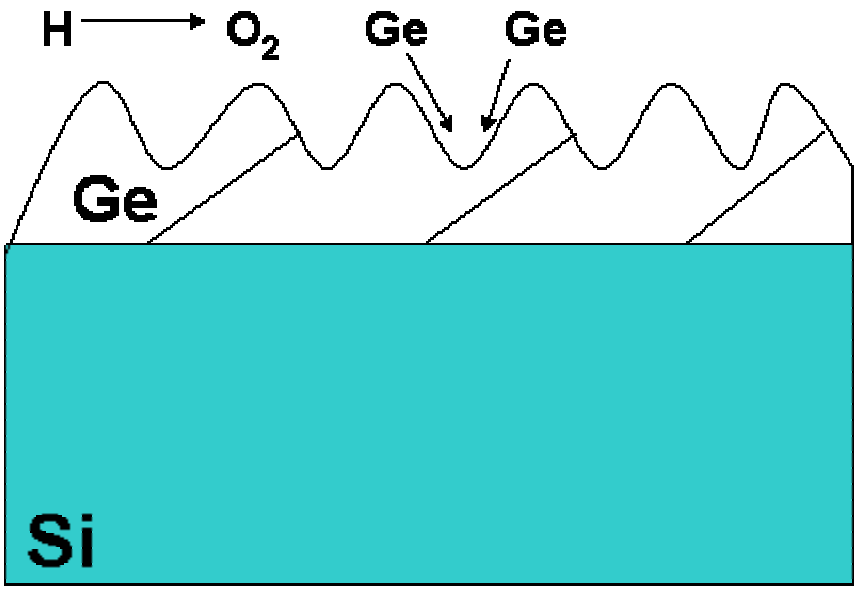


Figure 3.9: Cross sectional cartoon of initial germanium layer during the hydrogen annealing. The hydrogen ambient prevents surface oxide from forming allowing for germanium surface diffusion to take place

3.4.2 Chemical potential

The main parameter that governs Ge surface diffusion is the chemical potential ($\boldsymbol{\mu}$) of atoms on the surface. This potential will determine the direction of the mass transport during the annealing; the direction of the Ge diffusion on the surface. Atoms diffuse from regions of high chemical potential to regions of lower chemical potential. The chemical potential of a curved surface can be described by a simple continuum model [31]. This assumes a linear dependence of the surface chemical potential on surface curvature $\kappa(x,y)$. Equation 3.1 describes the change in chemical potential on a surface.

$$\mu = \mu_o + \Omega\gamma\kappa(x,y) \qquad \textbf{(3.2)}$$

The first term, μ_o is the chemical potential of a flat surface. In the second term of Ω is the atomic volume, γ is the surface free energy per unit area and $\kappa(x,y)$ is the surface curvature. In our case, the surface curvature totally governs the change in chemical potential on the surface since the layer is fully relaxed and defects have formed during the film growth and the initial stages of the anneal. The next section will highlight the case where stress can change the chemical potential profile. Convex regions will have a positive curvature while concave regions will have a negative curvature relative to the flat surface. Thus, the convex regions have a higher chemical potential than concave regions. As a result, Ge diffuses from convex regions to concave regions or

from higher chemical potential to lower chemical potential. Figure 3.10 shows magnified image of an individual hill and valley on the surface of the baseline Ge layer with the direction of the surface diffusion.

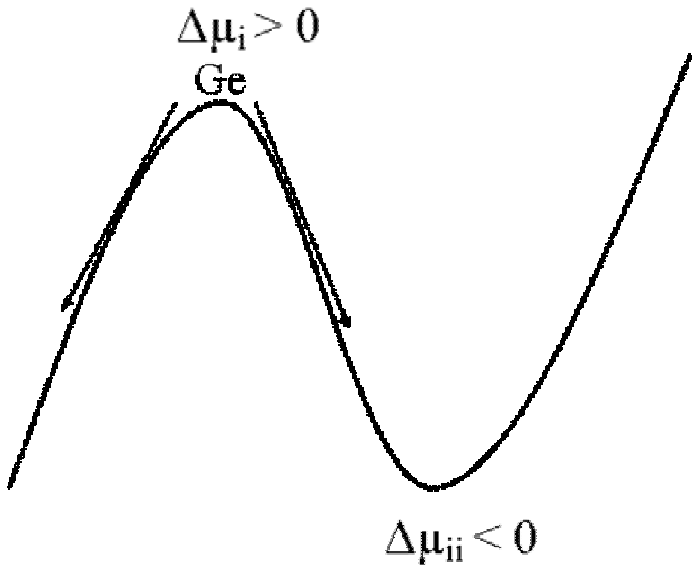


Figure 3.10: This is a cartoon of an individual hill and valley from the baseline Ge layer. Diffusion takes place from the region of positive curvature to the region of negative curvature; from concave up to concave down.

3.4.3 Effect of Strain on Chemical potential

In the case of strain, an extra term is added to equation that governs the surface potential [31].

$$\mu = \mu_O + \Omega\gamma\kappa(x, y) + \Omega E_s \qquad \textbf{(3.2)}$$

E_s is the elastic strain energy, which includes the misfit strain and a quadratic relationship with curvature. One example of such a system is Ge islands grown on Si where the islands are compressively strained due the lattice mismatch. The strain energy of surface atoms in this case is highest near the edges of the islands near the Ge/Si interface. Thus the strain relaxation term produces local chemical potential minima in the most convex regions opposite to the previous case. Figure 3.11 is a cross sectional cartoon showing the Ge islands on Si and the local chemical potential minimum. In this case during annealing, the island size will coarsen as diffusion will take place from the edges of the Ge/Si interface to the next adjacent island.

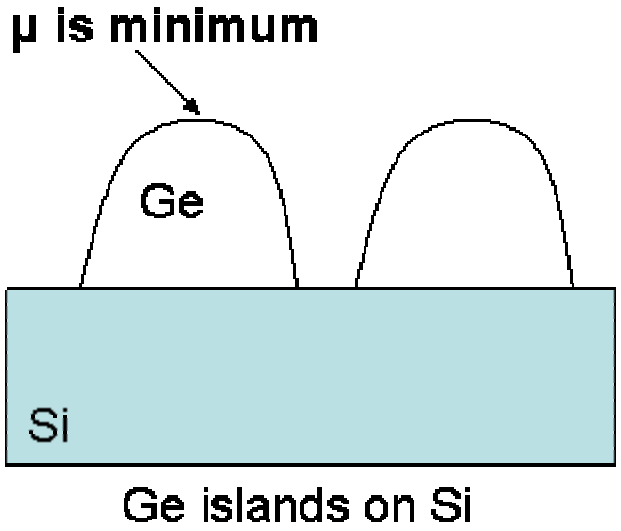


Figure 3.11: Cross sectional cartoon of Ge islands on Si showing local chemical potential minimum at the top of the Ge islands.

The above phenomenon has been observed experimentally in reference [32]. In this reference, the effect of hydrogen annealing on the surface roughness of Ge islands grown on Si was studied. The authors observed that after annealing the number of

islands reduce and surface roughness increases. To sum it up, in reference [32] and in this work as well, Ge surface diffusion is enhanced at higher temperature due to the presence of hydrogen. However, the chemical potential profile of the surface varies and thus the final surface topology or the minimum local surface energy state will also vary as a function of position.

3.5 Conclusion

In summary, chapter 3 began with a background on epitaxial Ge growth followed by a description of the equipment used in Stanford Nanofabrication Facility (SNF). This was followed by a presentation of the baseline Ge layer and hydrogen annealing experiment. We have demonstrated surface roughness reduction of relaxed heteroepitaxial layers of Ge layers grown on Si approaching 90% by hydrogen annealing. We found by studying the temperature dependence, the R_{rms} reduction becomes nearly temperature independent at elevated temperatures. Finally, an experimentally based theoretical model was presented to explain the surface roughness reduction results obtained.

Next, chapter 4 will focus on the complete method that was developed to grow relaxed Ge layers on Si.

CHAPTER 4

Multiple Hydrogen Annealing for Heteroepitaxy, *"MHAH"*

4.0 Abstract

One of the most important consequences of the lattice mismatch of Ge on Si is that dislocations form during the heteroepitaxy to relieve the misfit stress. These dislocations form at the Si/Ge interface as misfit dislocations and subsequently thread to the surface as threading dislocations, generally making the layers unsuitable for device applications. People and Bean calculated, from thermodynamic arguments, that in order to grow 100Å of Ge_xSi_{1-x} film on Si (100) without dislocations, one has to limit the Ge content to less than 50% [32].

This chapter focuses on the method we developed to reduce threading dislocations near the surface of the Ge layers. The chapter starts first with a historical timeline of research in the area, highlighting the most significant publications. Second, the initial idea to grow Ge on Si will be described. Third, the first Ge

growth experiment and characterization of the layers will be presented. Last, but not the least, an experimentally based theoretical model will be presented to explain the complete growth method.

4.1 History and State of the Art

Historically, heteroepitaxy of germanium on silicon has been a challenge. Many novel ideas and techniques have been introduced to grow high quality Ge layers. These layers have resulted in threading dislocation densities in the range of a 1×10^{7} cm^{-2} -1×10^{9} cm^{-2}. The following is a historical timeline of the important research publications in this area over the past three decades, giving a clear understanding to the direction of the research and the "state of the art" in this field.

1) Molecular Beam Epitaxy (MBE) 1983

Bean et al. from Bell Labs in "Pseudomorphic growth of Ge_xSi_{1-x} on silicon molecular bean epitaxy" [33].

Ge_xSi_{1-x} layers were grown on Si substrates over a full range of alloy compositions at temperatures from 400°C-750°C by means of molecular beam epitaxy. At a given growth temperature, films grow in a smooth, two dimensional manner up to a critical germanium fraction x_c. Beyond x_c the growth is rough. X_c increases from 0.1 at 750°C to 1.0 at ~550°C. Rutherford ion backscattering measurements indicated good crystallinity over a wide range of growth conditions. TEM revealed that in thin films,

the lattice mismatch between Ge_xSi_{1-x} and Si layers can be accommodated by elastic lattice distortion rather than misfit dislocation formation.

2) Low Temperature MBE (1991)

Eaglesham et al. from AT&T Bell Labs in "Low Temperature growth of Ge on Si (100)" [34].

Heteroepitaxial MBE growth of Ge on Si (100) was studied at temperatures down to room temperature. They showed that growth is planar for all temperatures below 300°C, so the low temperature growth can be used near 200°C to suppress island formation without encountering the limited thickness effect. In contrast with planar growth at high temperatures with an As "surfactant", strain relaxation of these planar epitaxial layers occurs by normal dislocation introduction to give an array of predominantly edge misfit dislocations.

3) Very High Temperature MBE (1991)

Malta et al. from North Carolina State University in "Low-defect-density germanium on silicon obtained by novel growth phenomenon" [36].

Heteroepitaxial Ge on Si was grown using molecular beam epitaxy at a Si substrate temperature of 900°C. Electron microscopy results revealed a highly faceted interface, indicating localized Ge melting and subsequent local alloying with Si. Furthermore, this phenomenon is associated with extensive threading dislocation confinement near

the Ge/Si interface. Etch pit density measurements obtained on Ge heteroepitaxial films that had undergone interfacial melting were as low as 10^5 cm^{-2}.

4) Solid-Phase Epitaxy (1993)

Liu et al. from the California Institute of Technology (CIT) in, "Ge epilayer of high quality on a Si substrate by solid-phase epitaxy" [37].

An epitaxial Ge layer was grown by solid-phase epitaxy on an underlying $Ge_{0.82}Si_{0.18}$ seeding layer with a Ge-SiO_2 matrix positioned between them. To this end, (100) Si substrate with $Ge_{0.82}Si_{0.18}$ epitaxial layer was first oxidized in a wet ambient at 700°C for 30 min to transform an upper fraction of the epitaxial layer to an amorphous $Ge_{0.82}$ $Si_{0.18}$ O_2. The second annealing step was done at 700°C for 6h in a 95% N_2 + 5% H_2 ambient (forming gas) which reduces the GeO_2 layer to Ge which grows epitaxially by solid-phase reaction on the remaining $Ge_{0.8}2Si_{0.18}$ layer. A self-induced intermediate layer of epitaxial Ge with SiO_2 inclusions restricts the propagation of dislocations, resulting in a crystalline perfection of the overlying Ge epilayer superior to that of the $Ge_{0.82}Si_{0.18}$ template.

5) **Graded Buffer Layer and CMP (1998)**

Currie et al. from MIT in , "Controlling threading dislocation densities in Ge on Si using graded SiGe layers and chemical-mechanical polishing" [38]

A method of controlling threading dislocation densities in Ge on Si involving graded SiGe layers and chemical-mechanical polishing (CMP) was presented. This method has allowed them to grow a relaxed graded buffer to 100% Ge without the increase in threading dislocation density normally observed in thick graded structures. Compared to other relaxed graded buffers in which CMP was not implemented, this method exhibited improvements in threading dislocation density and surface roughness. They have achieved relaxed Ge on Si layers with threading dislocation densities of 2.1 x 10^6 $cm^{-2.}$

6. Two Step Growth and thermal Annealing (1999)

Luan et al. from MIT in, "High-Quality Ge epilayers on Si with low threading-dislocation densities" [39].

High-Quality Ge epitaxial layers on Si with low threading-dislocation densities were achieved by two step ultrahigh vacuum/chemical-vapor-deposition process followed by cyclical thermal annealing. On large scale Si wafers, Ge on Si with threading dislocation density of 2.3x10^7 cm^{-2} was obtained. Combining selective growth with cyclic thermal annealing produced an average threading dislocation density of 2.3x10^6 cm^{-2}

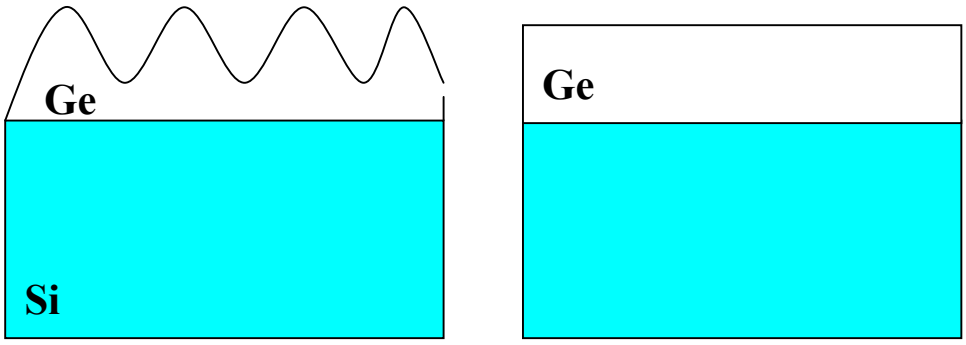
7) Nanoscale Ge seeds grown through a thin layer of SiO_2 (2004)

Li et al. from University of New Mexico, "Heteroepitaxy of high-quality Ge on Si by nanoscale Ge seeds grown through a thin layer of SiO_2" [40].

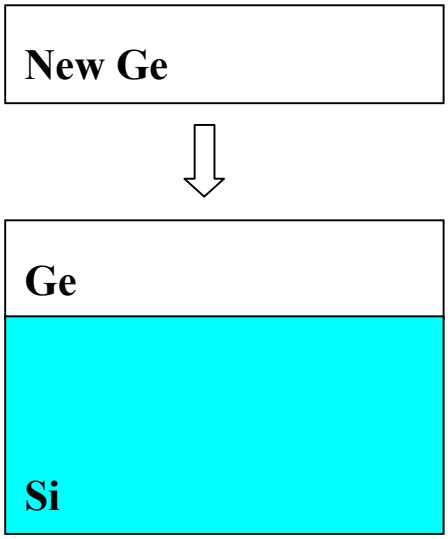
They demonstrated that high-quality Ge can be grown on Si covered with a thin layer of chemical SiO_2. When the oxidized Si substrate is exposed to Ge molecular beam, 7-nm-wide seed pads form in the oxide layer and "touchdown" on the underlying Si. Upon continued exposure, Ge selectively grows on the seed pads rather than on SiO_2 and the seeds coalesce to form an epitaxial lateral overgrowth (ELO) layer. The Ge ELO is free of dislocation network, but stacking faults exist near the Ge-SiO_2 interface. A fraction of these stacking faults propagate to the surface, resulting in etch pit density (EPD) less than 2 x 10^6 cm^2 . The high quality Ge ELO layer is attributed to a high density of nanoscale Ge seed pads interspaced by 2-12 nm wide SiO_2 patches.

4.2 Background and Motivation of Idea

In chapter 3, a 90% reduction in surface roughness of Ge layers grown on Si was achieved by hydrogen annealing. This low R_{rms} Ge layer can now be used as a starting substrate for subsequent Ge growth. ***Moreover, as described in this chapter later, the new growth mechanism will be homoepitaxy of Ge with no additional defects forming***. This is the fundamental idea of our growth technique of high quality layers of Ge on Si. A cartoon diagram of the method is shown in Figure 4.1. An additional Ge layer is grown on the low R_{rms} Ge layer without removing the wafer from the chamber. After that a final hydrogen bake is done to smooth out the final layer. This idea was given the name, "Multiple Hydrogen Annealing for Heteroepitaxy" or MHAH for short [41].



1. After Hydrogen Annealing



2. New Ge Starting Substrate; Homoepitaxy of Ge and thus no additional defects form

3. Final Hydrogen bake yields high quality Ge layer on Si. Method called "Multiple Hydrogen Annealing for Heteroepitaxy".

Figure 4.1: Cartoon showing Ge on Si growth method developed

4.3 Experimental Procedure

The initial MHAH Ge experimental recipe is described here. As before, the process starts with the pre-diffusion clean of a standard Si wafer. This clean was described in chapter 3 table 3-1. The same growth and annealing recipe that yielded 200nm of smooth 2.5 R_{rms} Ge will be the new starting substrate. The growth recipe is described in tables 3.2-3.4. Without taking the wafer out of the chamber after the growth, the temperature is ramped down from the hydrogen annealing temperature of 825°C to the Ge growth temperature of 400°C. After the temperature has stabilized, the germane gas is turned on (same conditions as first growth step) and the deposition is carried out for 15mins. The goal is to grow 200nm of homoepitaxial Ge on top of the original 200nm layer. Following the growth, the temperature is again ramped back up to hydrogen bake temperature of 825°C and annealed for 1hr. Table 4-1 is a modified version of table 3-4 beginning from step 17 after the first hydrogen bake. It includes the 2^{nd} growth and 2^{nd} anneal for the MHAH process.

	Step 17	**Step 18**	**Step 19**	**Step 20**	**Step21**
Step Name	**BAKE**	TEMP	STABDEP	DEPOSIT	TEMP CHECK
Duration	**60:00**	300	90	15:00	5:00
Token					
Center	**825**	400S	400	400	825S
Dep/Vent	**VENT**	VENT	VENT	DEPSOSIT	VENT
N2/H2	**50HR**	22H	22H	22H	22H
Rotation	***SAME**	*Same	*SAME	*SAME	*SAME
HCLHI	**0V**	0V	0V	0V	0V
HCL	**0V**	0V	0V	0V	0V
SiH4	**0**	0	0	0	0
Germane	**0**	0	30	30	0
V_pressure	**80**	80	10	10	80R
VentMatch	**1**	1	1	1	1

	Step 22	**Step 23**	**Step 24**	**Step 25**	**Step 26**	**Step 27**
Step Name	BAKE	POSTPRG	HOMSUS	UNLOAD	TMP RMP	END
Duration	60:00	45	15	.1	180	1
Token				UNLOAD		END
Center	825	825	825	820	800	800
Dep/Vent	VENT	VENT	VENT	VENT	VENT	VENT
N2/H2	50HR	20H	10HR	10H	20H	20H
Rotation	*SAME	10R	0	0	0	0
HCLHI	0V	0V	0V	0V	0V	0V
HCL	0V	0V	0V	0V	0V	0V
SiH4	0	0	0	0	0	0
Germane	0	0	0	0	0	0
V_pressure	80	ATM	ATM	ATM	ATM	ATM
VentMatch	1	0	0	0	0	0

Table 4.1: Modified growth recipe that includes 2nd growth and 2nd annealing for the MHAH Ge process. Modified process starts after step 17 from table 3.4

4.4 Characterization of Layers

4.4.1 Transmission Electron Microscopy

One of the most important methods used to characterize heteroepitaxial Ge layers grown on Si is transmission electron microscopy (TEM). Both plan-view and cross-section TEM can be used depending on the application. As the name suggests, cross sectional TEM is used to view the entire cross-section of layer, from Ge/Si interface to Ge surface. The sample preparation needed for cross section TEM is long and tedious. The sample must be thinned down until it is transparent to light. After that the sample is ion milled thin enough to allow electrons to be transmitted locally through a region of interest during microscopy. Despite the fact that the preparation is difficult, a plethora of information is obtained from viewing this sample. Moreover, due to the high resolution of the TEM and the ability to orient the sample in the proper k-space, dislocations can be viewed and studied effectively. High resolution cross sectional TEM can be used to see at the atomic level and study interfaces effectively. The only limitation is the size of the sample that will limit the visibility or resolution of dislocations. For example, if one has a sample with a dislocation density of $1x10^7$ cm^{-2} there is a very high probability a dislocation will not appear in the sample viewing area.

In order to make the dislocation visible with the goal of being quantified, plan-view TEM is used. In plan-view the viewing angle is from the top and thus a larger area of the sample can be examined. In addition, sample preparation is simpler since

thinning of the sample is done from the bottom up towards the surface. This method is very effective in quantifying the number of dislocations per are as they are visible through the strain contrast they produce in the image.

4.4.2 Etch Pit Density

Another method used to characterize the layers is chemical etching. In this method, a chemical solution that etches Ge is used. Moreover, the solution must etch the dislocations at a faster rate than Ge. This differential etching will create etch pits. The etch pits can then be viewed by using an optical microscope with one etch pit signifying one dislocation. The major limitations of this method are threefold. First, the size of etch pits could make optical microscope viewing very difficult. Second, the fast etch rate of solution makes it difficult to characterize thin Ge layers. Third, dislocations close to each other give rise to a single etch pit, giving an underestimation of the dislocation density. Nonetheless, this method along with plan-view TEM can give upper and lower bounds and thus was used to determine the dislocation density of the layers.

4.4.3 Results

Using the 400nm MHAH-Ge layer described in the section 4.3 various, TEM images were taken. For comparison, a 1μm as grown Ge layer on Si is included to highlight the differences from traditional SK growth (chapter 2). Figure 4-2 presents a cross sectional TEM of the 1 μm as grown Ge layer grown at 400°C. The image clearly shows that dislocations have formed at the Ge/Si interface and have thread to

the surface. Figure 4-3 on the other hand, presents the cross sectional TEM image of a two step *MHAH* growth that yielded a ~ 400 nm Ge layer. The image shows that near the surface the dislocation density is reduced while near the Ge/Si interface the dislocation density is very large. In addition, a finite dimension above the Ge/Si interface the dislocation density is below the resolution limit of the TEM since no dislocations are visible. This means the dislocation density is reduced near the surface during the double growth and double annealing. In addition to TEM, X-ray diffraction (XRD) is used to confirm the layer was single crystal and fully relaxed. Figure 4-4 gives the XRD result for the ~400 nm epi-Ge layer on Si. It shows the presence of the Ge and Si peaks, indicating that the layer has a single out-of-plane crystallographic orientation. The peak locations are consistent with a fully-relaxed Ge (100) epi-layer on Si (100). The Ge peak broadening indicates silicon diffusion from the substrate during the high temperature hydrogen anneals. 1×1 μm^2, 10×10 μm^2 AFM scans of the surface yielded a final surface roughness of 0.218 nm, and 2.5 nm, respectively [42].

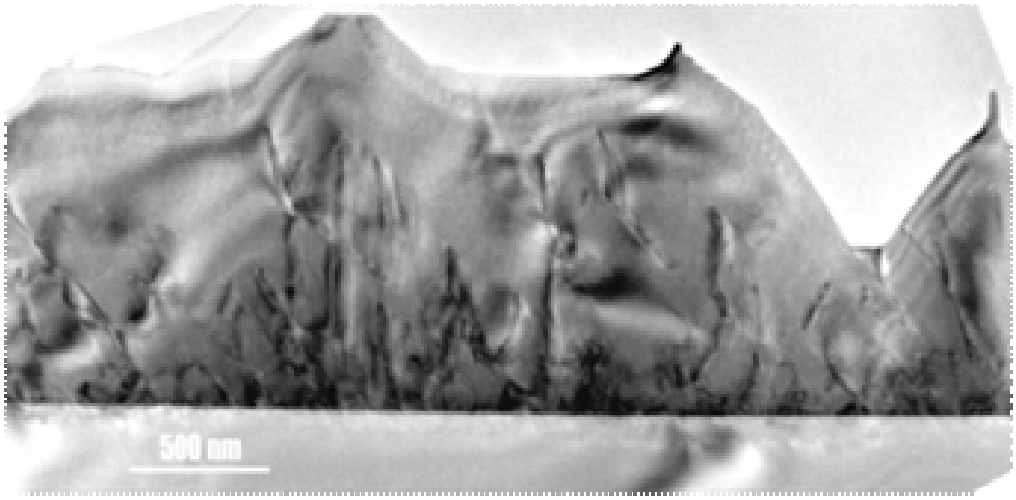


Figure 4.2: Cross-section TEM of as-grown Ge layer grown on Si. Misfit dislocations form at the Ge/Si interface and propagate to the surface as threading dislocations from the SK growth model

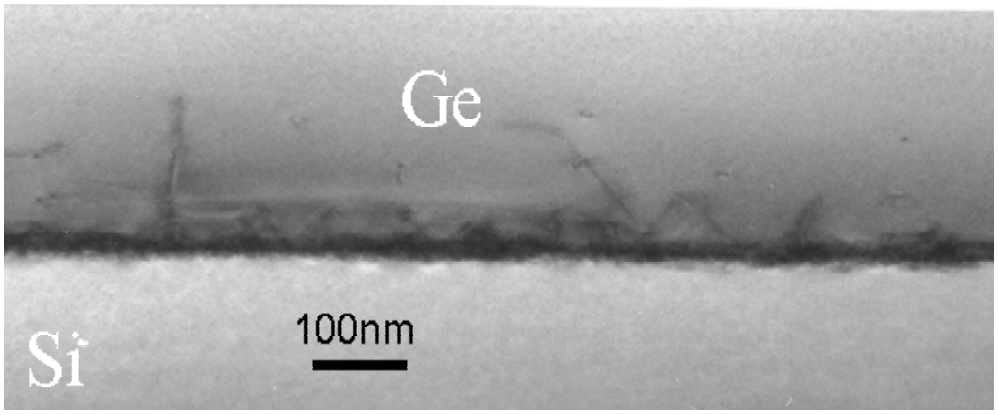


Figure 4.3: Cross-sectional TEM image of ~ 400 nm heteroepitaxial-Ge layer on Si grown by the MHAH method. Dislocations are concentrated near the Ge/Si interface.

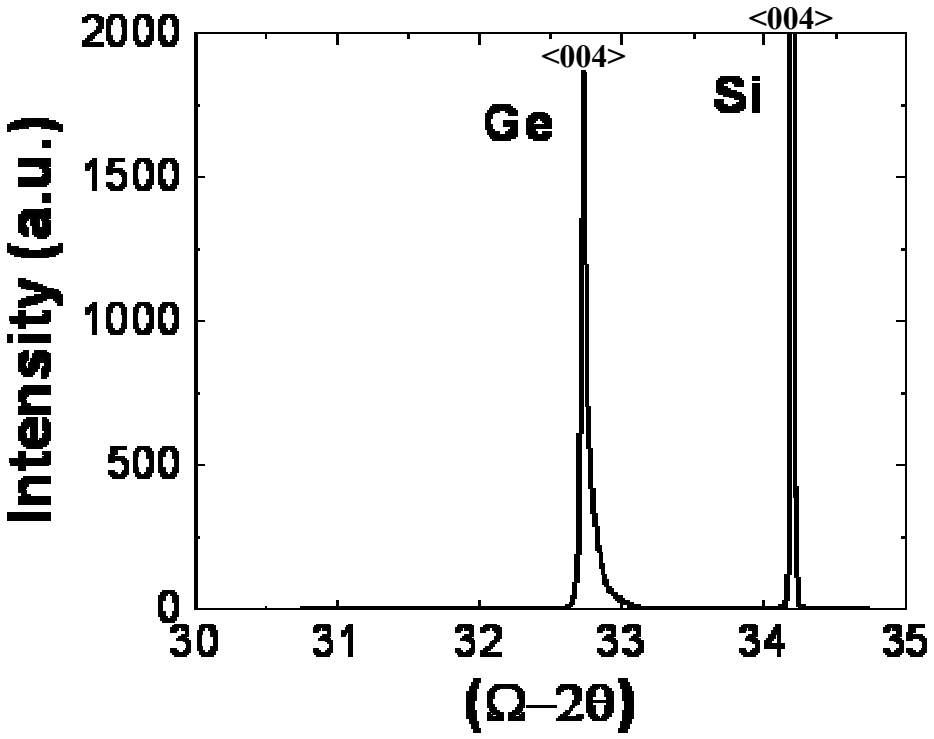


Figure 4.4: X-ray scattering intensity for 400 nm MHAH Ge layer on Si using XRD. The epi-Ge layer is single crystal and fully-relaxed. Ge peak broadening indicates Si diffusion that helps assist the Ge layer relaxing.

In order to quantify numerically the defect density, plan-view TEM was first used. Figure 4-5 shows the plan view-TEM image of the 400nm sample. Since the layer is thin, the entire layer from Ge/Si interface to Ge surface is visible. The Ge/Si interface is determined by using a magnifying glass and finding the moiré fringes that indicate the interface. The arrow indicates the direction of increasing thickness towards the top surface. It is immediately clear from the image that the dislocation density is much larger near the Ge/Si interface and decreases dramatically near the top surface. Also visible are locations near the surface with no dislocations. From this plan-view TEM image, the defect density on top of the layer 200nm was extracted to be 2×10^{8} cm^{-2}. Also, the dislocation density vs. depth was determined and plotted in figure 4-6. It should be noted that since the sample is thin, defect etching cannot be used due to the fast etch rate of the layer.

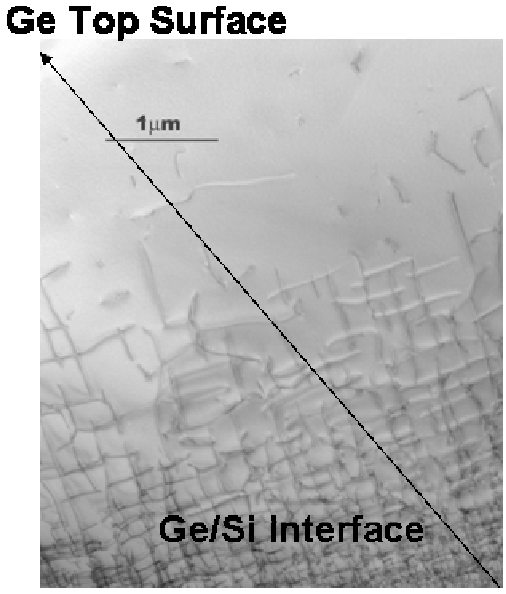


Figure 4.5: Plan view TEM image of the same layer. As the TEM sample becomes thinner (indicated by arrow), the lower part of the film is increasingly milled away and only the upper layer of the film, showing drastically reduced defect density, remains.

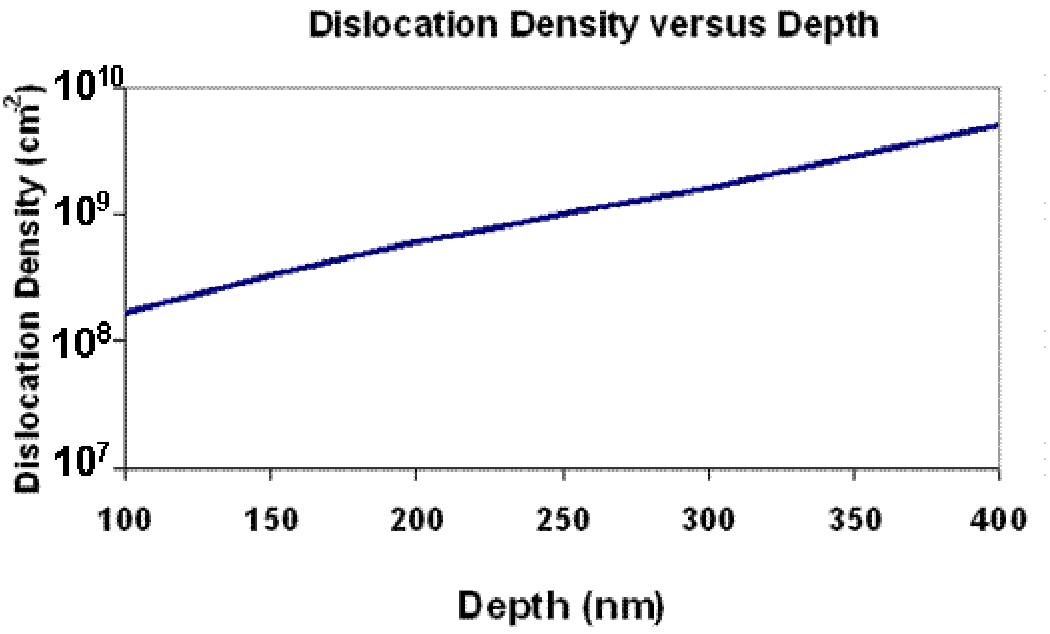


Figure 4.6: Dislocation density vs. depth from plan view image of figure 4.4

In order to further reduce the dislocation density, a modified MHAH growth recipe was used that included three growth steps and three anneals. The process was done starting with a standard pre-diffusion clean of standard Si wafer. After the 2nd growth and 2nd anneal as described before, the temperature was ramped down from the annealing temperature. In order to increase the growth rate, the growth temperature was increased to 460°C for 15min and then 500°C for 15min. After that a final hydrogen anneal was carried out. This three growth three annealing MHAH process yielded a 4.5 µm layer. Growth of the 4.5 µm layer reduced the dislocation density to around (5-7)×10^7 cm^{-2} as confirmed by plan view TEM as shown in figure 4-7. In addition, defect chemical etch treatment was preformed since the layer was thick.

The etchant, which consisted of CH_3COOH (67 ml), HNO_3 (20 ml), HF (10 ml) and I_2 (30 mg), was incubated for two days. Figure 4-8 is a plan-view optical micrograph image that shows etch pits on a 4.5 μm thick Ge epi-layer. The defect density was counted to be between 1×10^6 cm^{-2} to 1.4×10^6 cm^{-2}. This low threading dislocation density is smaller than what was determined by plan-view TEM. The EPD/TEM difference can be attributed to the resolution limit of the optical microscope. If two etch-pits overlap it becomes difficult to resolve individual pits.

In addition to TEM, Rutherford Backscattering Measurements (RBS) indicated the thin ~200nm Ge layer was 91% Ge while the ~400nm Ge layer was 96% Ge and the 4.5 μm epi-Ge layer yielded 100% Ge. The Si-Ge interdiffusion which occurs during the hydrogen annealing helps to relax the misfit strain, particularly in the thin layers.

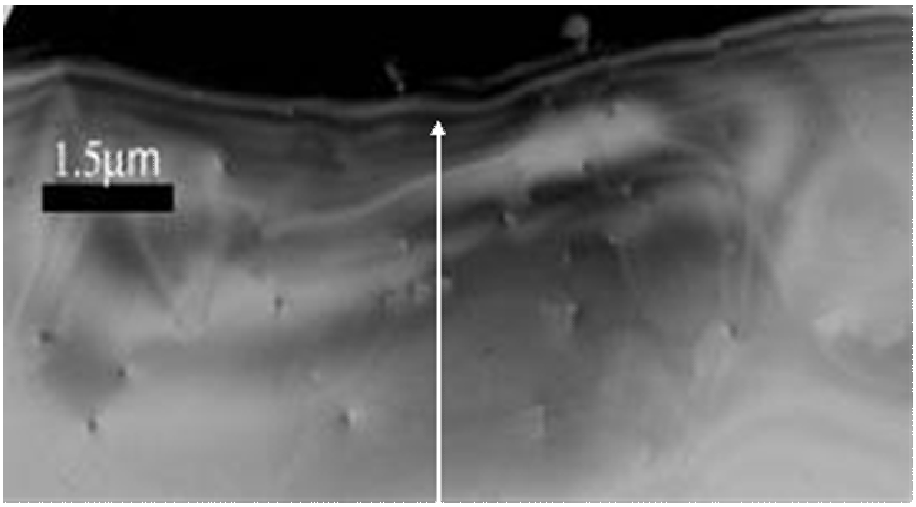


Figure 4.7: Plan view TEM image of 4.5 μm layer (200 nm from the surface (arrow). Dislocation density further was reduced to around (5-7)×$10^7$$cm^{-2}$.

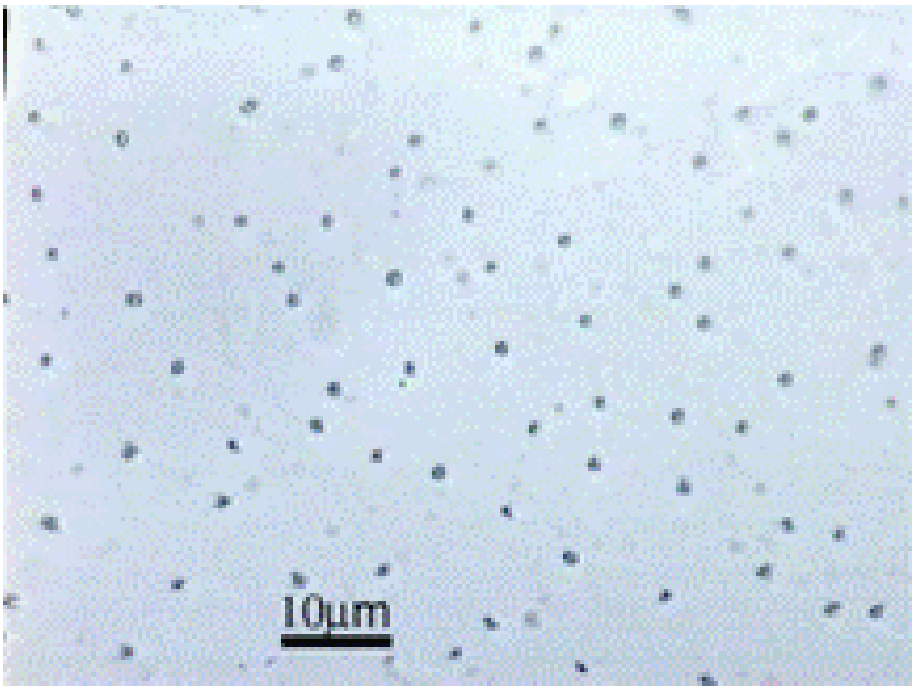


Figure 4.8: Optical Microscope 100× plan view image after defect etch: Threading Dislocation Etch Pits (EPD): $1 \times 10^6\,cm^{-2}$

In addition, we repeated the MHAH experiment with our colleague Takao Yonehara at Canon using an industrial reactor. This growth recipe carried out was a double growth and double anneal with the 2nd annealing done at 700°C. A 50x reduction in dislocation density was obtained form the as-grown case with final density of $1.5x10^7 cm^{-2}$. This density obtained is lower than that obtained using the Stanford epitaxial reactor, likely because of the use of a better-controlled industrial reactor. The plan-view TEM images are show in figure 4-9.

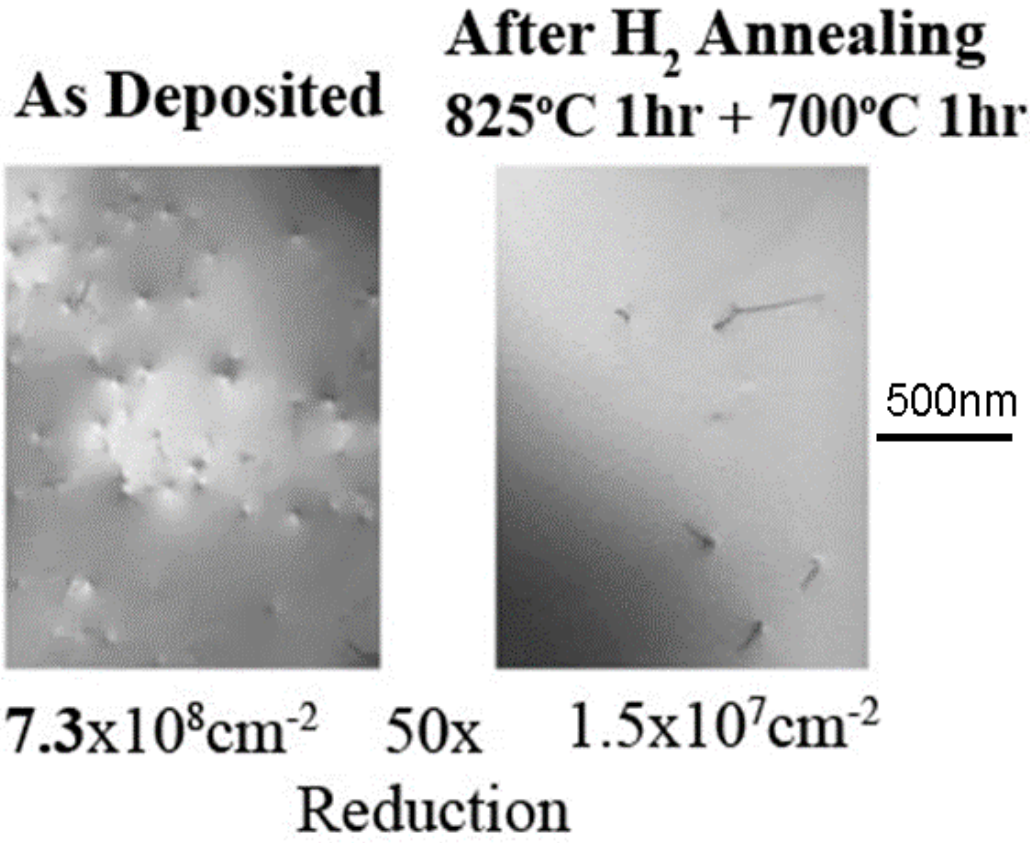


Figure 4.9: Plan-View TEM image of MHAH method repeated in industrial epi-reactor form Canon. 50X reduction in dislocation density obtained.

4.5 Model

As shown in the previous section, the threading dislocation density is reduced near the surface during the multi-step growth and hydrogen annealing. The main mechanism that causes the reduction is dislocation motion. During annealing, it is well understood that dislocations move with a velocity dependent on several factors.

Equation 4.1 describes the dislocation velocity in the Ge layer determined experimentally [43]

$$V_{dislocation} = V_0 \cdot \sigma_{exc} e^{-\frac{E_v}{kT}} \qquad \textbf{(4.1)}$$

In equation 4.1, V_o is a constant, σ_{exc} is the excess stress driving dislocation motion and E_v is the energy barrier to dislocation glide. σ_{exc} is a function of the thermal expansion coefficients, temperature, Possion Ratio and Young's modulus of the film and substrate. The thermal stress between Ge and Si is induced due to the difference in coefficients of thermal expansion between Ge and Si. The excess stress is the thermal stress minus the dislocation line tension stress. Since dislocation line tension stress is not strongly related to temperature and the much smaller compared to the thermal stress, thermal expansion stress dominates the equation. As a result, equation 4.1 indicates there are two conflicting regimes for dislocation motion. At low temperature, the dislocation velocity is limited by the energy barrier. As a result, the velocity increases with temperature. At high temperature however, the limitation is the thermal expansion coefficient stress as described in reference 4-8. Figure 4-10 is a plot of dislocation velocity vs. temperature from reference 4-8 on relaxed Ge layers grown on Si. The peak velocity occurs at 825°C, which is coincidently the temperature used in the initial hydrogen bake experiments (see chapter 3).

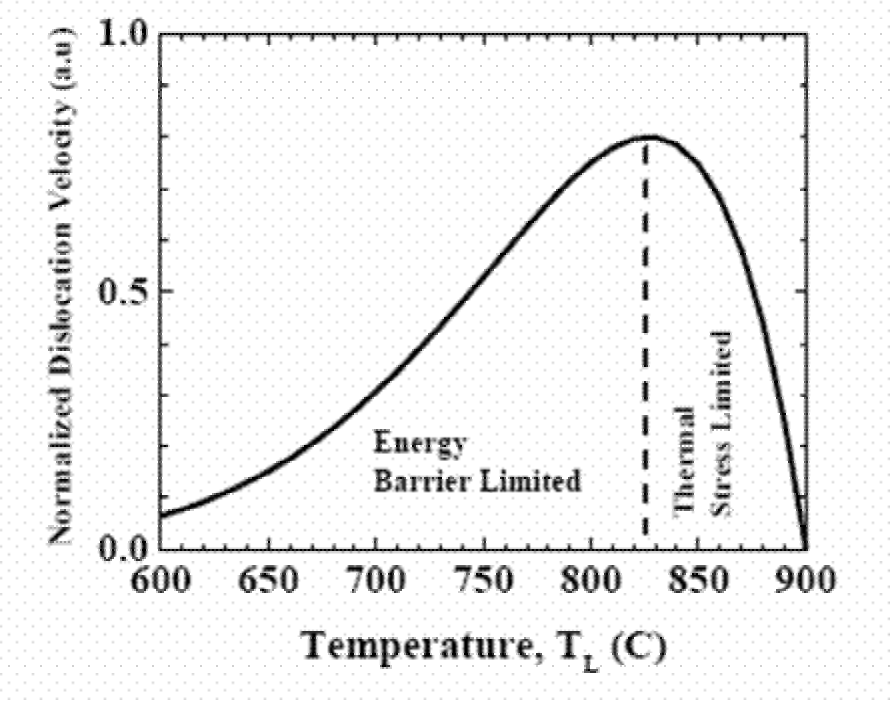


Figure 4.10: Ge dislocation velocity versus temperature from reference 4.9

Dislocation motion in the layer leads to various mechanisms that lead to a reduction in the dislocation density. First, threading of dislocation arms can move out of the film towards the edges. Second, dislocations can interact with each other during their motion. This leads to the concept of annihilation which has been studied mathematically [42]. It has been shown that the longer the annealing time the higher the probability that the dislocation can be annihilated. However, as annealing continues, the dislocation density drops, reducing the dislocation annihilation rate. Thus there appears to be finite limit to the degree of dislocation reduction achieved by hydrogen baking. Figure 4.11 shows the cross section cartoon of dislocation motion and the effects per se.

In addition to dislocation motion, the MHAH method takes advantage of two other important mechanisms to reduce the dislocation density further. The idea of double growth and double anneal adds a homoepitaxial growth feature. This disallows any additional defects from forming. Moreover, the final hydrogen bake will further reduce the dislocation density. Furthermore, the MHAH process growth of thick layers can reduce densities even further. The MHAH method can be modified for the thickness desired for the individual application.

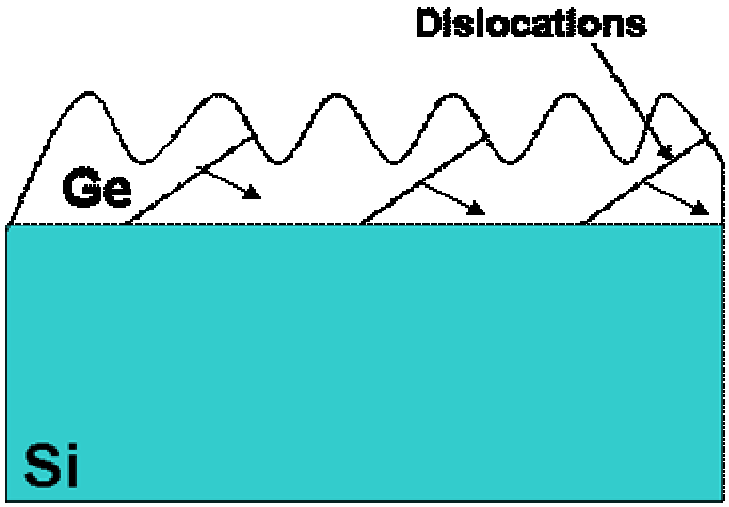


Figure 4.11: Cross section cartoon of dislocation motion during annealing.

The complete *MHAH* process flow and model is shown schematically in Fig. 4.12

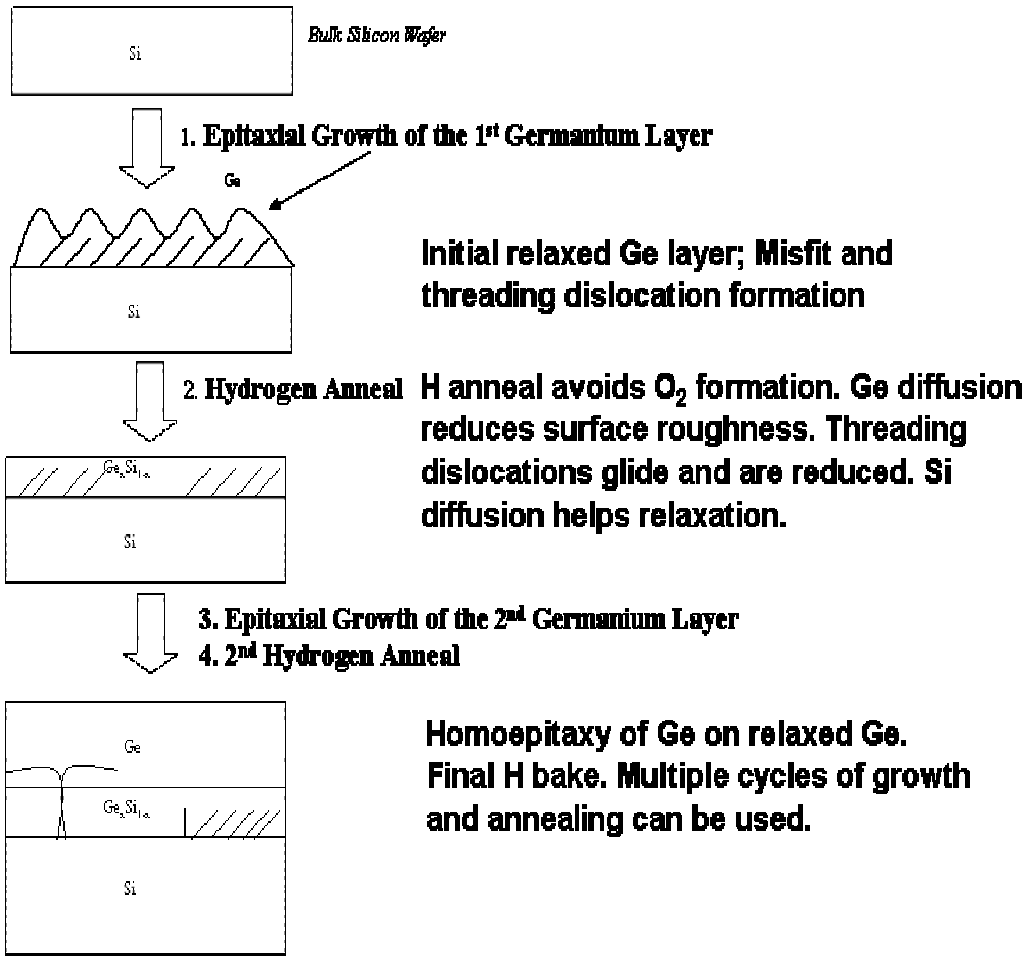


Figure 4.12: Complete MHAH growth model

4.6 Conclusion

In conclusion, chapter 4 began with a summary of the state of art of the Ge on Si system. Most of the techniques published required very complicated SiGe grading, CMP, UHV double growth, very long annealing times, or very fancy selective growth process. Our MHAH technique uses straightforward multiple steps of growth and hydrogen annealing. We found that threading dislocations are confined to the Ge/Si interface. Moreover, dislocation density as low as $1x10^{7}cm^{-2}$ was achieved by using the MHAH method. Finally a model explaining the growth mechanism was presented.

Chapter 5 will focus on the electrical characterization of the MHAH-Ge layers grown.

CHAPTER 5

Electrical Characterization

5.0 Abstract

This chapter highlights the various electrical devices fabricated on the Ge layers grown using the MHAH technique described in chapter 4. The results will provide an indication of the quality of the layers and their suitability electrically. The devices fabricated include MOSCAPS, a pMOS transistor, and a MSM photodetector. In addition, high-κ/metal gate compatibility is also demonstrated. The fabrication process and electrical results will be presented for each device fabricated.

5.1 Introduction

To date, heteroepitaxial Ge based electron devices have focused more on photodetectors due to the more lenient dislocation threshold requirement [5-(1-2)]. Only a few publications on Ge-based CVD grown Ge-MOS transistors have been reported since dislocation and surface roughness make it a very serious challenge. Also as discussed in chapter 2, one of the the main challenges for Ge based transistors is the gate dielectric. GeO/GeO_2 is unstable and soluble in water so they cannot survive a CMOS process. As a result, most of the Ge transistor work has used a Si cap to avoid the Ge dielectric challenge or a SiGe graded layer to avoid the 4.2% lattice mismatch.

As discussed in the previous chapters, dislocations can dominate the Ge growth due to the 4.2% lattice mismatch. The electrical characterization is therefore important to assess weather the grown Ge layers can behave electrically as close as possible to bulk Ge. The following sections highlight the electrical devices fabricated on the MHAH Ge layers and include a detailed electrical characterization of the layers.

5.2 MOSCAP

5.2.1 MOS CAP Fabrication

The smoother Ge surface we achieved enabled us to evaluate the electrical quality by fabricating MOSCAPS. MOSCAP CV characteristics can give a good understanding of the quality of the layer and more importantly the quality of the dielectric/Ge

interface. MOSCAPs were fabricated on 4.5μm MHAH-Ge layers. The dielectric used in the work was Germanium Oxynitride (GeO_XN_Y) that was developed by Dr. Chi On Chui during his PhD research in our group [5]. It was shown that (GeO_XN_Y) is stable and could survive a CMOS process.

The fabrication process begins with a 4.5um MHAH-Ge layer that was described in chapter 4. The main difference is that the growth recipe from chapter 4 was altered to allow *in-situ* doping of the substrate. The n-type doping species available is phosphorous while p-type is boron in SNF. N and P -type Ge layers of $1x10^{17}cm^2$ were achieved by in situ CVD doping and later confirmed by the CV measurement.

The first step of the MOS CAP fabrication process is the passivation of the surface prior to the gate dielectric growth. Traditionally for Si based devices, a complete pre-diffusion clean is used before the gate dielectric growth (chapter 3). This procedure cannot be used for Ge since sulfuric acid used in cleaning Si etches Ge. For Ge, the chemical treatment used is "cyclical-HF", which includes multiple cycles of 50:1 HF solution and DI water. The procedure uses a total of twelve fifteen-second intervals between the DI water and HF treatments. After the clean the wafer is ready gate dielectric growth. Immediately following the clean and dry, the wafer is loaded into a rapid thermal processing (RTP) system to insure that the native oxide does not form. GeO_xN_y was grown in the RTP system using ammonia (NH_3). The complete detailed recipe can be found in ref. [5]. This yields an 80Å thick layer of Ge oxynitride. The next step is to immediately cap the sample with a gate electric. Instead of doing a complete lithography process, a shadow mask method is used. In

the shadow mask method, a mesh is mounted on the sample that consists of tiny circles of various radii. After the mesh is mounted, a 500 Å tungsten (W) electrode is deposited by room temperature e-beam evaporation through a shadow mask, leaving a tungsten circular gate. A backside aluminum contact is also evaporated to insure proper substrate contact during the measurement. The samples are finally un-mounted and a 30min 300°C forming gas anneal (FGA) concludes the process. Table 5.1 shows the complete fabrication process for the MHAH-Ge MOSCAPS.

Step	Comment
MHAH Ge Growth	To growth low defect density Ge on Si
Ge surface cleaning	Cyclical HF. Multiple cycles of (50:1) HF followed by DI water for a total of twelve times each fifteen seconds
GeO_XN_Y Growth	RTP System using NH_3 at 600°C
Gate Metal	W e-beam evaporation through a shadow mask
FGA	Forming Gas Annealing 300°C to passivate the Ge/GeO_XN_Y interface

Table 5.1: MHAH-Ge MOSCAP process flow.

5.2.1 MOSCAP Results

Before measuring the CV characteristics of the fabricated capacitors, a cross section TEM was taken to see the quality of the Ge/GeO_xN_y interface. Figure 5.1 shows high resolution cross sectional TEM of $Ge/GeO_xN_y/W$ stack showing the Ge single crystal lattice, Ge/ GeO_xN_y interface, GeO_xN_y amorphous layer and W gate. Both n-p type MOSCAPs were fabricated. Figure 5.2 and 5.3 present bi-directional

high frequency CV characteristics measured at 100 kHz and 1 MHz, showing negligible hystersis or frequency dispersion. CV hystersis is an indicator of the level of interface states (through interface charge trapping) that can eventually degrade the MOSFET mobility. This indicates both the high quality of the MHAH-Ge layer and the high quality of the MHAH-Ge/GeO_xN_y interface. In addition, figure 5.4 shows a direct comparison with CV characteristics of a bulk Ge MOSCAP, which displays the bulk-like electrical quality of the MHAH-Ge. ***These Ge layers have a dislocation density of around 1.5 x $10^7 cm^{-2}$ indicating that the Ge layer begins to electrically approach bulk quality***. Finally, the D_{it} vs. Φ_s relation was extracted using the "high-low" technique as shown in figure 5.5 [48]. The figure shows an asymmetry with higher D_{it} in the conduction band which, may explain why researchers have found Ge nMOS mobility to be low [49].

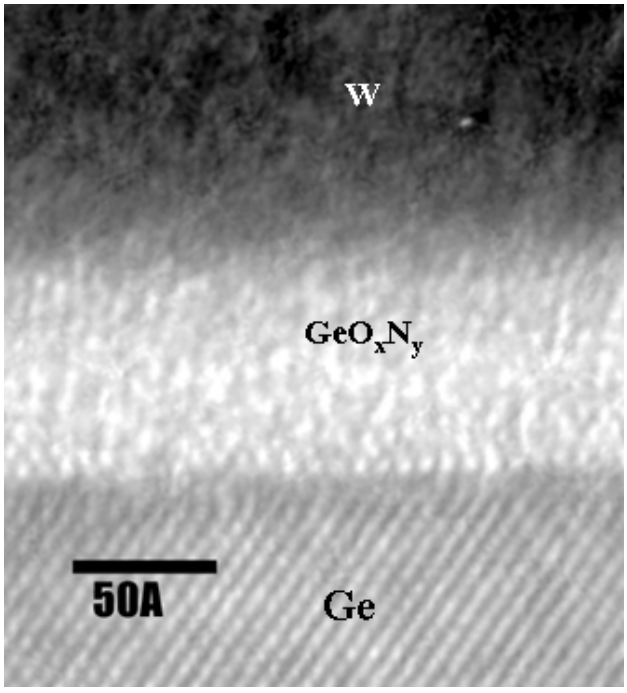


Figure 5.1: High Resolution Cross Sectional TEM of GeO_xN_y/Ge stack showing the Ge single crystal lattice and high quality interface**.**

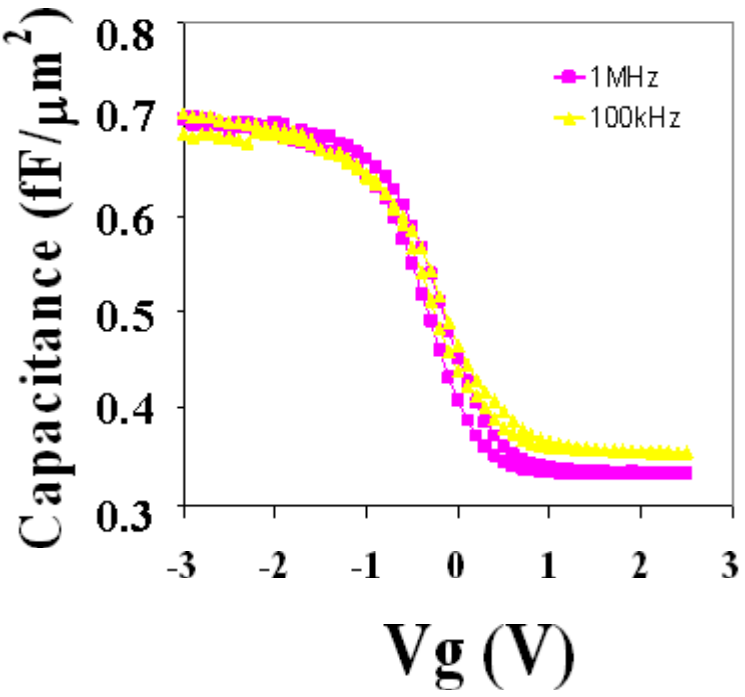


Figure 5.2: Bi Directional CV Characteristics of Ge/GeO_xN_y MOS-caps on p-type 1.5µm MHAH Ge Layer.

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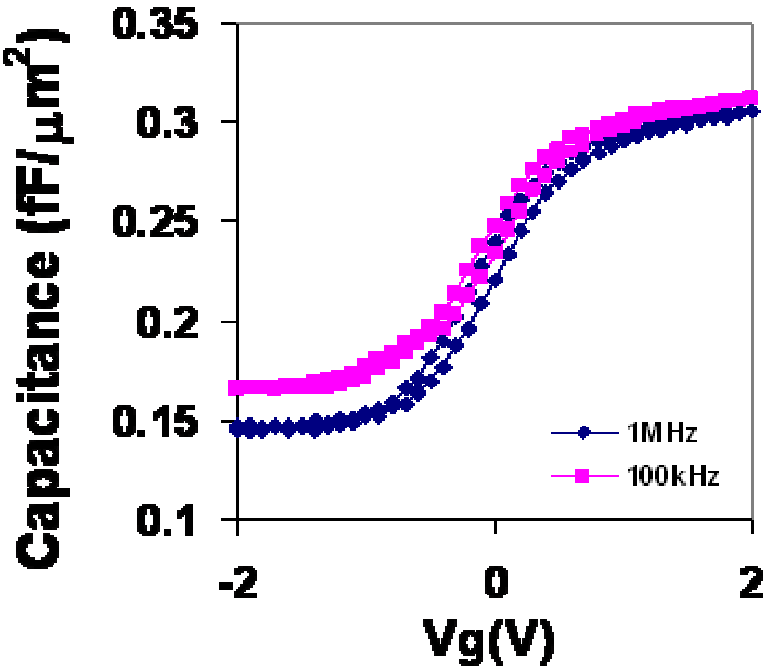

Figure 5.3: Bi Directional CV Characteristics of Ge/GeO_xN_y MOS-caps on p-type 1.5µm MHAH Ge Layer.

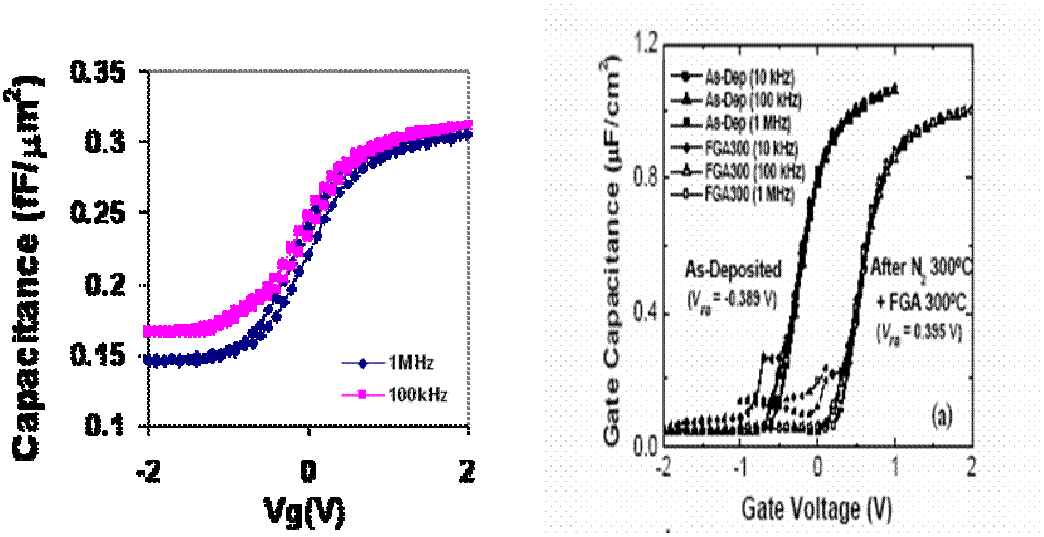

Figure 5.4: Comparison between MHAH-Ge CV and Bulk Ge CV;

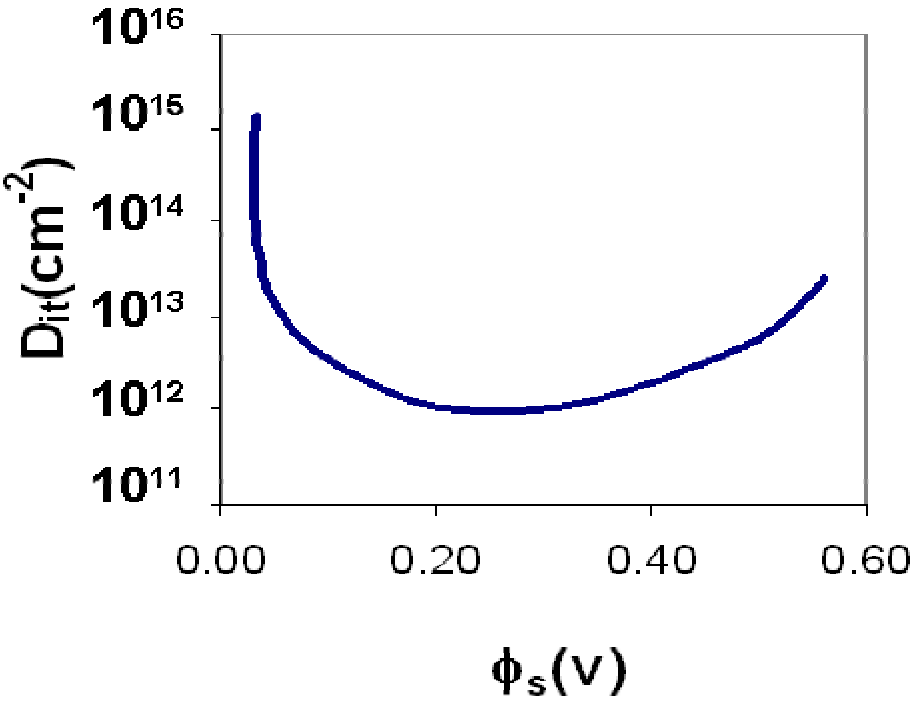

Figure 5.5: $D_{it}(cm^{-2})$ vs. $\Phi_s(V)$ showing assymetry which may indicate why Ge NMOS mobilty is degrated

In addition to the 4.5µm layer, MOS caps were fabricated on the 200nm Ge layer to understand the role of dislocations on the electrical results. The 200nm layer differs from the 4.5µm in that it has dislocation density is larger than 1 x 10^8 cm^{-2} and the Si/Ge interface is much closer to the top Ge surface. Figure 5.6, which presents the bi-directional high frequency CV characteristics (100 kHz and 1 MHz), shows negligible hystersis, indicating the high quality of the GeO_xN_y interface. From the 100 kHz sweep, however, we observed two kinks near inversion that suggests the presence of a finite amount of interface states resulting from the much higher dislocation density in these layers. The dislocations that affect the electrical results can either be at the GeO_xN_y/Ge interface, in the main Ge layer, or near the Si/Ge interface. [30].

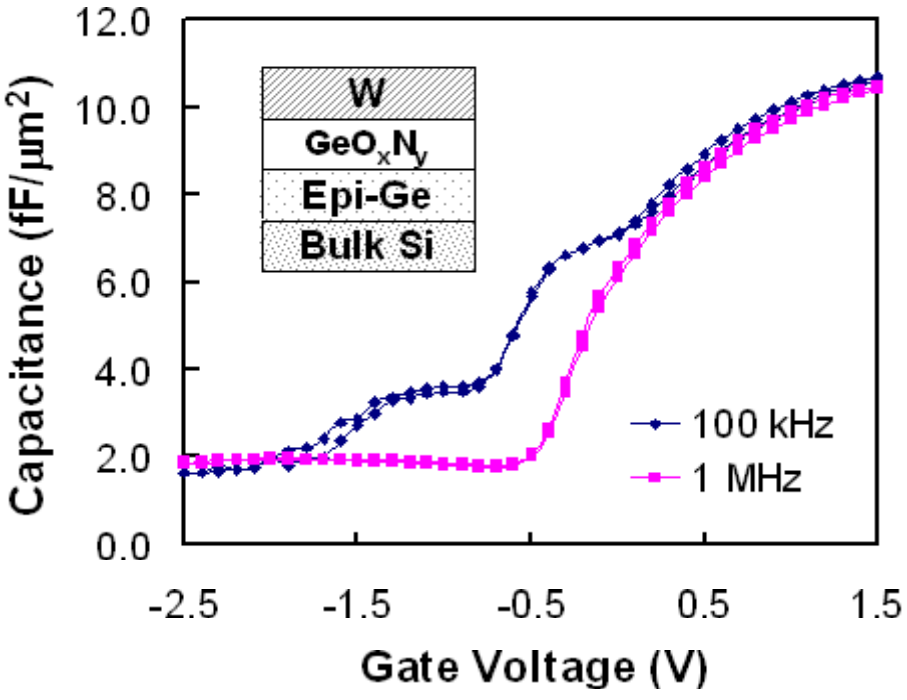

Figure 5.6: Bi-directional CV characteristics of MOS capacitor structure using a 200nm MHAH-Ge layer with 1x10^8 cm^2 dislocation density; the two kinks in inversion are the result of higher dislocation density compared to the 1.5µm based caps.

5.3 p-MOS Fabrication

5.3.1 Ge PMOS Process Flow

The starting substrate is a 400 nm high quality MHAH grown Ge layer on Si as described in chapter 4. This was grown using a double growth/annealing MHAH cycles. Before this can be done the Ge surface must be passivated using a cyclical HF clean, which we described in section 5.3.2. The first step in the transistor fabrication is field isolation. Field isolation was done in a rapid thermal processing (RTP) system using ammonia to grow to an 8 nm thick GeO_xN_y layer at 600°C followed by deposition of 400 nm thick LPCVD SiO_2 (LTO) . This field oxidation has been shown to be much better in suppression of leakage than just the use of LTO. Following the field isolation, lithography is performed to open active area. The active area is etched open by wet HF etching. Following this the photoresist is removed. If the active area was made of Si the photoresist could be removed by standard chemical etching using "piranha", which contains H_2S0_4. However piranha etches Ge so it cannot be used in our Ge processing. The only method that can be used is ashing. After ashing is done, the surface is cleaned prior to gate dielectric growth. This is done with cyclical HF cleaning. The wafer is then loaded in the RTP system. 8 nm GeO_xN_y was grown at 600°C followed by 10 nm LTO deposition at 450°C as the gate dielectric yielding 14 nm equivalent oxide thickness (EOT). The LTO cap was used to suppress gate leakage that would make it very difficult to extract mobility.

Immediately following the LTO deposition, an in-situ boron doped $Si_{0.75}Ge_{0.25}$ gate was grown by CVD at 500°C to form gate electrode. This gate was used rather

than un-doped p+ poly-Si since the gate doping in $Si_{0.75}Ge_{0.25}$ is activated during the CVD growth. In the poly Si case, the activation would have to be done after the source/drain implant at very high temperature above the thermal budget of GeO_xN_Y. After deposition, the gate is patterned by dry etching. After gate definition and self aligned source/drain boron (B) implant, a 450 °C Rapid Thermal Anneal (RTA) was used to activate the dopant. Contacts were defined by LTO/Aluminum based on the standard process from EE410 [50]. Finally a 300°C, 30min forming gas anneal concluded the process. Table 5.2 shows a complete process flow of the PMOS transistor. Figure 5.7 is a cross section of the fabricated transistor.

Step	Description	Process Details
0	Starting Substrate	MHAH-Ge
1	Field Isolation	Cyclical HF->GeO_xN_y[5]->LTO400 ~22min 4000Å
2	Active Area Etch	6:1 Buffered HF ~71seconds
3	Photoresist Removal	"Ash" resist with Gasonics Resist Strip recipe 041
4	Gate Oxide Deposition	Cyclical HF; RTA in NH_3 to grow GeO_xN_y followed by LTO450P (O_2=87, SiH_4=7.8, P=250mT)
5	Gate Deposition	CVD $Si_{0.75}Ge_{0.25}$ in-situ doped p-type at T=500°C
6	Gate Etch	Plasma Etch using CH_4 in Drytec ~139 seconds
7	Source/Drain Implant	p-type source drain $BF_2$49 80keV at $1x10^{15}cm^{-2}$
8	Activation	450 °C Rapid Thermal Anneal (RTA) for 10 seconds
9	Contact Definition	LTO400 6000Å followed by plasma contact etch using CH_3/O_2
10	Metallization	Aluminum (1000Å) by sputter deposition
11	Forming-Gas Anneal	300°C for 30min

Table 5.2: PMOS MHAH-Ge process flow and details.

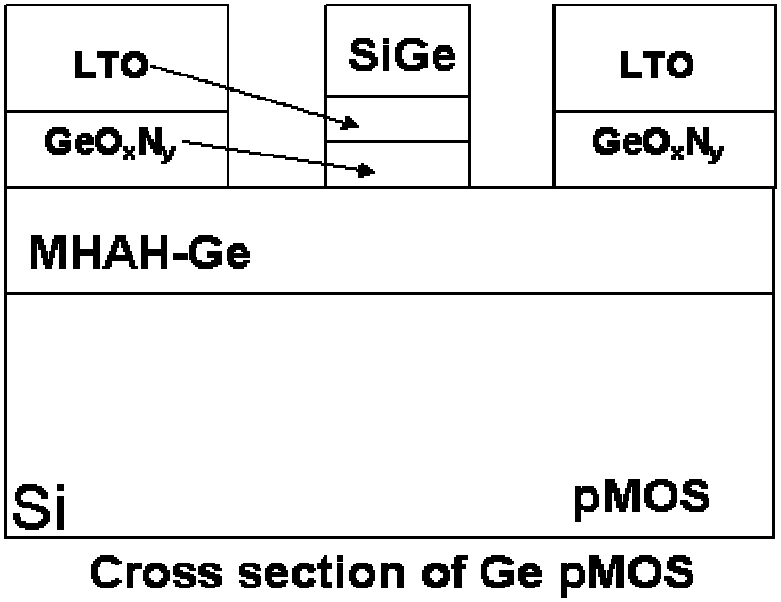

Figure 5.7: Cross section cartoon of fabricated MHAH-Ge PMOS.

5.3.2 PMOS Results and Discussion

In order to characterize the fabricated pMOS transistor, I-V measurements and mobility extraction were carried out [51]. Figure 5.8 and 5.9 are the I_s-V_s and the I_d-V_d respectively of the p-MOSFETs. The W/L ratio for both devices is 100µm/6µm. In the measurement, V_d and V_s were swept from 0 to -1 V while V_g was stepped in 0.1 V increments from 0 to -1.6 V. It is to be noted that the gate current from these devices was minimal. Comparing the I_d-V_d and the I_s-V_s curves one can observe a small asymmetry in the curves originating at the drain side, which implies leakage current. Since the gate current is small, we believe this leakage current is largely due to drain to substrate leakage resulting from electrostatic interaction between the drain depletion

region and confined defect region. Figure 5.10 shows the substrate and gate current as a function of drain voltage. It can be seen that as drain voltage increases the substrate current increases independent of V_g while the gate leakage decreases and is on average less than 6 x 10^{-6} μA/μm. Thus the leakage current seen on the drain side is largely due to drain to substrate leakage resulting from either junction leakage due to small band gap of Ge or from electrostatic interaction between the drain depletion region and confined defect region. Finally, it should be noted that one would expect this leakage path based on analytic calculations of the drain depletion width. Fabrication of the transistors on a thicker MHAH-Ge layer should suppress this leakage path.

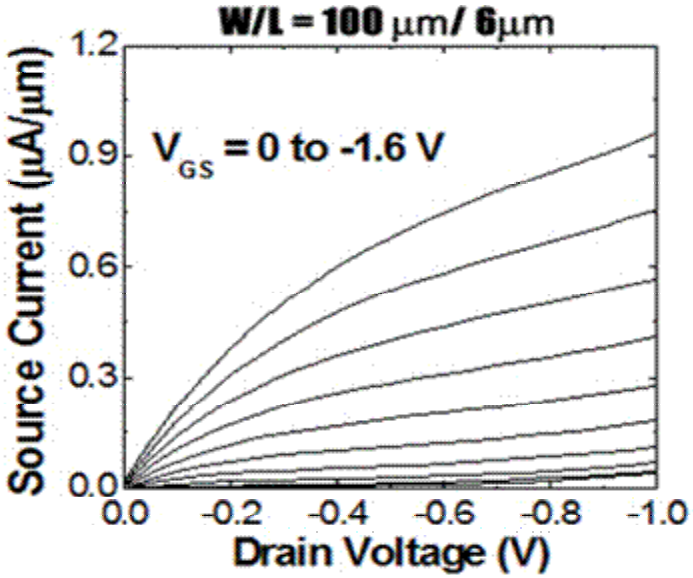

Figure 5.8: Measured I_s-V_s characteristics.

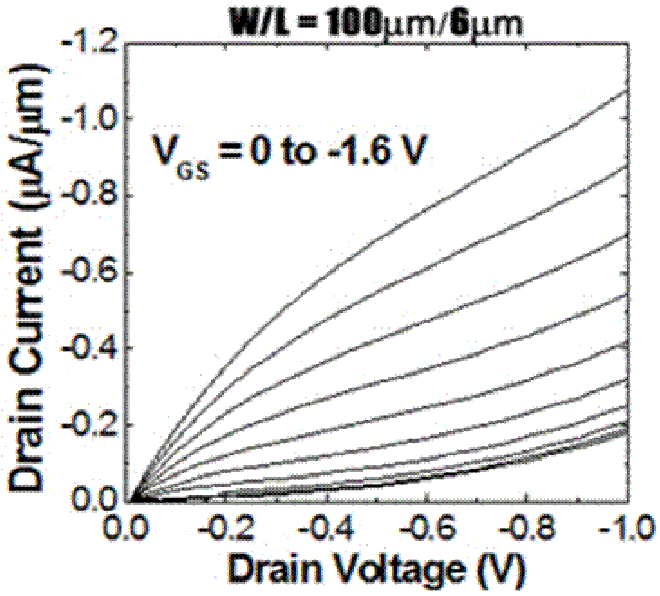

Figure 5.9: Measured I_d-V_d characteristics.

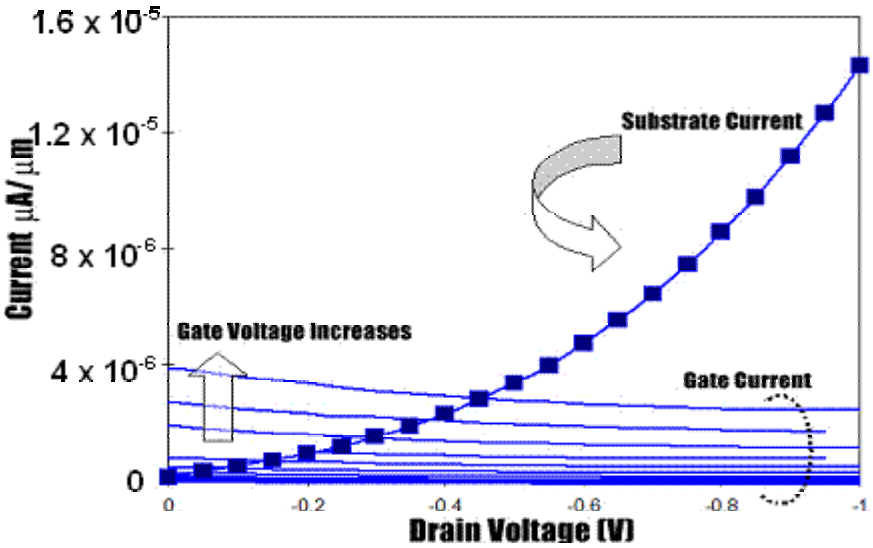

Figure 5.10: I_{sub}/I_{gate}-V_d characteristics; I_{sub} is independent of Vg.

Effective mobility μ_{eff} was extracted using the simple I_d-V_d method according to

$$\mu_{eff} = \left(\frac{2L}{W}\right) \times I_d \times \frac{1}{C_{ox}\left(V_g - V_t\right)^2} \tag{5-1}$$

Threshold voltage, V_t was extracted to be 0.7 V from I_d-V_g slope extrapolation. The V_t shift on this p-MOS device is due to the p-type SiGe doped gate electrode. Effective mobility (μ_{eff}) was calculated at two points to be ~ 250 cm^2/V-sec at V_g-V_t = 80 mV and ~ 95 cm^2/V-sec at V_g-V_t = 1V, which corresponds to low and high effective fields respectively. We should note that this procedure overestimates the amount of charge in the channel and thus gives underestimates of the mobility. The effective field can be calculated for holes from Gauss's law using

$$E_{eff} = \frac{1}{\varepsilon_{Ge}}\left(\left|Q_d\right| + \frac{1}{3}\left|Q_i\right|\right) \tag{5-2}$$

where Q_d is the depletion charge and Q_i is the inversion charge. This equation can be simplified using

$$\left|Q_d\right| = C_{ox}\left(V_t - V_{fb} - 2\psi_B\right) \tag{5-3}$$

and

$$\left|Q_i\right| = C_{ox}\left(V_g - V_t\right) \tag{5-4}$$

to

$$E_{eff} = \frac{V_t - V_{fb} - 2\psi_B}{3t_{ox}} + \frac{V_g - V_t}{9t_{ox}} \tag{5-5}$$

where Ψ_B is the separation of the fermi level from the midgap in Ge, and V_{fb} is the flat band voltage [52]. Using the doping concentration and the work function of the SiGe gate and of Ge, we calculated using equation (5-5) that V_g-V_t = 80 mV corresponds to an effective field of 0.138 MV/cm and V_g-V_t = 1 V to 0.79 MV/cm. Using the universal mobility curves we find that for silicon at effective fields of 0.138MV/cm and 0.79MV/cm, effective mobilities are approximately 125 cm^2/V-s and 69 cm^2/V-s respectively [53]. Thus the MHAH-Ge devices show a 2× enhancement in mobility at low effective fields and a 1.5× enhancement at high fields. Figure 5.11 plots mobility vs. effective field for both MHAH-Ge pMOS and Si universal mobility. The high effective mobility measured in our devices indicates the high quality of the MHAH-Ge substrate grown.

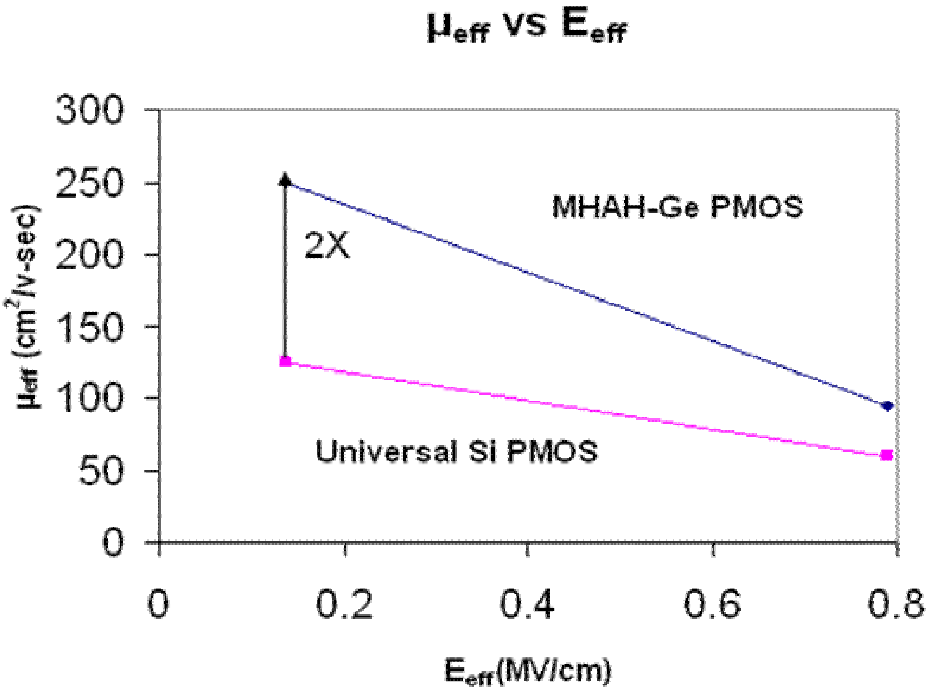

Figure 5-11: Mobility vs. Effective Field

5.4 High-κ Dielectric and Metal Gate Compatibility

5.4.1. Background

As described in chapter 2, high-κ dielectric and metal gate have become a serious option for 45nm technology. The shift to high-κ/metal gate will eliminate dopant-depletion effects in polysilicon, decreasing T_{ox} inversion and thus increasing the transistor performance. In addition, it will reduce I_{gate} due to the thicker physical thickness allowed and possibly allow for continued scaling of EOT as predicted by the ITRS roadmap. With any new semiconductor growth technology, as our MHAH-Ge growth method, it is important to test for high-κ/metal gate compatibility.

5.4.2 High-κ/Metal Gate Fabrication/Results

Using a 4.5 μm MHAH-Ge layer as the starting substrate, MOS capacitors with a gate stack of aluminum/aluminum oxide (Al/Al_2O_3) were fabricated. The MHAH-Ge wafers were cleaned using cyclical rinsing between HF and DI water prior to high-κ growth as described before. 80Å Al_2O_3 film was grown by ALD using TMA as the precursor for Al and ozone as the oxidant. Afterwards, 1000Å Al gate electrode was deposited by e-beam evaporation. Table 5.3 shows the complete process flow of the MOSCAP.

Figure 5.12 shows bi-directional high frequency (100 kHz and 1 MHz) CV characteristics. The CV's show a negative 1.5V V_{fb} shift not seen in Al_2O_3 MOS-cap

fabricated on Si. This indicates the presence of positive oxide charge. Also hystersis was extracted to be 100mV. Frequency dispersion in inversion could indicate the presence of increased trap sites near the Al_2O_3/Ge interface. In addition figure 5.12 shows the effect of a forming gas anneal (FGA) at 350^{o}C for 30min. This shows a 0.5V positive V_{fb}, indicating a reduction in interface charge. C_{ox} increases after FGA suggesting the possible presence of a GeO_x layer. Figure 5.13 also shows a reduction in gate leakage after FGA due to a reduction in interface states or possible growth of a GeO_x layer. This high-κ was done in collaboration with Duygu Kuzum and will be a continued in her future research.

Step	Comment
MHAH Ge Growth	To growth low defect density Ge on Si
Ge surface cleaning	Cyclical HF. Multiple cycles of (50:1) HF followed by DI water for a total of 12 times each 15sec
High-κ Growth	Al_2O_3 ALD using TMA as the precursor for Al and ozone as the oxidant
Gate Metal	Al e-beam evaporation through a shadow mask
FGA	Forming Gas Annealing 300°C to passivate the Ge/GeO_XN_Y interface

Table 5.3: High-κ Metal Gate MHAH-Ge MOS CAP Process Flow

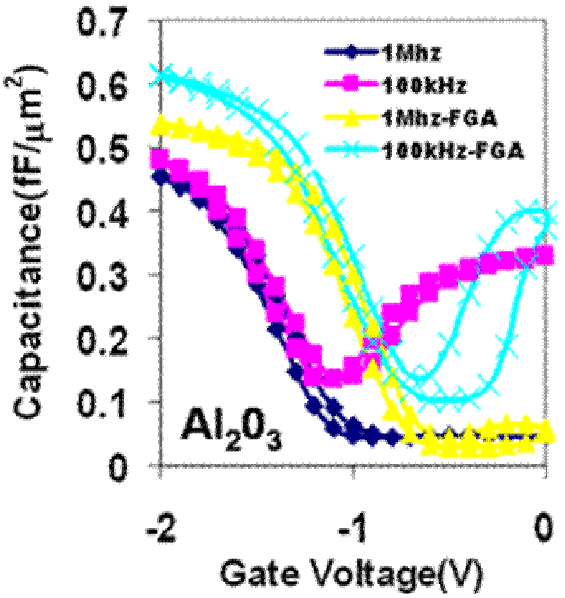

Figure 5.12: Bi directional CV characteristics of Al/Al_20_3 MOSCAPs on p-type Ge layer; CV Characteristics before and after FGA

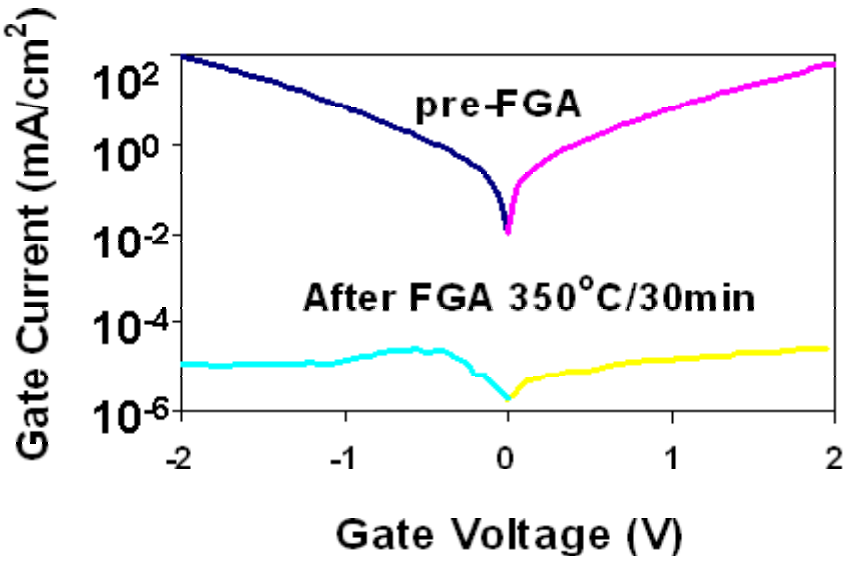

Figure 5.13: Gate current vs. gate voltage (V) of Al/Al_20_3 MOSCAPs before and after FGA

5.5. MSM PHOTODECTOR

5.5.1. Background

In addition to electrical compatibility, optical compatibility of MHAH-Ge is an indication of the quality of the layer. Due to its inherent large bandgap, Si is not an efficient optical material at wavelengths in the range 1.3-1.55 μm, a window required for medium- and long-haul optical fiber communications. As a result, Ge, with a lower bandgap, has been emerging as a viable candidate for integration with Si for low-cost transceivers to overcome the spectral limit of Si photodetectors. Moreover, the interest is strengthened by its compatibility with Si CMOS technology, prompting researchers to focus on developing procedures for integration of SiGe and Ge photodetectors on Si.

Several technologies have been employed to grow Ge heteroepitixally on Si and allow the fabrication of efficient photodetectors. For instance, superlattice buffer layers were used to avoid the large lattice mismatch. Using this procedure, p-i-n Ge detectors on Si with a quantum efficiency of 40% at 1.3 μm were demonstrated [54]. Heteroepitaxial growth of Ge on Si followed by cyclic thermal annealing is also a technique used to achieve better quality Ge layers. With such technologies, p-i-n detectors have been built on 4 μm Ge layers grown on Si using a low temperature buffer layer [55], yielding responsivity $\Re \sim 0.89$ A/W at 1.3 μm. Moreover, with this technology, 52% quantum efficiency at 1.3 μm was demonstrated on 1 μm Ge films

grown on Si [56]. Using dual strain-relaxed buffer layers, very high 3dB bandwidth up to 38.9 GHz was demonstrated on vertical p-i-n detectors with 300 nm intrinsic regions [57].

The next section will detail the fabrication and demonstration of high quality Ge based MSM-PDs using the MHAH method [58]. We demonstrate responsivities as high as 0.85 A/W at 1.55 μm and 2 V reverse bias. This technology is promising to realize monolithically integrated optical links as an alternative to electrical interconnects. This work was done in collaboration with Ali Okyay. It should be noted that only a highlight of the work will be presented here with the rest to be published in the PhD thesis of Ali Okyay.

5.5.2 MSM Fabrication and Results

We used a ~ 4.5 μm high quality intrinsic *MHAH*-Ge layer on Si as the starting substrate. We then fabricated MSM-PDs with interdigitated electrode width and spacing ranging from 1 to 10 μm in active absorption regions of 10^2-10^4 μm^2 [58]. Intrinsic Ge was chosen to allow low voltage device operation. A 3000 Å thick low temperature chemical vapor deposited oxide (LTO) layer was deposited at 400 ^oC for surface passivation. This oxide layer was patterned and HF-etched followed by metal electrode e-beam evaporation and photoresist liftoff. Fig. 5-14 shows a schematic of the final structure. About 150 Å of Ti, Cr, or Ni were used for work function control and adhesion and topped with ~ 350 Å of Au to allow high-speed measurements. No

thermal treatments were performed afterwards to avoid inter-diffusion and alloying between semiconductor and metal.

Fig. 5-15 plots $\Re$ vs. reverse bias for Ti-Ge-Ti photodetectors operated at 1.55 μm_with 330 μW incident intensity. The active absorption area of the device is 10^4 μm^2 with 5 μm electrode spacing. We observe responsivities of 0.76 A/W under 1 V reverse bias, corresponding to 61% external quantum efficiency (η). The highest $\Re$ of 0.85 A/W, corresponding to $\eta \sim 68\%$ was observed from a detector with 5 μm electrode width and spacing. Under similar conditions, the theoretical maximum collection efficiency, for a film of 4.5 μm thick, is 88% without accounting for reflections from the surface. Detectors were not optimized for fast response due to lithographic resolution capabilities.

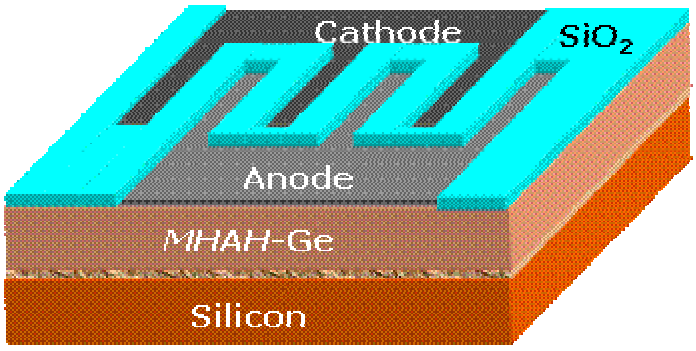

Figure 5.14: Cross-section of MSM photodetector fabricated on MHAH-Ge layer grown on Si starting substrate. SiO_2 layer was deposited and patterned before the e-beam evaporation of the metal electrodes. Defects are concentrated near the Si/Ge interface.

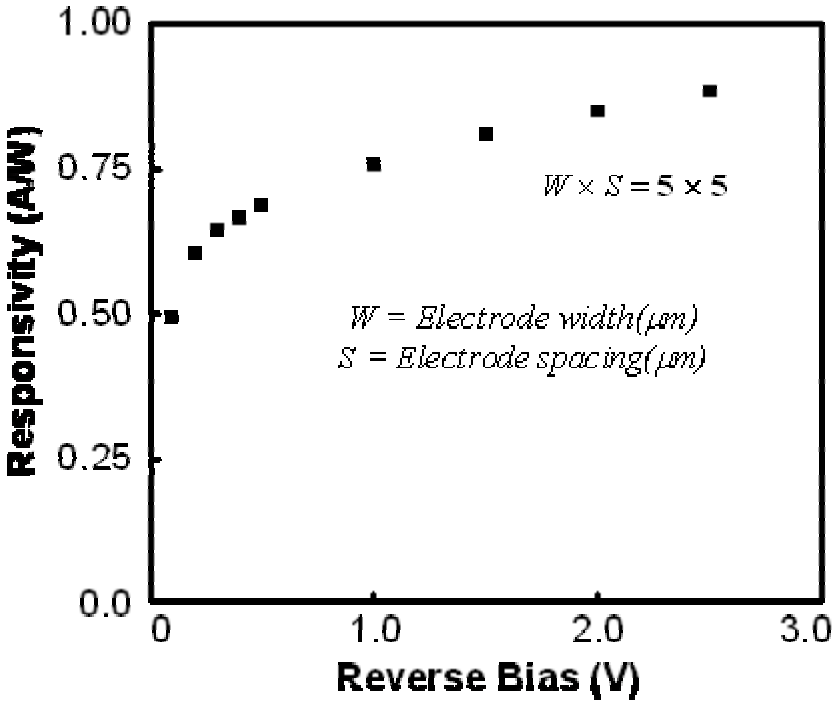

Figure 5.15: Photodetector responsivity at λ=1.55 μm versus reverse bias for Ti-Ge-Ti MSM-PDs with 5 μm finger width and spacing and 10^4 μm^2 active area.

5.6 Conclusion

In conclusion, chapter 5 presented both electrical and optical compatibility of MHAH-Ge. MOSCAPs were fabricated with excellent CV characteristics and low D_{it}. We have also successfully demonstrated a high mobility Ge based p-MOSFET and a Ge MSM photodetector with high efficiency. High-κ/metal gate compatibility of the

layers for MOS technology applications was also demonstrated. Finally, these results indicate that the MHAH-Ge layer is approaching the electrical quality of bulk Ge. Chapter 6 will summarize the thesis and describe recommendations for future work.

CHAPTER 6

Summary and Future Work

6.0 Abstract

In this work, we have developed a novel technique to grow high quality germanium on silicon by multiple steps of growth and hydrogen annealing. The technique was coined "Multiple Hydrogen Annealing for Heteroepitaxy, *MHAH*". In addition it was shown, both electrically and optically, that MHAH-Ge approaches the quality of bulk Ge. The following chapter will summarize the key achievements and list recommendations for future work.

6.1 Summary

Germanium has been emerging as a viable candidate to augment silicon for CMOS and optoelectronic applications. Thus it is pivotal to develop new methods for heteroepitaxial Ge technology. However, Ge growth on Si is hampered by the large

lattice mismatch (4.2%) between Ge and Si. The large mismatch results in growth that dominated by "islanding" and misfit dislocations, rendering the layer obsolete.

We have developed a procedure to grow high quality thick heteroepitaxial-germanium layers on silicon. With this technique of *Multiple Hydrogen Annealing for Heteroepitaxy* (MHAH), high quality heteroepitaxial Ge layers on Si are can be grown. The technique involves CVD growth of Ge on Si, followed by in-situ hydrogen annealing with subsequent growth and annealing steps. Misfit dislocations are concentrated at the Si/Ge interface rather than threading to the surface as expected in this 4.2% lattice-mismatched system. Using this technique Ge layers were grown on Si with dislocation densities as low as $1x10^{7}cm^{-2}$ and R_{rms} surface roughness as low as 2.5nm.

In addition, a complete experimentally based theoretical model was developed. The model shows that hydrogen annealing removes any native oxide from the surface allowing for high temperature Ge surface diffusion, which is governed by the surface chemical potential, to take place. Because the diffusion takes place from regions of high chemical potential to regions of low chemical potential in the strain relaxed film, the Ge layer flattens out to a smooth layer. Also, during the hydrogen annealing, the model shows that the high temperature leads to dislocation motion and subsequent annihilation. The combination of these two mechanisms and the multiple growth aspect of MHAH leads to a homoepitaxial step resulting in very high quality Ge layers.

Using these layers, high quality MOSCAPS were fabricated with excellent CV characteristics and low $D_{it.}$ Also high-κ/metal-gate compatibility with MHAH-Ge was demonstrated by fabrication of MOSCAPS. In addition, a high performance

MHAH-Ge p-MOSFET was demonstrated with peak mobility of 250 cm^2/V-sec. We also demonstrate extremely efficient metal-semiconductor-metal photodetectors (MSM-PD) with responsivities ($\Re$) as high as 0.85 A/W at 1.55 μm and 2 V reverse bias. This technology is promising to realize monolithically integrated optical links as an alternative to electrical interconnects. Finally, these results indicate a promising step in achieving heterogeneous integration of a high mobility pure Ge channel transistor directly on Si using high-κ/metal gate which may be used in future technology nodes.

6.2 Recommendations for Future Work

This work constitutes a comprehensive investigation into growth of relaxed germanium on silicon. Using this method developed exiting research topics can be investigated further and will be listed here.

1. MHAH-Ge NMOS transistor: With bulk Ge NMOS showing poor mobility some researchers suggest that NMOS mobility may be degrading by the quality of the bulk Ge or by the doping species of p-type Ge. This can be investigated by fabricated NMOS transistors using MHAH-Ge.
2. Modified MHAH growth process: Using a modified version of MHAH, can thinner layers of germanium on silicon be grown? Can the dislocation density be further reduced? One possible idea is use more cycles of growth and annealing for shorter times. Or alternatively use more cycles and longer annealing times.

3. Selectively grow MHAH-Ge on patterned SiO_2 substrates: The idea is to make active area islands of Ge on Si. The active area islands can be used for fabrication of Ge devices.
4. Fabrication of Germanium on Insulator (GOI): Transfer the high-quality MHAH-Ge layer to a handle Si wafer with SiO_2. This can be done by simply bond and etch-back, smart cut, or by using porous silicon. The challenge here is also how to deal with the defect region near the Si/Ge interface vital to the MHAH-Ge method. Figure 6.1 highlights a method that uses porous silicon and MHAH-Ge to make GOI. In the method, MHAH is used as the starting substrate and CVD Ge is then grown on the porous Ge. After that the Si/MHAH-Ge/porous-Ge/CVD-Ge substrate stack is bonded to a SiO_2/Si handle wafer. Then a water jet is used to remove the original Si substrate/MHAH-Ge and some of the porous Ge. During this removal the defective region of the original MHAH is also removed. The remaining porous Ge layer is selectively etched leaving a defect free CVD germanium layer on SiO_2 on Si which is Germanium On Insulator (GOI).

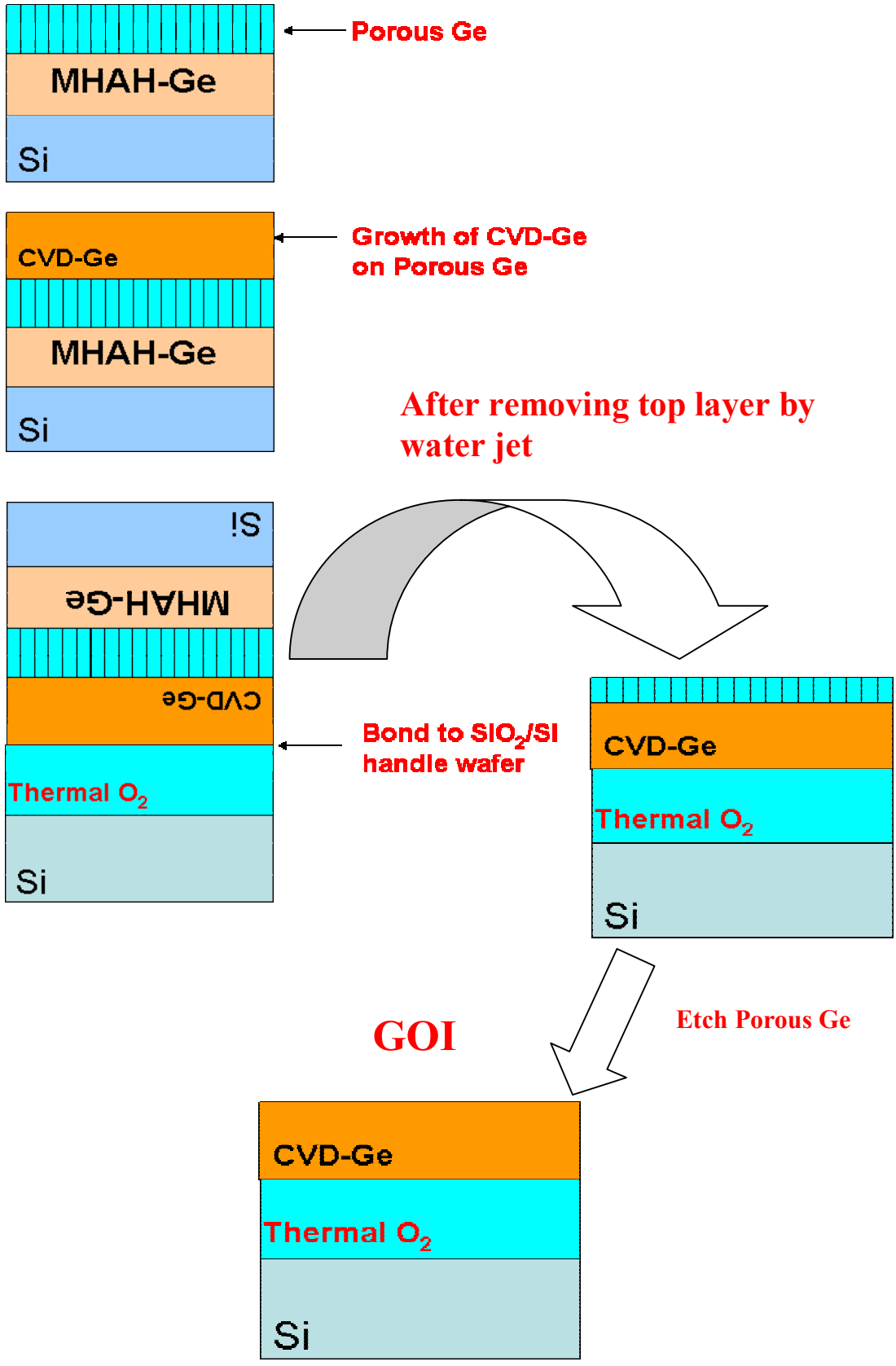

Figure 6.1: Fabrication of Germanium on Insulator (GOI) using MHAH-Ge and porous-Ge.

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